Accurate, Compact, and Power Efficient Li-Ion Battery Charger Circuit

Min Chen, *Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Senior Member, IEEE*
Georgia Tech Analog and Power IC Design Lab

***Abstract*— A novel, accurate, compact, and power efficient Lithium-Ion (Li-Ion) battery charger designed to yield maximum capacity, cycle life, and therefore runtime is presented and experimentally verified. The proposed charger uses a diode to smoothly (i.e., continuously) transition between two high gain linear feedback loops and control a single power MOS device, automatically charging the battery with constant current and then constant voltage. An adaptive, power efficient charging scheme in the form of a cascaded switching regulator supply ensures the voltage across the charging power-intensive PMOS remains low, thereby reducing its power losses and yielding up to 27% better overall power efficiency. An 83% power efficient PCB prototype was built and used to charge several Li-Ion batteries to within ±0.43% of their optimum full-charge voltage and therefore within a negligibly small fraction of their full capacity.**

***Index Terms*— Adaptive power supply, constant current charger (CC), constant voltage charger (CV), Li-Ion battery, linear charger, switching charger.**

I. Introduction

LITHIUM-ION (Li-Ion) batteries are widely used in portable electronics such as cell phones, PDAs, laptops, and the like because of their high energy density, long cycle life, high voltage, and absence of memory effects [1]. However, the fragile nature of Li-Ion batteries to over-charged voltages imposes stringent charge requirements on the design, especially when slightly under-charged voltages significantly reduce capacity. Under-charging the battery by 1.2% of its optimum full-charge voltage, for example, incurs a 9% capacity loss [2]. Consequently, charging a Li-Ion battery to within 1% of its optimum full-charge voltage is prudent and common-place, and considered to yield maximum capacity and cycle life [3].

Power and size are also important parameters in portable electronics. High power efficiency is critical in mobile high temperature and energy-deficient environments, like the cellular phone and other power intensive portable devices, because of heat sink and therefore board space requirements. The charger must therefore be compact, power efficient, and accurate, an embodiment of which is proposed here.

Section II of this paper reviews Li-Ion charging considerations and various state-of-the-art schemes. Section III introduces, explains, and formally discusses the stability and design constraints of the proposed linear charger circuit, followed by experimental results in Section IV. Section V and VI discuss power efficiency and how a cascaded adaptive switching regulator is used to relax the ratings of the power PMOS and improve overall efficiency performance. Finally, conclusions are drawn in Section VII.

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The authors are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: minchen@ece.gatech.edu, rincon-mora@ieee.org).

II. Background

Li-Ion chargers generally extract unregulated dc power from an ac wall outlet or a dc power source, such as USB supplies, on-board batteries, fuel cells, and others, and use it to charge batteries via a combination of linear and switching regulators, as shown in Fig. 1(a). To quickly, safely, and efficiently charge a Li-Ion battery, charger circuits typically start by sourcing a regulated current into the battery and end by forcing whatever decreasing current is necessary to charge the battery to a regulated full-charge voltage, all of which constitutes the well-known constant current-constant voltage (CC-CV) technique, as conceptually shown in Fig. 1(b) [1].

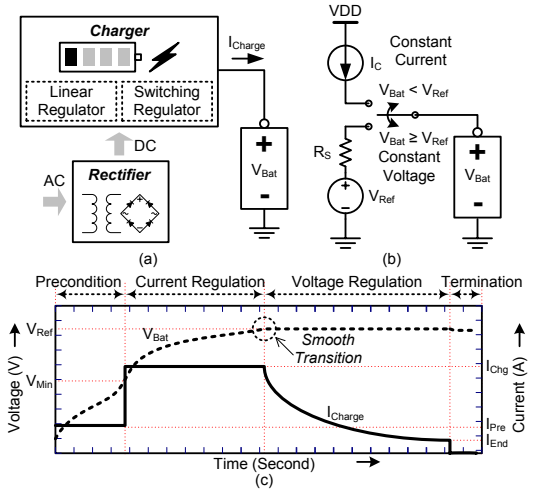

Fig. 1. (a) Typical Li-Ion battery charger and constant current-constant voltage
(CC-CV) charging (b) scheme and (c) sequence.

The CC-CV charging procedure, shown in Fig. 1(c), starts with a pre-conditioning phase, if the battery is deeply discharged and its voltage is consequently below minimum charging limit V_{Min}. Small current I_{Pre} is therefore sourced until the battery is ready for full charging conditions, at which point higher constant current I_{Chg} is applied, which is the current-regulation phase. When the battery voltage nears full-charge voltage V_{Ref}, it enters the voltage regulation phase, thereby gradually decreasing the charge current as the battery slowly reaches V_{Ref}. The charging cycle ends when the sourcing current falls below end-of-charge current I_{End}, which is

low.

Key to CC-CV chargers is how to smoothly and properly transition between the current and voltage sources shown in Fig. 1(b). In practice, current and voltage feedback loops are used to regulate the charging process, giving rise to three distinct regions of operation: constant current, current-voltage, and constant voltage regions. Transitioning between the two feedback loops is therefore a critical feature for safe and uninterrupted charging sequences.

Relatively complex switching circuits are normally used to transition between these two aforementioned feedback loops, both in academic circles and commercial products. Jung *et al.*, for instance, use two PNP transistors to switch between a current and a voltage loop, both of which share the same class-AB output stage [4]; Lima *et al.* concurrently operate a continuous, low-gain, high-bandwidth current loop and a complex, switched-sampled, high-gain, low-bandwidth voltage loop [5]; Tsai *et al.* switch between two separate low dropout (LDO) regulators (i.e., two complete shunt-feedback loops) [6]; and Liu *et al.* and Demian *et al.* employ a field programmable gate array (FPGA) and a microcontroller to determine which loop to operate [7-8]. Commercial charging ICs are no different and use analog "OR" functions and/or digital circuits to switch between the two loops [9]. In all, the interdependence and interaction of the two complex interconnected loops compromise stability and therefore complicate the design, in other words, increase cost and component count and decrease yield. The proposed charger circuit shares a single power PMOS charge device and combines two relatively simple feedback loops via a diode, achieving the stability and accuracy required for safe operation and maximum capacity.

III. Proposed Charging Circuit

The proposed solution sources the pre-conditioning and constant charging currents through a power PMOS device whose gate is controlled by the output of a transconductor (G_{mi}) connected in series feedback, as shown in Fig. 2. Voltage V_C is impressed across resistor R_C and therefore determines the value of charge current I_C, which is low for pre-conditioning and higher for the charging cycle. The voltage, shunt-feedback loop is comprised of the same charging power PMOS and a low-impedance operational amplifier A_V, which are used to regulate battery voltage V_{Bat} to full-charge voltage V_{Ref}. Series diode D_{SW} determines which and how these two feedback loops are to operate, and comparator C_{end} disables the whole charging process through pull-up transistor M_{End} (i.e., shut off charge PMOS device M_P) when charge current I_C is below pre-set value I_{End} [10].

Key to the transitional phase of this circuit is the interaction and changing impedances of diode D_{SW}, amplifier A_V, and transconductor G_{mi}. If V_{Bat} is well below the reference, for instance, amplifier A_V attempts to sink current but diode D_{SW} prevents it (i.e., switch D_{SW} is off), allowing the current loop to dominate. On the other hand, when V_{Bat} is close to V_{Ref}, A_V sources current through the diode to increase the gate voltage of M_P and therefore decrease charge current I_C. When D_{SW} conducts, the impedance at the gate of M_P is low and the gain of the current loop is therefore negligibly small, allowing the voltage loop to dominate the charging process.

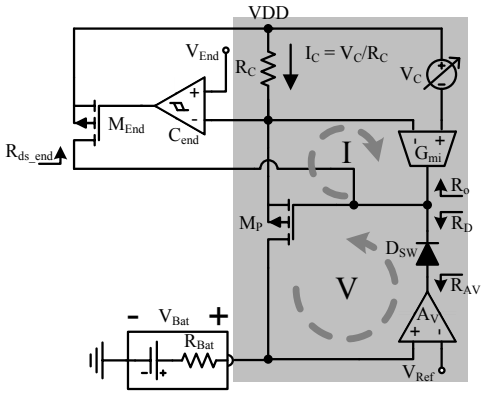

Fig. 2. Proposed charger circuit.

In the constant-current region, dominant low-frequency pole p_{Gate} is at the gate of M_P because its impedance is the highest in the loop – high output resistor R_o of transconductance amplifier G_{mi}. Its frequency response has therefore a single pole drop-off and yields a phase-margin of 90°, as shown in Fig. 3(a), where the circuit was simulated using vendor-provided sub-circuit models for the various discrete components. For the constant-voltage loop, the gate of M_P is no longer the dominant low frequency pole because its impedance is now shunted by A_V, whose output resistance is low. The dominant pole for this loop is A_V's internal pole p_{AV}, as shown in Fig. 3(c).

In the current-voltage region, current loop gain LG_I decreases and its bandwidth increases because its gain- and bandwidth-setting resistance (at the gate of M_P) decreases as diode D_{SW} starts to conduct, which is the same reason why voltage loop gain LG_V simultaneously increases, now that D_{SW} starts to short-circuit and close the voltage feedback loop. The overlap of these two responses introduces a left-hand plane (LHP) zero into the p_{Gate}-p_{Av} mix, as shown in Fig. 3(b).

For analysis, the loop is "broken" at the gate of M_P, which results in two parallel feedback paths, LG_I and LG_V, and whose total loop gain LG is simply their sum. When plotted in dB (i.e., logarithmic scale), the sum of LG_I and LG_V in dB is approximately the maximum of the two (i.e., $LG \approx \mathrm{Max}(LG_I, LG_V)$), as shown by the solid (LG), dotted (LG_V), and dashed (LG_I) traces in Fig. 3. Consequently, assuming R_{AV} and R_o are low and high, respectively, and r_{ds_end} is negligibly high, the open-loop gains of the current and voltage loops are

$$LG_I = \left(\frac{g_{mp}R_C}{1+g_{mp}R_C}\right)\left(-G_{mi}\left[R_o \parallel R_D \parallel \frac{1}{sC_g}\right]\right) = \frac{-K_I}{1+sC_g\left(R_o \parallel R_D\right)} \qquad (1)$$

and

$$LG_V = \left(-\frac{g_{mp}R_{Bat}}{1+g_{mp}R_C}\right)\left(\frac{A_V}{1+s/p_{AV}}\right)\left(\frac{R_o \parallel 1/sC_g}{R_D+R_o \parallel 1/sC_g}\right), \qquad (2)$$

$$= \frac{-K_V}{\left(1+s/p_{AV}\right)\left(1+sC_g\left[R_o \parallel R_D\right]\right)}$$

where g_{mp} and G_{mi} are the transconductances of M_P and G_{mi} and R_o and R_D are the output resistor of G_{mi} and the equivalent ac resistance of D_{SW}, respectively. In the narrow current-voltage region, the system loop gain is

$$LG = LG_I + LG_V = (K_I + K_V)\cdot\frac{1 + s\,K_I/((K_I + K_V)p_{AV})}{(1 + s/p_{AV})\cdot(1 + sC_g(R_o \,||\, R_D))}. \quad (3)$$

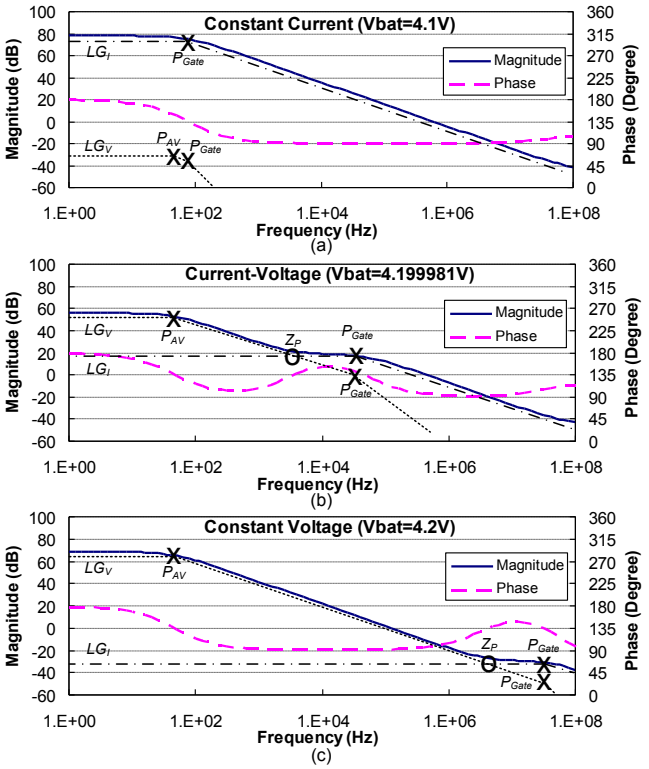

Fig. 3. Simulated Bode plots during constant- (a) current, (b) current-voltage, and (c) voltage regions.

As R_D changes from infinity (D_{SW} is off) to a negligibly small value (D_{SW} is on) and therefore gain K_V increases from zero to a high value, p_{Gate} shifts to higher frequencies and LHP zero z_p from p_{Av} also to higher frequencies. This pole-zero-pole staircase shifts continuously and monotonically, guaranteeing a phase-margin performance of 90° throughout all regions, including the transitional phase, when the current and voltage loops are both engaged. Consequently, unlike threshold-based schemes, the transition is monotonically continuous ("smooth") and unconditionally stable, as shown in Fig. 4(b).

IV. Experimental Results

A printed-circuit board (PCB) prototype of the proposed circuit shown in Fig. 2 charged several 800 mAh Li-Ion batteries with a constant charge current of 800 mA, a constant full-charge voltage of 4.2 V, and an end-of-charge current of 50 mA. The battery was fully charged in less than 1.7 hours. Although shorter charge times are possible with higher charge currents, Li-Ion chemistries respond better (i.e., have higher capacities) when charged at slower rates. As illustrated in Fig. 4, the transition from current to voltage regulation is monotonically continuous – voltage slowly increases from 4.2 V to 4.206 V while charge current gradually decreases from 800 mA to 50 mA. The 6 mV end-of-charge voltage error includes line regulation (ΔV_{LNR}), load regulation (ΔV_{LDR}), and gain (ΔV_{Gain}) error effects. The bandgap-derived 5 V reference chip has a maximum error of ±0.2% (ΔV_{REF}) from -40 to 85 ºC and the Op-Amp chip has less than 3 mV of input-referred offset voltage (ΔV_{Offset}), leading to a worst-case accuracy error of approximately ±0.43%,

$$\frac{\Delta V}{V_{REF}} = \frac{\Delta V_{LNR} + \Delta V_{LDR} + \Delta V_{Gain} + \Delta V_{REF} + \Delta V_{Offset}}{V_{REF}} = \pm\frac{17.9mV}{4.2V} = \pm 0.43\% \quad (4)$$

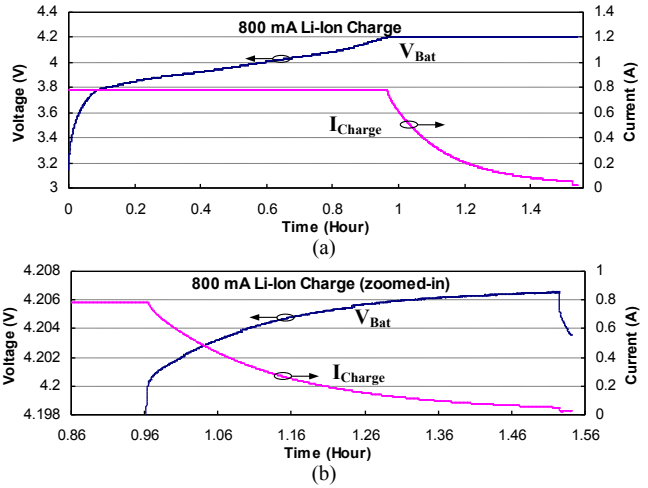

Fig. 4. Experimental Li-Ion battery charge curves using the proposed charger circuit: (a) expanded and (b) zoomed-in scales.

V. Proposed Power Efficient Charging Scheme

As mentioned in Section I, power efficiency is a critical design specification, especially for integrated solutions. Almost all charger IC vendors consequently provide two types of solutions, linear and switching chargers for accuracy and efficiency, respectively [9]. Conflicting design tradeoffs exist between efficiency and accuracy: linear solutions sacrifice efficiency for accuracy while switching circuits trade noise and accuracy performance for improved efficiency [11-12]. This tradeoff explains why Jung *et al.* use a linear regulator and a switching converter in parallel for both accuracy and efficiency [4]. Their scheme, unfortunately, suffers from complexity and therefore compromised loop stability and reliability.

Linear chargers lose their power efficiency across the charging power PMOS device, since it sources significant current while dropping a non-negligible voltage across it (dropout voltage V_{DO}),

$$V_{DO} = V_{DD} - V_{Bat}, \quad (5)$$

where V_{DD} is a standard, pre-determined input supply above 4.2 V and V_{Bat} can be as low as 2.7 V. The worst-case efficiency of the linear circuit for a 5 V supply is therefore less than 54%,

$$\eta_{Chg\_Linear} = \frac{V_{Bat} I_{Bat}}{(V_{DD} - V_{Bat})I_{Bat} + V_{Bat} I_{Bat} + P_{Other}} \le \frac{V_{Bat}}{V_{DD}}, \quad (6)$$

where P_{Other} are other charger-related losses (e.g., feedback amplifiers) and V_{DD} and V_{Bat} are 5 and 2.7 V, respectively. The charging MOS device can consequently dissipate up to 2 Watts, which requires heat sinks and the like.

In the case a suitable supply voltage (i.e., higher than 4.2 V) is not available, a switching boost regulator with a 4.5 V out-

put, for instance, is required, which degrades overall efficiency performance (η_{Chg_Switch}) by that of the boosting supply (η_{Switch}),

$$\eta_{Chg\_Switch} = \left(\frac{V_{Bat} I_{Bat}}{V_{Switch} I_{Bat} + P_{Other}}\right)\eta_{Switch} \le \left(\frac{V_{Bat}}{V_{Switch}}\right)\eta_{Switch}, \quad (7)$$

where V_{Switch} is the output voltage of the boosting supply. The resulting worst-case efficiency can be less than 54% for a 4.5 V V_{Switch}, 2.7 V V_{Bat}, and a 90% efficient switching supply circuit.

To improve overall power efficiency performance, an adaptive supply scheme is proposed, whereby the voltage across the two most power-consuming components of the linear charger circuit, current-sensing resistor R_C and power PMOS M_P, is kept low and constant throughout the charging process:

$$\eta_{Chg\_Adapt} = \left[\frac{V_{Bat} I_{Bat}}{(V_{Adapt} - V_{Bat}) I_{Bat} + V_{Bat} I_{Bat} + P_{Other}}\right]\eta_{Adapt} = \left[\frac{V_{Bat} I_{Bat}}{V_{Const} I_{Bat} + V_{Bat} I_{Bat} + P_{Other}}\right]\eta_{Adapt} \le \left[\frac{V_{Bat}}{V_{Const} + V_{Bat}}\right]\eta_{Adapt} \quad (8)$$

and

$$\eta_{Adapt} = \frac{V_{Adapt} I_{Bat}}{V_{Adapt} I_{Bat} + P_{Cond.} + P_{Switching}}, \quad (9)$$

where V_{Const} is the constant voltage applied across R_C and M_P and V_{Adapt}, η_{Adapt}, $P_{Cond.}$, and $P_{Switching}$ are the output voltage, efficiency, and corresponding conduction and switching power losses of the adaptive supply circuit. As with most switching regulators, since $P_{Cond.}$ across the power switches and inductor's equivalent series resistor (ESR) are directly proportional to the square of the load (charge) current ($P_{Cond.} \propto I_{Bat}^2$), η_{Adapt} increases with decreasing I_{Bat} (i.e., $P_{Cond.}$ outpaces $V_{Adapt}I_{Bat}$), but only until $P_{Cond.}$ decreases below $P_{Switching}$, at which point $P_{Switching}$ dominates and η_{Adapt} decreases with decreasing I_{Bat}. But as verified in Fig. 7, the overall variation of η_{Adapt} is minimal and therefore assumed constant. The resulting worst-case efficiency for a 90% efficient supply circuit, 300 mV V_{Const}, and 2.7 V V_{Bat} is less than 81%, approximately 27% better than the non-adaptive supply schemes.

Fig. 5(a)-(b) illustrates a prototype embodiment of the proposed charger circuit shown in Fig. 2 with the power efficient charging scheme, where the adaptive supply is built with TI's TPS61030 boosting switching supply chip and the adaptive reference is generated from a combination of two level-shifting Op Amps, all of which force a constant voltage (e.g., 0.3 V) across R_C (0.1 Ω) and M_P throughout the charging process. The experimental results shown in Figs. 5(c) and 6 verify the functionality, start-up, and battery-tracking features of V_{Adapt} for an input supply voltage of 2.7 V and an 800 mAh Li-Ion battery. The linear charger suppresses approximately half the adaptive supply ripple. More rejection can be achieved if the switching frequency of the adaptive supply (600 kHz) were well within the bandwidth of the linear charger (less than 100 kHz) – this was not adjustable in the prototype built. As shown, supply and ground bounce noise were well within acceptable limits.

To gauge the efficiency performance of the proposed adaptive scheme, the measured efficiency results of the PCB prototype are compared against a conventional, non-adaptive boosting supply circuit with the same input voltage (2.7 V) so that no differences in the power conversion ratios of the stage driving these supplies are introduced. For completeness, the efficiency performance of the linear charger circuit alone, which requires a 5 V supply, is also included. The PCB prototype had 83% efficiency for most of the charging phase, well above the theoretical efficiencies of the 5 V supplied and 2.7 V supplied (charger and 90% efficient non-adaptive boosting supply circuit), as shown in Fig. 7. The efficiency of the prototyped circuit peaked when the charging current started to drop, corresponding to an increase in the boosting supply circuit's efficiency performance. The overall efficiency ultimately drops as charging current continues to decrease because the efficiency of the boosting supply circuit degrades (switching losses become dominant) and other charger-related losses (P_{Other}) start to overwhelm current-dependent losses ($P_{Cond.}$).

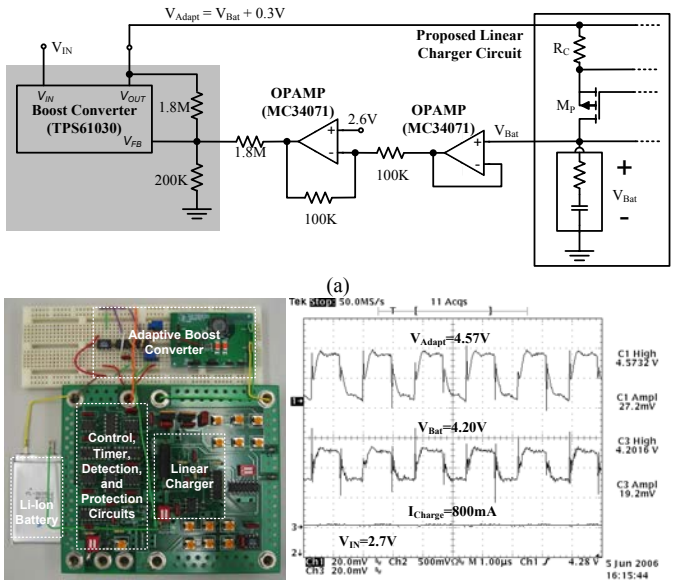

Fig. 5. (a) Schematic and (b) PCB prototype of the proposed power efficient charging scheme and (c) time-domain snapshots of V_{Adapt} and V_{Bat}.

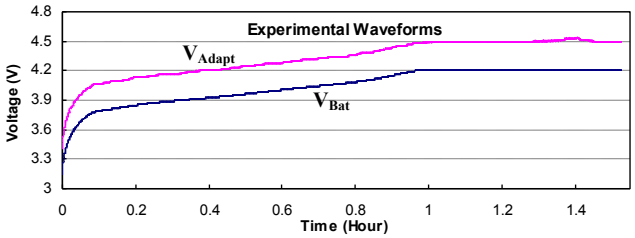

Fig. 6. Experimental start-up and charging sequence (data points collected from HP-IB controlled HP 3478A 5.5 digital multi-meters).

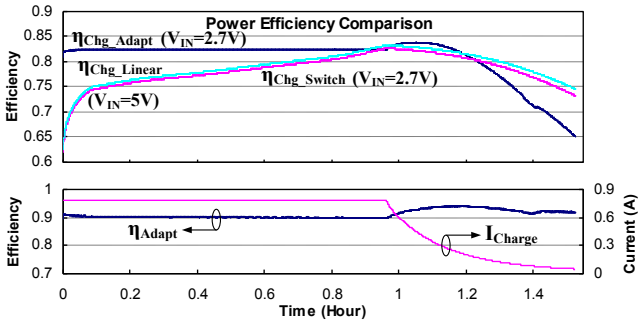

Fig. 7. Power efficiency performance of the prototyped adaptive and theoretical non-adaptive boosted and 5 V supplied charger schemes.

VI. Recommended IC Embodiment

To further improve efficiency performance, the voltage drop between the adaptive supply and battery in Eq. (8) must be reduced, and this can be done by eliminating sense resistor R_C, which is possible if the power PMOS itself were used to sense the charge current, as shown in Fig. 8, where the adaptive function has also been simplified. Mirroring PMOS M_{PS} and source-drain voltage equalizer A_{Mirror} ensure the voltage across R_S is linearly proportional to the charge current, just as R_C did in Figs. 2 and 5. The voltage drop across the adaptive supply and the battery can now be reduced to approximately 0.2 V.

The adaptive supply function is now performed by a voltage-current-voltage translation of the battery voltage. To generate an adaptive voltage equal to the sum of the battery and a constant voltage that is to be applied across the power PMOS device, the battery voltage is turned into a current (V_{Bat}/kR), mirrored by an Op-Amp and a MOS device, and applied to a matching resistor (kR), which rides on the constant reference voltage (V_{Const}) of switching regulator A_{SW}, thereby generating the desired adaptive supply (e.g., $V_{Adapt} = V_{Bat} + V_{Const}$). Consequently, the dropout voltage across power transistor M_P (equal to V_{Const}) is kept low and constant throughout the charging process. Since the output of the shunt-feedback switching regulator is low impedance and the current mirror is independent of the main charger's current and voltage feedback loops, the loop-gain response shown in Fig. 3 is preserved.

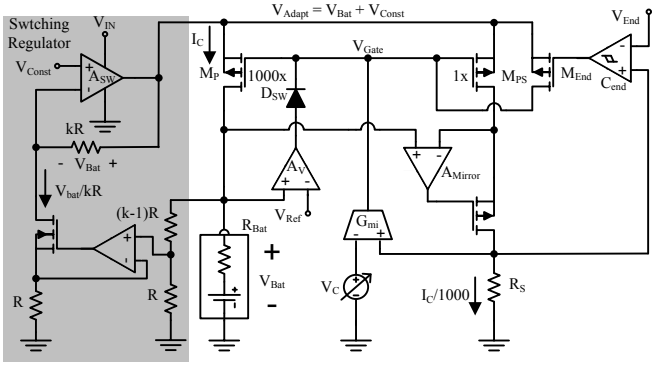

Fig. 8. Recommended IC embodiment of the proposed charging scheme.

The recommended IC embodiment was simulated using AMI's 0.5 µm technology models for MOSFETs; macro models for the Op Amps, transconductors, and the 90% efficient regulator; and a 720 F - 0.1 Ω series combination for an 800 mAh battery. With V_{Const} set to 200 mV, the efficiency of the mirror-sensing charger circuit outperformed the resistor-sensing circuit by 2.9%, as shown in Fig. 9, which constitutes the power lost in sense resistor R_C (Fig. 5).

VII. Conclusion

An accurate, continuous, and compact Li-Ion charger with a power efficient adaptive supply scheme has been presented and experimentally verified. The accuracy of the proposed constant current-voltage architecture ensures maximum Li-Ion capacity and cycle life. The circuit combines and continuously transitions a current- to a voltage-regulated feedback loop with a single diode, sharing a single power MOSFET. Cascading an adaptive switching converter to ensure the voltage drop across the power charge MOS device is low and constant and using a mirror to sense the charge current minimizes power losses and therefore achieves high power efficiency. In all, the proposed circuit optimally charges a Li-Ion battery with minimal power losses, mitigating the power-rating requirements of the power MOS device, increasing the life of bootstrapping laptop-to-cell phone charge cycles, and circumventing the need for bulky heat sinks, all of which incur costly tradeoffs in mobile electronics.

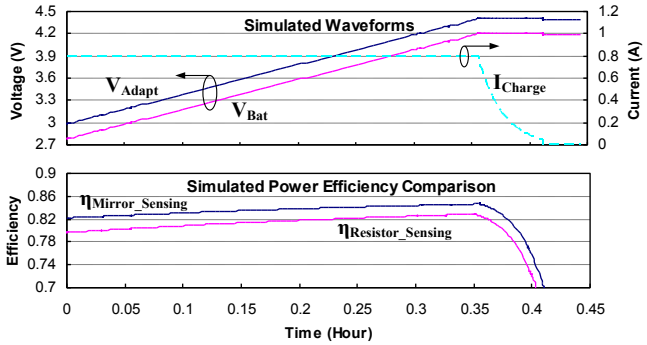

Fig. 9. Simulated charging response and efficiency performance of the recommended mirror-sensing charging circuit shown in Fig. 8.

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