Compact Fast-Waking Light/Heat-Harvesting 0.18-µm CMOS Switched-Inductor Charger

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***Abstract*—Although microsystems can nowadays consume microwatts, onboard batteries can be so small and leaky that sustaining microwatts for months or years without recharge cycles can be virtually impossible. Tiny photovoltaic cells and thermoelectric generators can help, but only when light or heat is available, and only to the extent that light intensity and thermal gradients allow. This is why energy-harvesting microsystems idle and shut down often and fast-wakeup provisions are important. The 0.18-µm CMOS charger proposed here is 8.31% more efficient during wakeup than the smallest reported and 7.69% more efficient than the next best, but without a 1:60 off-chip transformer and without vibration energy. Although 3.27% less efficient than the most efficient, the system here uses 3 fewer off-chip inductors. And after waking, the system is 5% to 46% more efficient than the others. The key innovations are low-power management and design. The system in essence charges a 200-pF capacitor with just enough energy to transfer two energy packets per cycle: one to charge a 1.8-µF battery and the other to replenish the 200 pF. This way, and with 100 nF across the source, the system charges a fully depleted 1.8-µF battery to 0.9 V in 45 ms and draws in steady state 98.8%–99.7% of available input power to deliver 76%–86% of the 40–150 µW drawn.**

***Index Terms*—Boost dc–dc converter, charger, harvester, heat, light, photovoltaic, starter, switched inductor, thermoelectric.**

I. Light- and Heat-Harvesting Microsensors

Wireless microsensors can add life-, energy-, and cost-saving intelligence to homes, hospitals, factories, biological systems, and other networked spaces and difficult-to-reach locations [1]–[6]. Although sensors, data converters, digital-signal processors (DSPs), and power amplifiers (PAs) can nowadays require 10 µW to 10 mW to operate [7], onboard batteries are very small, so lifetimes without recharge cycles can be impractically short. Fortunately, ambient energy E_A can replenish a battery, but only when available, and only to the extent that ambient conditions allow.

Batteries, however, are imperfect. Lithium ions, for example, store usable energy at 2.7–4.2 V, leak up to 10% per month, and survive 1k–2k recharge cycles [8]. Unfortunately, microsensors can be so small and so universally spread that they can only sustain up to 0.9–1.8 V, recharge 10–50 times per day, and operate 5–10 years for a total of 18k–182k cycles. Although super capacitors can leak 100% per month, they are popular in this research space because they operate at lower voltages and survive 100k–500k cycles [9]. But since leakage is high, designers often resort to conventional capacitors. In other words, batteries in this space are essentially capacitors.

An energy-harvesting charger like Fig. 1 shows should therefore be able to replenish its battery C_B with as much power as possible. A maximum power-point (MPP) tracker continually adjusts the charger for this purpose [10]. This way, C_B can receive and supply maximum power. Even though maximum input power $P_{IN(MPP)}$ is important, what matters most is maximum output power $P_{O(MPP)}$. This is why the MPP tracker senses the battery voltage v_B. But since v_B varies with incoming and outgoing charge, a power supply normally conditions and feeds power to system components [11]–[12].

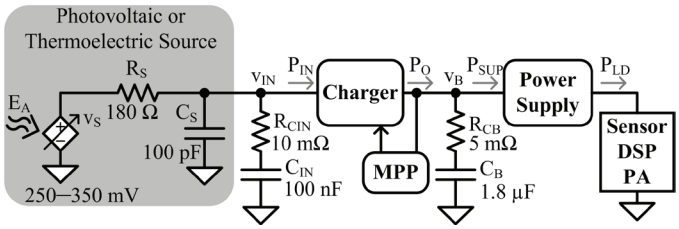

Fig. 1. Light- or heat-harvesting microsensor.

Of possible ambient sources, photovoltaic (PV) cells can at 100–400 µW/mm^2 generate over 100× higher power from sunlight than piezoelectric, electrostatic, and electromagnetic transducers, antennas, and thermoelectric generators (TEGs) can from motion, radiation, and heat [13]–[15]. Light, however, is not always available. Considering the computers or engines to which many microsensors attach, heat can at times be more available. Although the application ultimately dictates which ambient source is more accessible, light and heat are often available and therefore popular options [1].

Interestingly, one PV cell outputs more power than several cells in series that occupy the same area. This results because the space between cells does not collect charge and mismatched currents and parasitic PN junctions between cells leak charge [15]. A PV source can therefore establish a dc voltage that is as low as 300–500 mV. When stacked, thermoelectric piles generate even lower dc voltages [7]. This is why light- and heat-harvesting microsystems often share similar components, and why the ambient source voltage v_S in Fig. 1 is dc and only 250–350 mV.

Operating from such a low input voltage is challenging because, with low gate drive, transistors are resistive and therefore lossy. As a result, the charger can consume much of the power drawn, leaving little left for C_B and other blocks. In

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other words, C_B charges slowly, if at all, and the microsensor must wait for v_B to reach a headroom level that is high enough for system components to perform their prescribed tasks.

Waiting is a problem when ambient energy for short intervals because v_B might not climb high enough to power the sensor. Leakages can also drain C_B before the source returns. The charger should therefore replenish C_B quickly, and since space is so scarce in microsensors, with few off-chip devices.

C_B should be as high as possible to power microsensors continuously for extended periods. Except, higher capacitance requires more time to wake. So C_B should be *just* high enough when fully charged to the breakdown level to sustain the system for the length of time that the application requires.

This paper presents a CMOS charger that draws power from a light- or heat-harvesting source with only one input capacitor and one transfer inductor. The system charges a temporary on-chip 200-pF supply, and with it, charges an off-chip battery C_B from no-charge conditions. To understand how this shortens wake time, Sections II and III explain the operating principles and mechanics of the design. Section IV then details how the prototyped implementation performs across operating conditions and compares against the state of the art. Section V finishes with relevant conclusions.

II. Operating Principle

The fundamental reason why batteries charge slowly from no-charge conditions is low gate drive. The problem is, with low gate voltages, transistors are resistive and therefore lossy. So of the power drawn, little reaches the battery. And with microfarads or more to charge, battery voltage climbs slowly.

The guiding principles that drive the design here are: small capacitors charge quickly and transistors switch faster and with less power when supplied from higher voltages. So the basic aim of the system proposed is to charge a very small temporary supply C_T from which circuits can later draw power above the headroom level V_{HR} that transistors need to switch efficiently. This way, the charger can deliver 80%–90% of the drawn power [16], instead of the 0.1%–7% that a millivolt supply could have supplied [7], [17]–[25].

For this, the system should first charge a small on-chip supply capacitor C_T to a level that is high enough to feed the charger without dropping below V_{HR}. But to store as much energy as possible with the least capacitance, C_T should charge to the technology's breakdown level V_{BD}. Plus, at that level, capacitance should be sufficiently high to store the energy the charger requires to deliver at least two energy packets: one to the battery C_B and another to C_T.

Although the system is inefficient when first charging C_T with the harvesting input voltage v_{IN}, C_T is so low at 200 pF that the process can be short. Once at V_{BD}, which in this case is 1.8 V, the charger draws power from C_T to deliver one energy packet to C_B and another back to C_T so C_T can recharge back to V_{BD} for the next cycle. Since v_T (by design) remains above V_{HR} through this process, the charger can supply 80%–90% of the power drawn.

The system delivers energy packets to C_T and C_B this way, in alternating cycles, until C_B charges above V_{HR} to threshold level $V_{B(MIN)}$. Past that point, the controller connects C_T to C_B and uses them together to wake and supply the microsensor. So the charger is inefficient only when charging C_T to V_{BD} the first time. After that, as C_T supplies the charger and the charger charges C_B and replenishes C_T, and later when C_B supplies the charger, the charger can be 80%–90% efficient [16]. Delivering this much charge to C_B is how the system proposed reduces wake time after harvesting droughts.

The system, however, does not react until v_{IN} reaches $V_{ST(MIN)}$ (in Fig. 2). The controller then waits for the starter to charge C_T above the level $V_{T(MIN1)}$ that can operate the charger. Past that, the controller shuts the starter, and if v_T is below the threshold $V_{T(MIN2)}$ needed to deliver two energy packets, the charger delivers one packet to C_T. When v_T rises above $V_{T(MIN2)}$, the system starts charging C_B. But if v_B is below $V_{B(MIN)}$ and v_T below $V_{T(MIN2)}$, the system recharges C_T.

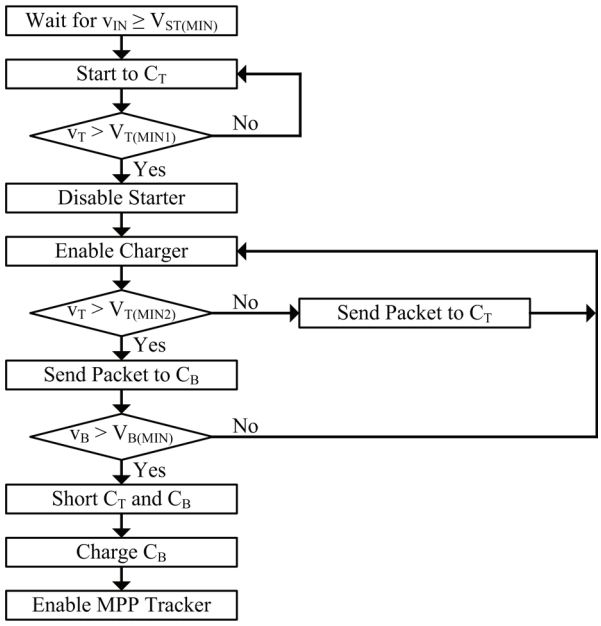


Fig. 2. Flow chart of the wakeup process proposed.

The maximum power-point (MPP) tracker draws power that C_T cannot sustain (by design). So once v_B reaches $V_{B(MIN)}$, the controller also enables the tracker. $V_{B(MIN)}$ therefore corresponds to the headroom level of the tracker. But since the tracker requires time to determine the MPP [26], the charger does not output maximum power until some time later. This is why the settling time of the tracker is also important.

III. Energy-Harvesting Charger

The energy-harvesting charger proposed in Fig. 3 energizes and drains inductor L_X from the harvesting input v_{IN} into either the small temporary supply C_T or the larger battery C_B. L_X, ground switch M_{GND}, and output diode D_B implement a boost dc–dc converter stage. When fully drained, the starter first charges C_T above the headroom level V_{HR} that transistors need to switch efficiently. Then, while supplied by C_T, the controller disables the starter and enables the oscillating pulse generator, which with the controller's v_{AID} commands ground switch M_{GND} and diode switch D_B to energize and drain L_X from v_{IN} into C_B and C_T in alternating cycles.

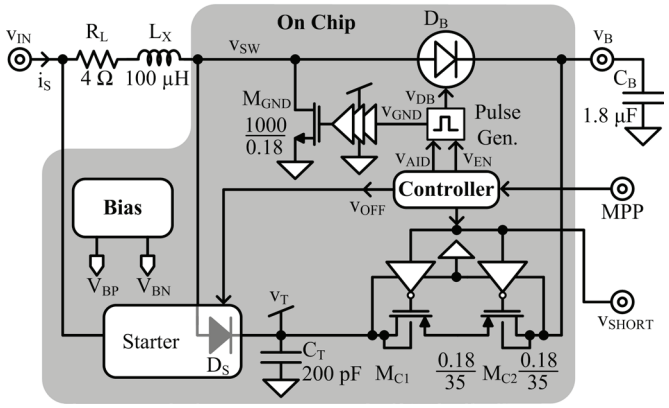


Fig. 3. Proposed 0.18-µm light- or heat-harvesting CMOS charger.

When C_B's voltage v_B is above minimum threshold $V_{B(MIN)}$, the controller's short signal v_{SHORT} closes M_{C1} and M_{C2}. That way, C_T and C_B short and together supply the charger. v_{SHORT}, which marks the end of wake period t_W, also enables the MPP tracker. Note the starter operates the charger when no other power source than v_S is available. Although inefficient with v_S's 250–350 mV, the starter is still functional, whereas with such a low voltage, the controller is not.

A. Controller

The purpose of the controller is to decide when to (*i*) disable the starter and enable the oscillating pulse generator, (*ii*) replenish the temporary supply C_T, and (*iii*) use the battery C_B to wake and supply the system. For this, the controller in Fig. 4 incorporates three threshold detectors: TD_{EN}, TD_{AID}, and TD_B. Since replenishing C_T presupposes v_T is high enough to operate circuits, the AND gate that TD_{AID}'s output drives does not engage until TD_{EN}'s output v_{EN} rises to indicate C_T is ready to supply. TD_B's AND gate similarly keeps TD_B and v_{SHORT} from shorting C_B to C_T until C_T is ready to replenish.

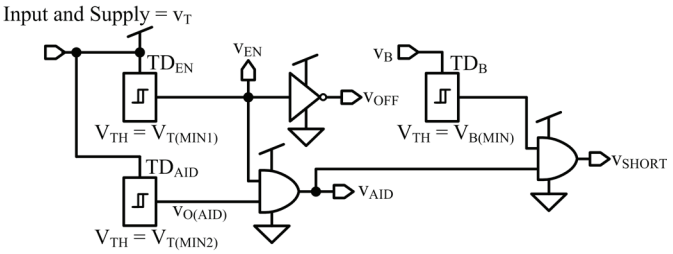
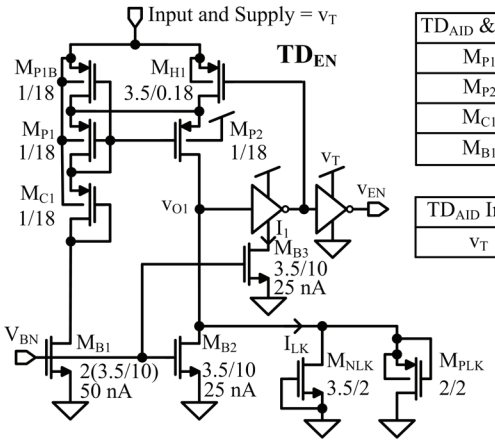


Fig. 4. Controller.

TD_{EN}, TD_{AID}, and TD_B are essentially headroom detectors because they trip when the supply is just high enough to activate a current source. When TD_{EN}'s supply voltage v_T in Fig. 5 is low, for example, M_{P1} and M_{C1}'s diode connections push M_{B1} into triode, reducing M_{B1}'s current below what V_{BN} would otherwise set. M_{B2}'s current therefore overwhelms M_{P2}'s mirrored reflection of M_{P1}–M_{B1}'s current to keep v_{O1} and v_{EN} low. When v_T is high enough to pull M_{B1} out of triode, M_{P2}'s current surpasses M_{B2}'s, so v_{O1} and v_{EN} rise. This way, TD_{EN} trips when v_T rises above M_{B1}, M_{C1}, and M_{P1}'s headroom level $V_{T(MIN1)}$, which here is 0.75 V, and from simulations, is 0.56–0.88 V across process and temperature.

To help, M_{NLK} and M_{PLK} leak I_{LK} to keep M_{P2}'s leakage from inadvertently tripping v_{O1}. M_{B3}'s I_1 limits the current and power that v_{O1}'s first inverter consumes as v_{O1} transitions. M_{H1} adds headroom to M_{B1} as v_{O1} rises to reinforce (with hysteresis) v_{O1}'s rising transition. The resulting hysteresis is (from simulations) 90–200 mV.



TD_{AID} & TD_B	W_{CH}/L_{CH}
M_{P1}	1/36
M_{P2}	1/36
M_{C1}	1/36
M_{B1}	2×3.5/36

TD_{AID} Input	TD_B Input
v_T	v_B

Fig. 5. Enable, aid, and battery threshold detectors TD_{EN}, TD_{AID}, and TD_B.

TD_{AID} operates the same way, except M_{C1}'s and M_{P1}'s longer channel lengths raise M_{B1}'s headroom level above that of M_{B1} in TD_{EN}. TD_{AID} therefore trips at a higher threshold level $V_{T(MIN2)}$ than TD_{EN}'s $V_{T(MIN1)}$. $V_{T(MIN2)}$, which here is 0.85 V, should be high enough above $V_{T(MIN1)}$'s 0.75 V to keep the system from discharging C_T below $V_{T(MIN1)}$. Although $V_{T(MIN2)}$'s simulated 0.68–1.09-V range overlaps $V_{T(MIN1)}$'s, M_{C1} and M_{P1}'s longer channel lengths ensure $V_{T(MIN2)}$ is always higher than $V_{T(MIN1)}$.

TD_{EN} disables the starter when C_T first charges to $V_{T(MIN1)}$, and with the battery diode D_B still off, the oscillating pulse generator, M_{GND}, and L_X can charge C_T after that. When TD_{AID} senses that v_T rises above $V_{T(MIN2)}$, v_{AID} prompts the oscillating pulse generator to enable D_B, and that way, steer L_X's energy into C_B. After supplying the charger across one or two cycles, C_T discharges below $V_{T(MIN2)}$, but not below $V_{T(MIN1)}$, because before that happens, TD_{AID} again disables D_B and allows the diode inside the starter D_S to replenish C_T with L_X's energy.

TD_B is a replica of TD_{AID}, except TD_B senses C_B's voltage v_B. So when v_B rises above $V_{B(MIN)}$, which with this circuit is $V_{T(MIN2)}$, the system shorts C_B to C_T, and this way, uses C_B to supply the charger. So even after transactions discharge C_B below $V_{B(MIN)}$, $V_{B(MIN)}$ is high enough above the headroom level V_{HR} and transaction losses are low enough fractions of the energy delivered that v_B does not fall below V_{HR}.

B. Oscillating Pulse Generator

The purpose of the oscillating pulse generator in Fig. 6 is to close (on-command) M_{GND} long enough to energize L_X with sufficient energy to replenish the temporary supply C_T, and when C_T is full, to draw and deliver energy from the ambient source v_S to the battery C_B. Once enabled by the controller's TD_{EN} (which trips when v_T rises above threshold $V_{T(MIN1)}$), the current that the gate voltage reference V_{BP} from the bias block establishes with M_{B1} charges C_1. When C_1 charges above the gate–source voltage that M_2 requires to sustain M_{B2}'s bias current, M_2 overwhelms M_{B2} to flip the SR latch, reset C_1 to ground, and allow M_{B3} to similarly charge C_3. C_3 therefore charges until M_4 overwhelms M_{B4} to reset the flip-flop and re-

start the process. C_1 and C_3 continue charging and resetting this way in alternating cycles to oscillate v_{OSC} at a frequency that M_{B1}, C_1, M_2, M_{B2}, M_{B3}, C_3, M_4, and M_{B4} set to 10.5 kHz. Note that, unlike a current-starved ring oscillator, this frequency is supply insensitive.

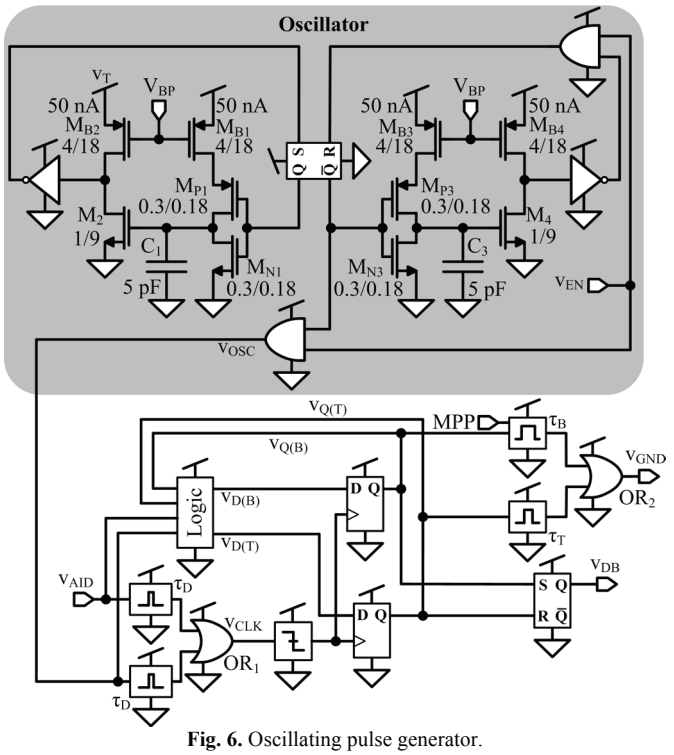


Fig. 6. Oscillating pulse generator.

The logic that v_{OSC} drives in Fig. 6 chooses the pulse length across which L_X energizes. Unless interrupted by v_{AID}, this logic (in Fig. 7) chooses the pulse τ_B that corresponds to charging C_B. C_T is so much lower than C_B, however, that τ_B would over-energize L_X, and with L_X, overcharge C_T. So when v_{AID} indicates L_X should replenish C_T, the logic chooses the pulse τ_T that is long enough (by design) to replenish C_T in one cycle. This is why v_{GND} in Fig. 8 energizes L_X across a shorter pulse τ_T when v_{AID} rises.

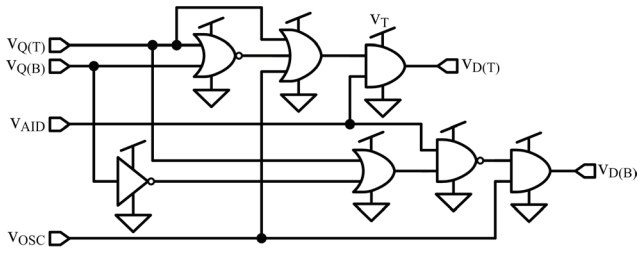


Fig. 7. Logic in the oscillating pulse generator.

So every time v_{OSC} rises, v_{GND} commands M_{GND} to start another energizing event. But since C_T can discharge below TD_{AID}'s $V_{T(MIN2)}$ while charging C_B, v_{CLK} in the logic keeps v_{DB} from changing D_B's state and v_{GND} from starting a pulse in the middle of a delivery. In other words, the logic does not generate overlapping pulsing commands.

Four instances of the one-shot pulse generator in Fig. 9 produce the energizing and filter-delay pulses τ_B, τ_T, and τ_D in Fig. 6. When the input v_I is low, the AND gate grounds the output v_O, M_{OFF} opens, and M_S grounds M_A's gate, so M_B's current keeps v_X high. When the input v_I rises, the AND gate raises v_O (in Fig. 10), M_S opens, and M_{OFF} closes to let I_P charge C_P. When C_P's voltage v_P is high enough for M_A to overwhelm M_B's current, v_X falls, and with it, v_O. In other words, v_O is high only as long as I_P requires to charge C_P above M_A's threshold. These pulse widths are 0.25–1 µs when I_P is 25–100 nA with about ±35% variation across process, voltage, and temperature corners.

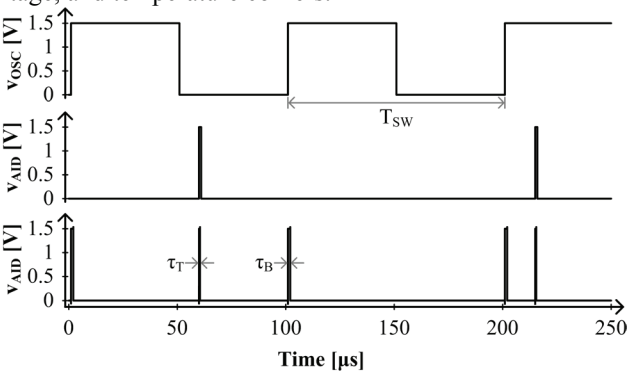


Fig. 8. Simulated timing diagram of the oscillating pulse generator.

I_P	Pulse	Time	W_P/L_P
25 nA	τ_B	1 µs	2/18
50 nA	τ_T	0.5 µs	4/18
100 nA	τ_D	0.25 µs	8/18

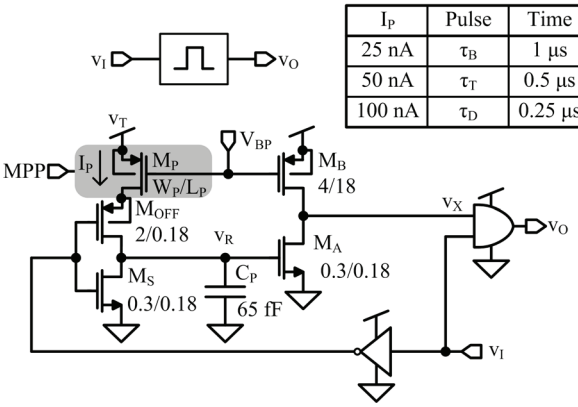


Fig. 9. One-shot pulse.

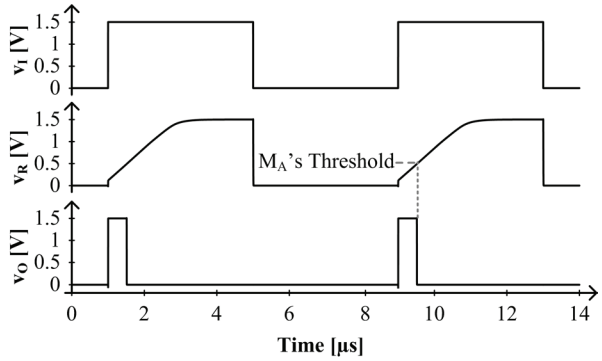


Fig. 10. Simulated timing diagram of the one-shot pulse.

Since v_B is not high enough to power the maximum power-point (MPP) tracker when first waking, τ_B starts at a pre-determined nominal setting. Once C_B charges to $V_{B(MIN)}$, the system should enable the tracker. So after the wake period t_W, the tracker adjusts τ_B to ensure L_X energizes long enough to draw and deliver maximum output power.

C. Battery Diode

Battery diode D_B in Fig. 3 is not an ordinary PN-junction diode for two reasons. For one, D_B should not direct energy to the battery C_B when the temporary supply C_T needs charge

and v_B is lower than v_T, which would otherwise engage a conventional diode. The second reason is that a diode would drop 0.6–0.7 V, which would burn substantially more power than a MOS implementation.

Unfortunately, D_B cannot be a typical MOSFET either because the system would not be able to block its body diode, which is necessary when steering energy into C_T. This is why back-to-back FETs M_{DB1} and M_{DB2} in Fig. 11 implement D_B. Because with their bulks tied, their body diodes block each other so no current flows when the FETs are off. The tradeoff for this functionality is power and maybe silicon area. Because for a given resistance, area and capacitance are higher, which means gate-drive power is also higher. Resistance is similarly higher when constrained to fit a particular area.

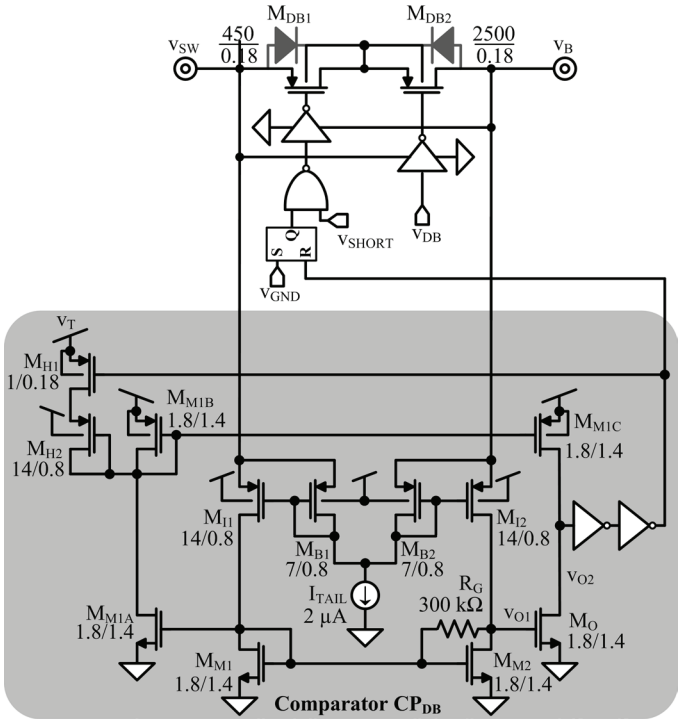


Fig. 11. Battery diode D_B.

M_{DB1} and M_{DB2} should together operate like a diode when enabled by v_{DB}. So v_{DB} closes M_{DB2} and allows the comparator CP_{DB} to switch M_{DB1} like a diode when v_{GND} opens M_{GND}. When CP_{DB}'s switching node v_{SW} rises above v_B, CP_{DB}'s v_{O2} rises to close M_{DB1}, and that way, connect v_{SW} to v_B like a diode, but with only millivolts across it. M_{I1} and M_{I2}, and as a result, their mirroring translations to v_{O1} and v_{O2} source equivalent currents when v_{SW} equals v_B. When v_{SW} rises above v_B, M_{I1}'s translation M_{M2} sinks more current than M_{I2} sources, so v_{O1} falls, M_O weakens, and M_{M1C} raises v_{O2} to close M_{DB1}.

For all this, M_{B1} and M_{B2} split I_{TAIL}'s 2 µA (from the bias block) to establish the currents that M_{I1} and M_{I2} and their translations conduct. M_{M1C} sources a mirrored reflection of M_{I1}'s current, so when M_{I1} conducts more current, M_{M1C}'s translation raises v_{O2} faster. And as v_{O2} falls, M_{H1} closes to decrease M_{M1C}'s mirror gain to v_{O2}. This hysteresis allows M_O to ground v_{O2} faster.

For fast turn-on transitions, R_G limits M_O's gate swing Δv_{O1}. When v_{SW} is below v_B, M_{B1} is off, so M_{B2} conducts I_{TAIL}. M_{B2}'s translation M_{I2} therefore feeds $2I_{TAIL}$ into R_G, M_{M1}, and M_{M2}. But since M_{M2} mirrors M_{M1}, $2I_{TAIL}$ splits between R_G and M_{M2}. v_{O1} therefore peaks to $I_{TAIL}R_G$ above the gate–source that M_{M1} requires to sustain I_{TAIL}, which combined is roughly 800 mV. During transitions, R_G also reduces the parallel resistance at v_{O1}, which lowers the gain, but not enough to be a problem.

When disabled by v_{DB}, M_{DB2}'s driver connects M_{DB2}'s gate to v_{SW}. Although M_{DB2} can still close when v_B is greater than v_{SW}, CP_{DB} commands M_{DB1}'s driver to connect M_{DB1}'s gate to v_B when v_B is above v_{SW} to ensure M_{DB1} stays off. So combined, M_{DB1} and M_{DB2} are off when v_{DB} is low. Otherwise, when v_{DB} is high, M_{DB1} closes only when CP_{DB} resets the SR latch, which happens just after v_{SW} rises above v_B.

D. Starter

The goal of the starter in Fig. 12 from [17] is to use the inductor L_X to charge the temporary supply C_T once after the ambient source first recovers from a long drought. As the input v_{IN} first rises, M_{SEN} energizes L_X and the jump starter and M_R help transfer and exchange the energy drawn between L_X and switching-node capacitance C_{SW}. Although the energy swapped is not at first high enough for M_{DS1} and M_{DS2} to steer charge into C_T, the energy grows, and with it, so does v_{SW}'s peak as it oscillates. Once v_{SW} is high enough above ground, M_{DS1} and M_{DS2} close to steer L_X's leftover energy into C_T.

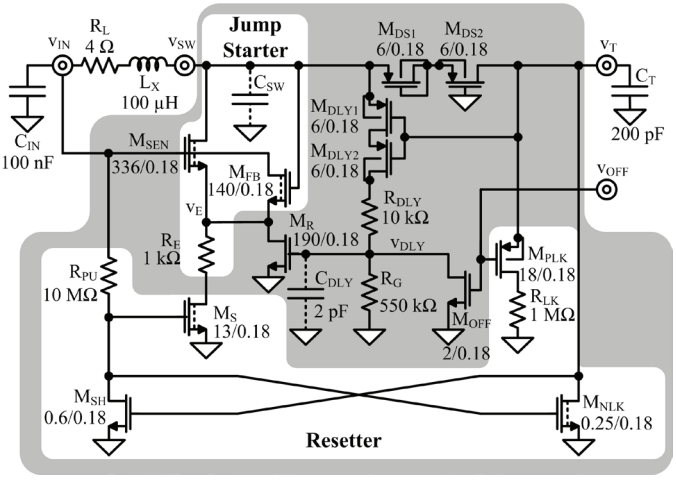


Fig. 12. Starter.

But if v_T does not climb sufficiently high for the controller to shut the starter, M_{SH} resets the jump starter. And to help M_{DS1} and M_{DS2} engage the next time v_{SW} is high, M_{PLK} leaks C_T. Since C_T does not altogether deplete, v_T reaches the first threshold level $V_{T(MIN1)}$ the next time C_T receives energy. This prompts the controller's TD_{EN} to shut the starter and enable the oscillating pulse generator.

To charge C_T from the lowest v_{IN} possible, L_X should transfer as much energy as possible. This is why L_X is high. But since microsensors cannot accommodate large inductors, L_X cannot occupy much space. So when constrained to mm's, increasing the number of turns is only possible when thinning the coil. This means, small inductors with high inductances are resistive [27]. Since raising inductance reduces current, and in consequence, ohmic power, the optimal inductor incorporates an L_X and R_L that balance energy transferred with energy lost.

E. Bias

The bias block in Fig. 13 establishes the reference gate voltages V_{BN} and V_{BP} for N- and P-channel MOS transistors that all circuits use to establish bias currents. For this, M_1 and M_2 sink equal currents because M_3–M_{3C} mirrors M_4–M_{4C}'s current. And since M_2's channel width is eight times wider than M_1's, M_2's gate–source voltage v_{GS2} is lower than M_1's v_{GS1} and the difference $v_{GS1} - v_{GS2}$ appears across R_B. In subthreshold, this difference is proportional to absolute temperature (PTAT) [28], so $v_{GS1} - v_{GS2}$ across R_B establishes a PTAT current. Although not implemented here for the sake of low power, adding a complementary-to-absolute-temperature (CTAT) component to the circuit can reduce the drift of the bias currents that V_{BN} and V_{BP} produce.

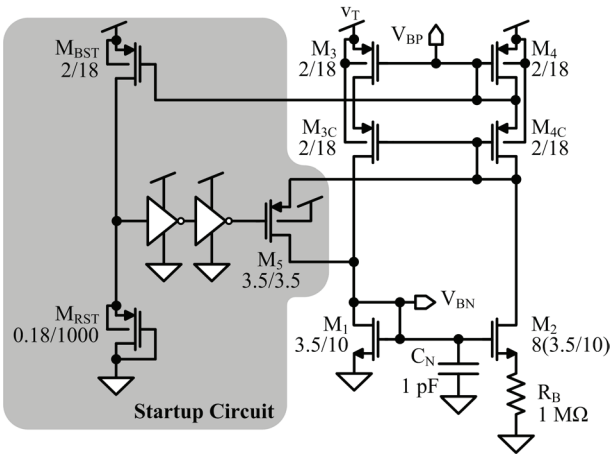


Fig. 13. Bias block.

The purpose of M_5, whose current is much lower than those of M_1–M_4, is to keep the circuit from entering the off state. To this end, M_{BST} mirrors M_4's current into a long-channel diode-connected PMOS M_{RST} that behaves like a high-value resistor. So if M_4's current is too low, the inverters close M_5 to pull and feed current from M_4 into M_1, and that way, push the circuit back into the on state. Here, C_N keeps noise from fluctuating V_{BN} to the extent that the startup circuit activates.

IV. Measured Performance

The prototyped 0.18-µm CMOS die in Fig. 14 integrates everything in Fig. 3, except the 70-mV/°C heat-harvesting source v_S, the 100-nF input capacitor C_{IN}, the 100-µH transfer inductor L_X, and the 1.8-µF battery C_B, which are off chip on the board shown. The die and board also include replica and monitoring circuits used to isolate and test different parts of the system. To discern the roles of v_S and R_S in the 3.3 × 2.5-mm^2 thermoelectric generator (TEG) in [29], a power supply establishes v_S and an off-chip resistor sets R_S. The die, packaged die, C_{IN}, L_X, and C_B measure 660 × 370 µm^2, 9.7 × 6.4 × 1.2 mm^3, 1.6 × 0.8 × 0.8 mm^3, 2 × 1.25 × 1.45 mm^3, and 2 × 1.25 × 1.25 mm^3. C_{IN}, L_X, C_B, and v_S's series resistances are 10 mΩ, 4 Ω, 5 mΩ, and from [29], 180 Ω.

A. Wakeup Charge Sequence

Off: Across a prolonged harvesting drought, leakages drain all capacitances in the circuit, so nothing works. As ambient energy E_A returns, the ambient source v_S climbs, but as long as v_S remains below the starter's minimum threshold $V_{ST(MIN)}$, which in this case in Fig. 15 is 220 mV, the system is off. So up to about 9.5 ms, the source resistance R_S drops zero volts and the harvesting input v_{IN} follows the ambient source v_S.

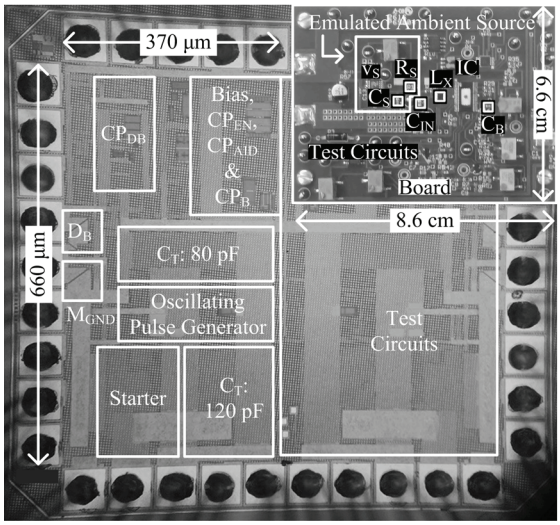


Fig. 14. Die and board photographs of the prototyped charger.

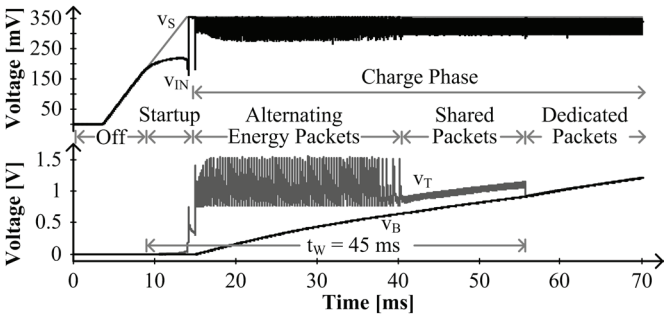


Fig. 15. Measured wakeup charge sequence.

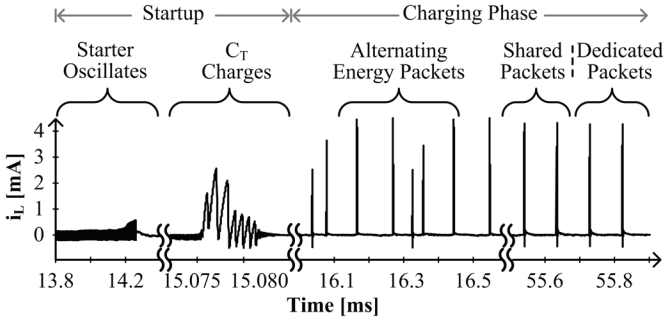


Fig. 16. Measured inductor current across wakeup phases.

Startup Phase: As v_S reaches 220 mV at 9.5 ms, the starter begins to energize L_X and help L_X drain into the switching-node capacitance C_{SW}. L_X and C_{SW} then exchange energy and continue to oscillate this way after that. Except, L_X's energy and current at 13.8–14.2 ms in Fig. 16 is not enough to raise v_{SW} above C_T's voltage v_T for the starter's D_S to steer energy into C_T. So although the starter draws harvested input power from v_{IN}, which is why R_S drops voltage and v_{IN} falls below v_S between 10 and 14 ms in Fig. 15, v_T remains near zero.

At 14.5 ms, however, L_X draws enough energy to charge C_{SW} and steer leftover charge into C_T. And although this energy is not enough to charge C_T above the first threshold $V_{T(MIN1)}$, L_X's energy on the next cycle at 15.1 ms in Figs. 15–16 is. So v_T in Fig. 15 climbs above $V_{T(MIN1)}$'s 0.75 V at about

15.1 ms. TD_{EN} in the controller senses this, and in response, shuts the starter and enables the oscillating pulse generator. This marks the end of the startup phase.

Charge Phase: Once shut, the starter no longer loads v_{IN}. So at 15.1 ms in Fig. 15, R_S conducts so little current that v_{IN} climbs close to v_S. With v_T now above $V_{T(MIN1)}$, the controller together with the oscillating pulse generator close and open M_{GND} to energize and drain L_X into C_T through the starter's D_S (with the rest of the starter off). This transaction charges C_T to the chip's breakdown level V_{BD}, which in this case is 1.8 V.

Now that v_T is greater than TD_{AID}'s threshold level $V_{T(MIN2)}$, the controller enables the battery diode D_B. So after M_{GND} energizes L_X again, D_B drains L_X into the battery C_B to begin charging C_B. This transaction, however, drains C_T below $V_{T(MIN2)}$, but not below $V_{T(MIN1)}$. The controller therefore disables D_B to let D_S drain L_X into C_T, and in so doing, replenish C_T. The charger *alternates* energy packets to C_B and C_T this way between 15 and 40 ms. With v_T at or above $V_{T(MIN1)}$, the system can draw from a lower input voltage $V_{IN(MIN)}$: 35 mV. So even if v_S drops to 35 mV in this charge phase, the charging process continues.

When v_B is within 300 mV of v_T's upper threshold level $V_{T(MIN2)}$ (at about 40 ms in Fig. 15), D_S begins leaking some of the energy meant for C_B into C_T. This leaked energy keeps C_T from discharging below $V_{T(MIN2)}$, so the controller stops steering energy packets directly into C_T. Or more to the point, TD_{AID} stops disabling the battery diode D_B. v_T is higher than v_B, however, because C_T is much lower than C_B, so v_T rises faster with less energy. C_B and C_T *share* energy packets this way until v_B reaches TD_B's threshold $V_{B(MIN)}$ at 55.7 ms. Past that point, v_B is high enough to supply the system, so the controller connects C_B to v_T. *Dedicated* energy packets charge C_B more than energy transactions load C_B through this last phase, so v_B climbs steadily with every switching cycle.

To deliver energy packets, the system energizes and drains L_X in alternating phases, which corresponds to i_L rising and falling in Figs. 16–17. After depleting L_X, however, the parasitic capacitance C_{SW} at the switching node v_{SW} still holds charge. So C_{SW} and L_X exchange this remnant energy until parasitic resistances burn it. This is why i_L in Figs. 16–17 reverses and rings after each packet. Although this energy never reaches C_T or C_B, C_{SW} is low, so little is lost.

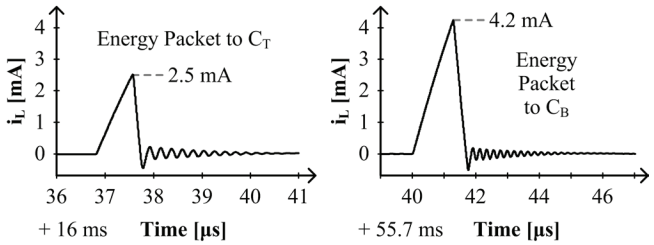


Fig. 17. Measured inductor current when delivering energy to C_T and C_B.

v_{IN} in Fig. 15 does not drop much below v_S across the startup phase and the alternating and shared packet sequences of the charging phase because v_B is not high enough to supply the maximum power-point (MPP) tracker. After v_B surpasses $V_{B(MIN)}$ (as L_X delivers dedicated packets), TD_B's output can enable the tracker. But like in [7], [18]–[19], [24]–[25], and [30]–[32], the system here excludes the MPP tracker because MPP is not possible during wake time tin_W. This is why MPP effects are absent even after v_B surpasses $V_{B(MIN)}$.

B. Harvesting Efficiency

For the battery to charge quickly in steady state, L_X should draw maximum power. The MPP tracker would do this by adjusting τ_B in the controller, which sets L_X's energizing period. But since the system excludes the tracker, τ_B is adjustable off chip and Fig. 18 shows measured MPP information when manually adjusted.

But as drawn source current i_S climbs, the source resistance R_S burns more power. And while power P_S drawn from the source v_S rises linearly with i_S, R_S's ohmic power $P_{R(S)}$ climbs quadratically. This means, increasing losses in $P_{R(S)}$ offset gains in P_S and harvested input power P_{IN} maxes when the extra loss $\Delta P_{R(S)}$ just cancels the additional gain ΔP_S. So as i_S in Fig. 18 increases and i_S into R_S reduces input voltage v_{IN}, P_S at 0 mA and 350 mV rises more linearly than $P_{R(S)}$ does quadratically, which is why P_{IN} climbs past that point. After 972 µA, $P_{R(S)}$ outpaces P_S, so at 972 µA, P_{IN} maxes at 170 µW and falls after that. Since P_S rises with v_S, $P_{R(S)}$ can be higher before P_{IN} peaks (with a higher v_S). P_{IN}'s maximum power point (MPP) $P_{IN(MPP)}$ therefore rises with v_S.

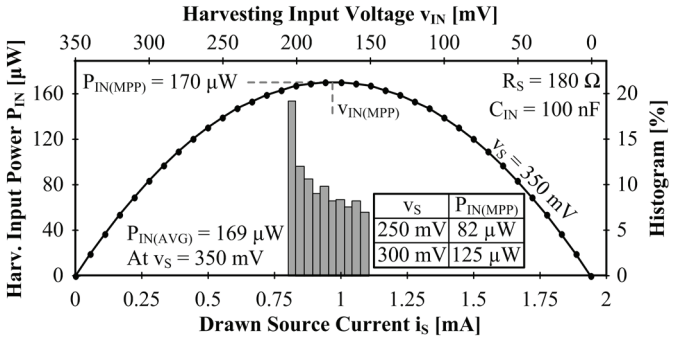


Fig. 18. Harvested input power and histogram measured in steady state.

Since L_X's current i_L peaks higher (to 4 mA) than the 972 µA that v_S can (on average) source at its MPP, source and input capacitors C_S and C_{IN} supply the difference. But any time i_L is less than 972 µA, v_S supplies more charge than L_X draws and the excess recharges C_S and C_{IN}. So across a switching cycle, C_S and C_{IN} supply as much charge as they receive.

Unfortunately, the ripple voltage that results at the harvesting input v_{IN} shifts the source from its MPP setting $v_{IN(MPP)}$. With 100 nF of input capacitance C_{IN}, v_{IN} ripples between 158 and 210 mV, like the measured histogram for v_{IN} in Fig. 18 shows. This variation, however, is close enough to $v_{IN(MPP)}$'s 175 mV to average 169 µW or 99.4% of the 170 µW that the input source v_S can deliver at 350 mV. With so little variation in P_{IN}, the charger's output power P_O is similarly insensitive to C_{IN} when C_{IN} is 100 nF or higher.

Average input power $P_{IN(AVG)}$ is so close to $P_{IN(MPP)}$ that improvements from higher input capacitances are hardly noticeable in Fig. 19. Lower input capacitances, on the other hand, increase the ripple to such an extent that the effects are apparent in both P_{IN} and P_O. With 10 nF, for example, v_{IN} ripples 280 mV, so maximum input power P_{IN} averages 120 µW (from instantaneous v_{IN} and i_{IN} data measured) or 70.6% of the 170 µW that v_S can deliver. P_{IN} averages less at 22 µW with 1 nF, but not much less below that level because board, source, and probe capacitance plateau at about 1 nF. In other words, input capacitance C_{IN} becomes a negligible fraction of

the total capacitance present at the input v_{IN}. This is why v_{IN} does not ripple more than 350 mV when C_{IN} is less than 1 nF.

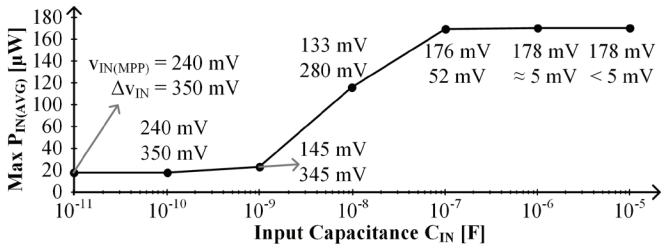


Fig. 19. Measured maximum input power and input ripple across C_{IN}.

C. Charging Efficiency

The source voltage v_S supplies the most power when the charger presents a load R_C that is equivalent to the source resistance R_S. When loaded this way, $0.5v_S$ appears across R_C's R_S and R_C receives maximum input power $P_{IN(MPP)}$ or $(0.5v_S)^2/R_S$. In the case of the source emulated from [29], v_S and R_S are 350 mV and 180 Ω, so $P_{IN(MPP)}$ is 170 µW.

Unfortunately, quiescent, gate-drive, and ohmic power in the charger $P_{Q(C)}$, $P_{G(C)}$, and $P_{R(C)}$ leak power. Wake efficiency η_W is the fraction of $P_{IN(MPP)}$ delivered $P_{O(W)}$ when waking. Here, like Fig. 15 shows, the system charges a fully depleted 1.8-µF battery C_B to the target $V_{B(MIN)}$'s 0.9 V across a 45-ms wake period t_W. Since C_B receives energy E_C or $0.5C_BV_{B(MIN)}^2$ in t_W, $P_{O(W)}$ is E_C/t_W or 16.2 µW and wake efficiency η_W is 9.53%.

Efficiency after that depends on static conversion efficiency η_C and the maximum power-point (MPP) tracker. Of the losses just mentioned, only $P_{R(C)}$ climbs with current. So as P_{IN} and P_O increase with v_{IN}, $P_{R(C)}$ in Fig. 20 rises (and $P_{G(C)}$ and $P_{Q(C)}$ do not). But since P_{IN} consistently rises more than $P_{R(C)}$ when v_{IN} is below 175 mV, the charger draws 55–168 µW or 98.2%–98.8% of the 56–170 µW that R_C can receive when v_{IN} is 100–175 mV and delivers 40–150 µW or 76%–86% of the drawn 55–168 µW. Past 175 mV, efficiency continues to rise with v_{IN} until $P_{R(C)}$'s added losses cancel P_{IN}'s gain, which in this case can happen near 200 mV. Past that, η_C drops.

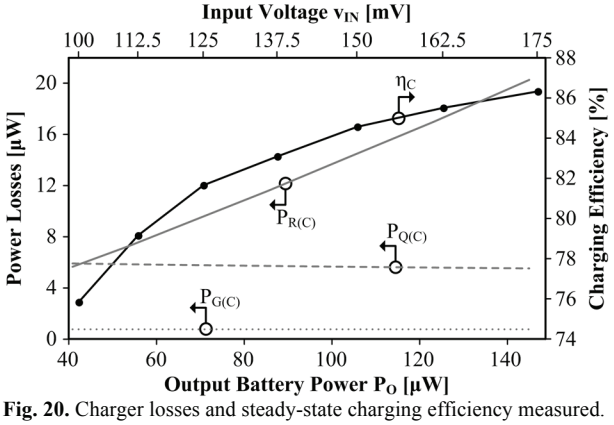


Fig. 20. Charger losses and steady-state charging efficiency measured.

When enabled, the starter burns the most power because, with only v_{IN}'s 100–175 mV, efficiency is 1%–7% [17]. But since the starter only operates when the system wakes, steady-state power is only the 1.86 µW that the starter leaks when disabled. The pulse generator consumes more power at 3.01 µW because, once enabled, it never stops switching.

The inductor's 4-Ω series resistance R_L consumes more power $P_{R(RL)}$ in Fig. 21 than those of the battery diode D_B and ground switch M_{GND}. Although a larger inductor with the same inductance can incorporate less resistance, longer dimensions counter the integration benefits of a smaller board component. D_B burns more power than M_{GND}'s resistance R_{GND} because D_B's resistance R_{DB} is, by design, close to 10 Ω. With a lower resistance, the voltage that L_X's 0–4 mA would drop across R_{DB} would not be sufficiently high to drive CP_{DB} quickly. With 10 Ω, however, R_{DB} does not consume more power than R_L because D_B conducts a fraction of the time that L_X does. M_{GND}'s resistance is considerably lower because, without R_{DB}'s limitation, M_{GND}'s channel width is wide enough to balance ohmic and gate-drive losses, at which point M_{GND} requires the least power possible to switch across states.

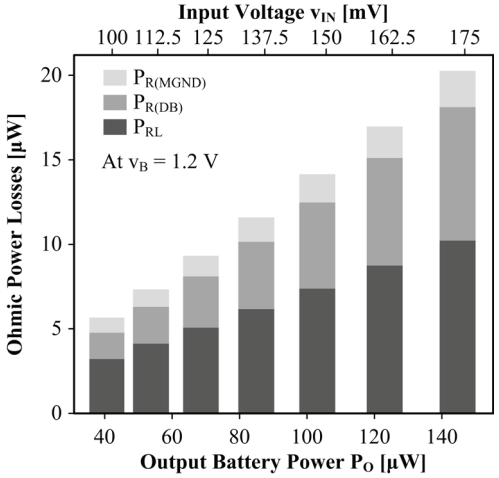


Fig. 21. Simulated ohmic power losses.

When the input v_{IN} is 150 mV, R_L, R_{DB}, and R_{GND} in Table I burn 7.40, 5.06, and 1.13 µW. Since R_{DB} is not low enough to balance gate-drive power, the gates of D_B's M_{DB1} and M_{DB2} require (at 100 nW) much less power to switch than R_{DB} consumes. M_{GND}'s gates, however, require about as much as R_{GND} dissipates. At 160 nW, D_B's comparator CP_{DB} requires a little more than what D_B requires to switch. With three threshold detectors to sustain, the controller burns more average power at 330 nW. The bias block consumes 60 nW.

TABLE I: SIMULATED POWER LOSSES.

With a 150-mV Input v_{IN}		Power Loss
Controller		330 nW
Pulse Generator		3.01 µW
CP_{DB}		160 nW
Starter		1.86 µW
Bias		60 nW
R_L		7.40 µW
D_B	R_{DB}	5.06 µW
	Gate Capacitance	100 nW
M_{GND}	R_{GND}	1.13 µW
	Gate Capacitance	650 nW
Total		**19.73 µW**

D. The State of the Art

Important parameters to consider when designing the charger of a microsensor are wake output power $P_{O(W)}$, steady-state output power $P_{O(S)}$, and size. Since the input v_{IN} is too low to operate the maximum power-point (MPP) tracker when waking with a tiny thermoelectric or solar source, systems do not engage the tracker until the wake period t_W ends [18] and

TABLE II: COMPARISON WITH THE STATE OF THE ART.

	[7]	[18]	[19]	[24]	[25]	[30]	[33]	This Work
Process Technology	0.35 µm	0.13 µm	65 nm	65 nm	–	65 nm	0.18 µm	0.18 µm
Off-Chip Components	22 µH 22 µH MEMS Switch	1:60 Trans- former	2 µH 2 µH 100 µH 27 µH	6.8 µH	One Inductor	None	None	100 µH
Minimum Startup Voltage $V_{ST(MIN)}$	35 mV	40 mV	50 mV	80 mV	330 mV	85 mV	350 mV	220 mV
Minimum Input Voltage $V_{IN(MIN)}$	25 mV	40 mV	30 mV	50 mV			250 mV	35 mV
Source Voltage v_S	50 mV	40 mV	50 mV	80 mV	1 V	120 mV	550 mV	350 mV
Source Resistance R_S	5 Ω	5 Ω	6.2 Ω		1 kΩ		10 Ω	180 Ω
Maximum Input Power Possible $P_{IN(MPP)}$ [B]	125 µW + P_{VIB} [A]	80 µW	100 µW		250 µW		7.60 mW	170 µW
Equivalent Battery Capacitance C_B	100 nF	10 µF	1 µF	10 nF		10 pF	1 F	1.8 µF
Battery's Target Charge Voltage $V_{B(MIN)}$	2 V	1.2 V	0.8 V	1.3 V	1.8 V	1.2 V	2 V	0.9 V
Wake Time t_W	11 ms + t_{VIB} [A]	4.9 s	25 ms	4.8 ms	1.2 s	8 µs	360 min	45 ms
Equivalent Wake Output Power $P_{O(W)}$ [C]	18.2 µW	1.47 µW	12.8 µW				92.6 µW	16.2 µW
Wake Efficiency η_W [D]		1.84%	12.8%				1.22%	9.53%
Peak Static Conversion Efficiency $\eta_{C(PK)}$ [E]	58%	40%	73%	72%	80%		81%	86%
MPP Tracker	No	Yes	No	No	Yes	No	Yes	No

[A]Requires vibration power P_{VIB} and time t_{VIB} for vibrations to begin. [B]$P_{IN(MPP)} = (0.5v_S)^2/R_S$. [C]$P_{O(W)} = 0.5C_B V_{B(MIN)}^2/t_W$. [D]$\eta_W = P_{O(W)}/P_{IN(MPP)}$. [E]$\eta_C = P_{O(S)}/P_{IN}$.

[25]. And even then, the tracker requires time to settle [26]. t_W is therefore the time the system requires to operate the tracker.

So $P_{O(W)}$ depends on source voltage and resistance v_S and R_S and losses. Wake efficiency η_W is a normalizing parameter that comprehends v_S, R_S, and losses. Although [19] in Table II is 3.27% more efficient in this respect, [19] uses three more microhenry inductors. Even with a 1:60 off-chip transformer, [18] is 7.69% less efficient. [33] requires less than [19] and [18], but η_W is 8.31% lower and minimum start and steady-state voltages $V_{ST(MIN)}$ and $V_{IN(MIN)}$ are 1.6× and 7.1× higher. [24] and [25] have similar requirements, but without reporting R_S in [24] and C_B in [25], they are not comparable. [7] uses one more microhenry inductor and a MEMS transistor that requires vibration power P_{VIB} to operate and additional wake time t_{VIB} for vibrations to begin. P_{VIB} is additional input power that the system unfortunately does not recover.

$P_{O(S)}$ depends on v_S, R_S, losses, and the MPP tracker. Although static efficiency η_S can account for all these, decoupling the tracker from the source and losses isolates the efficacy of the charger. This is why Table II reports static *conversion* efficiency η_C: the fraction of *actual* drawn power P_{IN} (not $P_{IN(MPP)}$) that the charger outputs with $P_{O(S)}$. In this respect, while peak efficiency $\eta_{C(PK)}$ in [18] and [7] is low at 40%–58%, [24] and [19] is moderate at 72%–73%, and [25] and [33] is high at 80%–81%, $\eta_{C(PK)}$ here is higher at 86%.

Like [7], [19], [24], and [30], the system here excludes the MPP tracker that, like [18], [25], and [33], they should all ultimate include. Although [32] includes a wake function, the system works when the battery voltage is greater than 2.9 V, which is compatible with lithium ions, but not the capacitor batteries that researchers envision microsensors might use. [31] charges a battery, but from an input that an RF source sets, not a thermoelectric or photovoltaic source.

The advantage of the transformer in [18], MEMS switch in [7], multiple inductors in [19], and ring oscillators in [23]–[24] is that they start from a lower input voltage $V_{ST(MIN)}$. Replacing the starter in Fig. 3 with the ring oscillators that [23]–[24] use can reduce the startup voltage of this system to the 80 mV they report. But still, to deliver 9.53% of the highest possible input power when waking, the system must retain the controller, switching network, oscillating pulse generator, small temporary supply, and operating principles proposed and presented here. And while [16] only theorized what was possible, the prototype designed and presented here proved it with circuits and measurements.

V. CONCLUSIONS

With 100 nF and 100 µH, the 0.18-µm CMOS charger prototyped delivers 9.53% of the maximum input power possible to wake and charge a fully depleted 1.8-µF battery to 0.9 V in 45 ms. This is 8.31% more efficient than the smallest reported and 7.69% more efficient than the next best, but without a 1:60 off-chip transformer. Although 3.27% less efficient than the most efficient, the system uses three fewer off-chip inductors. After waking, the charger draws 98.8%–99.7% of the power supplied by a 200–350-mV source to deliver 76%–86% of the 40–150 µW drawn, which is 5% to 46% more efficient than the state of the art. Like others, the system excludes a maximum power-point tracker that, although ineffectual during wakeup, is essential in steady state. Still, wake efficiency is critical because tiny batteries exhaust easily and frequently, and clouds, debris, and other factors interrupt the harvesting action of small photovoltaic and thermoelectric generators. With this charger, wireless microsensors can wake more quickly and function more often.

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