

A Programmable 210 μV Offset Rail-to-Rail G_M -C Filter

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Abstract— Low input-referred offset performance and linearity in analog filters are critical design parameters, yet transistor mismatch limitations are a severe hindrance. Programmability is also a feature of growing significance because high performance state-of-the-art systems must adapt on-the-fly to various operating conditions, as is the case in battery-operated electronics where systems traverse through idle, alert, and high performance modes in an effort to conserve energy and extend battery life. This paper presents a continuous and programmable first-order G_M -C filter with sub-milli-Volt offset performance. Low offset is achieved by auto-zeroing and continuity by ping-ponging between two transconductors, all under the construct of a compact and bandwidth-efficient circuit topology. The proposed G_M -C circuit was fabricated with AMI's 0.5- μm CMOS process technology and achieved an input-referred offset of less than 210 μV , hand-over glitches of less than 40 mV, and 57 dB of linearity over the rail-to-rail input span for a lithium-ion battery supply range of 3 to 4.2 V. The bandwidth and gain of the filter were programmable from 1.1 to 6.5 kHz and 1.27 to 29.1 V/V, respectively, both with better than 3.2% resolution.

Index Terms— G_M -C filter, programmable, low offset, auto-zero, ping pong, linearity, rail-to-rail, current sensing.

I. INTRODUCTION

Low-offset performance in analog filters can be as important as their frequency filtering properties, as is the case in analog sensors like temperature and capacitive sensing applications [1-2] and instrumentation amplifiers [3-10], where both the DC and ac portions of the signal carry important information. When sub-milli-Volt input-referred offsets are required, increasing the dimensions of critically matched CMOS transistors is often impractical, if not insufficient, because of their inherent offsets and implied bandwidth tradeoffs (i.e., larger devices achieve better matching performance but in the process introduce larger parasitic capacitors), which is why dynamic offset cancellation is so popular. And given the analog nature and accuracy requirements of many applications, these dynamic solutions must also be continuous, that is, capable of filtering the signal linearly with time. Unfortunately, dynamic (i.e., switching) schemes necessarily introduce undesired transient glitches to the system. A few milli-Volts glitch at the input of a high-speed high-resolution comparator, for instance, may inadvertently trigger unexpected transitions and therefore degrade the noise and jitter performance of the overall system.

Tuning the gain and bandwidth of analog filters is also increasingly important in a wide range of applications, from

receiver radio-frequency (RF) filters, where the filter's bandwidth must match the frequency of the received signal to discern the desired signal from noise, to switching power supply circuits, where a filter is tuned to accurately sense the inductor and therefore the output current. State-of-the-art current-sensing filters for switching supply circuits, in fact, are discrete and cumbersome to program (gain and bandwidth parameters are tuned manually with off-chip resistors and capacitors) [11-12]. An on-chip programmable and continuous low offset G_M -C integrated circuit (IC) that meets the accuracy and low glitch requirements of a current-sensing filter for switching power supply applications, particularly a step-down DC-DC converter, as shown in Fig. 1, is therefore proposed [11].

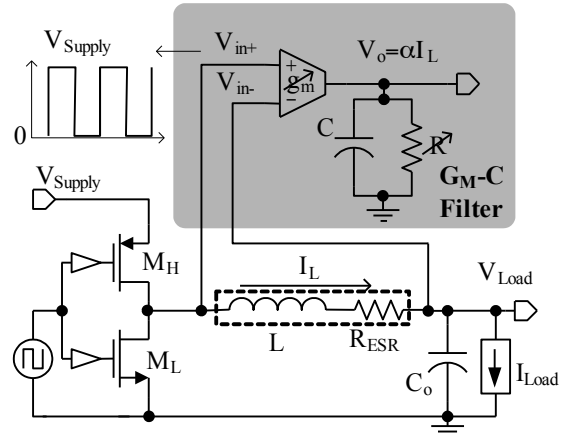


Fig. 1. Programmable and continuous low offset G_M -C filter for current sensing in switching supply applications.

The filter is comprised of programmable, auto-zeroed, ping-ponged transconductor G_M ; adjustable resistor R ; and bandwidth-setting capacitor C . The voltage across inductor L and its equivalent series resistor (ESR) is an indicator of the output current (current flowing through L), but its value is low because ESR is typically only a few milli-Ohms, which is why low offset performance is required. The bandwidth of the G_M -C filter is “tuned” (“programmed”) to match the process-dependent cut-off frequency of the L-ESR path, thereby canceling the frequency dependence of the measured output (V_o) and ascertaining both DC and ac current information [12-13]. While this cut-off frequency is only a few kilo-Hertz, a single pole response must exist and extend through several decades of frequency, requiring all parasitic poles and zeros to reside well above the frequency range of the system, which can easily exceed 10 MHz. Linearity is also critical for

accuracy over the entire input voltage range, which includes both supply rails because the non-inverting input of the filter traverses from ground to input supply V_{Supply} .

A continuous and tunable first-order G_M -C filter with sub-milli-Volt offset performance is presented and experimentally validated in this paper. A review of dynamic offset cancellation techniques within the context of continuous low offset operation is offered in Section II. Section III introduces and discusses the proposed G_M -C filter and Section IV details the particulars of the circuit. Experimental results are then presented in Section V and conclusions drawn in Section VI.

II. OFFSET-CANCELLATION TECHNIQUES

Real transistors, in spite of being fabricated with the same process, near one another, surrounded by similar devices, and in the same orientation, suffer from threshold-, mobility-, and geometry-induced mismatch effects, the end result of which is undesired DC offsets in analog circuit applications [3]. In CMOS process technologies, for instance, threshold voltage and mobility mismatches of supposedly identical devices are inversely proportional to active area, which is why larger devices are normally selected in low offset applications. However, when sub-milli-Volt input-referred offsets are required, such as in precision analog sensor applications, increasing the dimensions of critically matched CMOS components is not practical and dynamic offset-cancellation circuit techniques become necessary [3].

State-of-the-art dynamic offset-cancellation circuits generally fall in one of two categories: auto-zero (AZ) and chopper [3-10]. Auto-zeroing is performed in two phases, the sampling phase where the offset is measured and the processing phase when the offset is subtracted (cancelled) and the input signal is processed. The chopper, on the other hand, periodically switches the polarity of the offset at relatively high frequencies and therefore, on the average, cancels the DC offset of the circuit. In practical terms, a modulator and a demodulator (both at the same chopping frequency) are placed at the front and back ends of a high offset amplifier and a low pass filter at the output. As a result, the input is modulated to high frequencies, but not the DC offset of the amplifier, so that when the output of the amplifier is demodulated back to broadband frequencies, the DC offset is modulated to high frequencies, beyond the pass-band of the low pass filter, canceling in the process the effects of DC offsets.

Although both chopper and auto-zero schemes cancel DC offsets, their time-domain and frequency responses differ. Chopper schemes, for instance, are continuous in time, unlike auto-zeroed amplifiers where information is processed only at discrete times. The signal bandwidth of an auto-zeroed amplifier, on the other hand, is not necessarily limited by auto-zeroing but by the amplifier itself, whereas the signal bandwidth of a chopper amplifier is constrained to half the chopping frequency to prevent the offset from aliasing back into the signal bandwidth during the demodulation phase. What is more, the chopping frequency is limited to several kilo-Hertz because its offset-canceling features are mitigated by clock feed-through and coupling-induced offsets [3]. As a

result, since the input of the filter in current-sensing applications for switching supply circuits can pulse up to a few mega-Hertz and the sensing bandwidth must therefore exceed it by at least a decade, auto-zeroing is preferred. Table 1 summarizes and compares these features.

Table 1. Summary of dynamic offset cancellation techniques.

Chopper	Auto Zero
Modulates and filters DC offset	Samples and subtracts offset
Continuous	Discontinuous
Higher noise reduction	Lower noise reduction
Low Bandwidth ($BW < 0.5f_{\text{Chop}}$)	High Bandwidth

Continuity in auto-zeroed amplifiers can be achieved by adopting ping-pong and/or feed-forward architectures [3], although both at the cost of complexity, area, and power. In the former, while one amplifier is sensing and measuring its offset, another is processing the signal [6-8]. The operation is then reversed to allow the amplifier that was previously processing the signal to now sense and measure its offset. In practice, noise in the form of transient spikes (glitches) is introduced at the output when the output is disconnected from one amplifier and connected to the other. In feed-forward implementations [9-10, 14-15], an error amplifier is designed and dedicated to continually cancel and compensate the offset of the processing amplifier, thereby avoiding the switching that occurs in the ping-pong strategy. The offset-nulling amplifier is itself auto-zeroed and its output, which tunes the main amplifier, is sampled and held across a capacitor. Feed-forward unfortunately suffers from intermodulation effects between the auto-zero clock frequency and the input signal [14-15], which results in signal distortion. The main disadvantage of this technique, however, within the context of general G_M -C filters, is lack of versatility because negative feedback around the processing amplifier is necessary to continually supply a sample of the offset across its input terminals without changing its connectivity, which is why ping pong is often times preferred. Table 2 summarizes and compares ping-pong and feed-forward strategies.

Table 2. Summary of continuous-time auto-zero techniques.

Ping Pong	Feed Forward
Higher glitch content	Lower glitch content
Used in open- and closed-loop amplifiers	Only used in closed-loop, negative feedback amplifiers
No intermodulation effects	Intermodulation effects

III. PROPOSED LOW OFFSET G_M -C FILTER

The proposed continuous low offset G_M -C filter, as illustrated in Fig. 2, is comprised of two well-matched, auto-zeroed, ping-ponging dual-input summing transconductors (i.e., G_{M1} and G_{M2}); two offset-programming capacitors for each transconductor (i.e., C_{h1-} , C_{h1+} , C_{h2-} , and C_{h2+}); a single bandwidth-setting capacitor C ; gain setting resistor R ; and non-overlapping clock signals ϕ and ϕ_n . The non-overlapping feature is implemented to prevent various cross-wiring events. Input voltage V_{ref} , against which filter output voltage V_o is referenced, is used as a virtual ground (ac ground). Finally, as in all ping-pong schemes, while one transconductor processes

the input signal, the other one auto-zeroes.

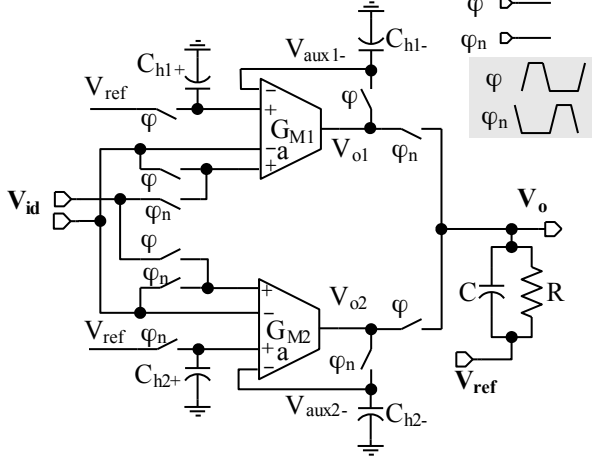


Fig. 2. Proposed ping-pong G_M -C filter with two auto-zeroing summing transconductors.

The difference in the proposed scheme is that a summing comparator is used to program and cancel the offset by dedicating an input differential pair to the input signal and another to subtract (i.e., cancel) the offset. The key advantage to this configuration is that the large holding capacitor is decoupled from the high bandwidth path, that is, not connected to the input ac-signal path and therefore not bandwidth-limiting the signal. A large holding capacitor is desirable because it reduces clock feed-through and charge injection, consequently improving offset cancellation performance [3], all without adversely affecting bandwidth.

A. Offset Cancellation

The Norton equivalent circuit of the summing transconductor, as shown in Fig. 3(a), is composed of two voltage-dependent current sources $V_{id}g_m$ and $V_{ida}g_{ma}$, where g_m is the main input-to-output and g_{ma} is the auxiliary input-to-output transconductances, V_{id} is the differential voltage applied to the main input, and V_{ida} is the differential voltage applied to the auxiliary input. The equivalent circuit also includes output resistance R_o and voltage source $V_{Unloaded}$, which is the unloaded (i.e., open-circuit) output voltage of an ideal (i.e., perfectly matched) transconductance G_M cell when its input pairs are short-circuited.

In the programming phase (Fig. 3(b)), the main input pair is short-circuited and the auxiliary pair connected in unity-gain configuration, forcing its output to superimpose the overall offset of the transconductor on programming capacitor C_h :

$$V_{aux-} \approx \frac{[(V_{ref} + V_{os2})g_{ma} + V_{osl}g_m]R_o}{1 + g_{ma}R_o} \approx V_{ref} + V_{os2} + V_{osl} \frac{g_m}{g_{ma}}, \quad (1)$$

where V_h is the voltage across holding capacitor C_h , V_{os1} and V_{os2} are the offsets of the main and auxiliary ports, and $g_{ma}R_o$ is the loop gain, which is designed to be much higher than one (i.e., R_o is large). In ping-ponging the circuit to the processing phase, the stored offset is subtracted from the input by breaking the unity-gain feedback loop, allowing the stored offset voltage to remain across the auxiliary input pair, and

connecting the input signal across the main input pair (Fig. 3(c)),

$$\begin{aligned} V_o &= ((V_{id} + V_{osl})g_m + (V_{ref} + V_{os2} + V_{inj} - V_{aux-})g_{ma})(R_o \parallel R) \\ &= \left[(V_{id} + V_{osl})g_m + (V_{ref} + V_{os2} + V_{inj})g_{ma} - \left(V_{ref} + V_{os2} + V_{osl} \frac{g_m}{g_{ma}} \right)g_{ma} \right] (R_o \parallel R) \\ &\approx (V_{id}g_m)(R_o \parallel R) + (V_{inj}g_{ma})(R_o \parallel R) \\ &= \left(V_{id} + V_{inj} \left(\frac{g_{ma}}{g_m} \right) \right) g_m (R_o \parallel R) \end{aligned}, \quad (2)$$

where V_{inj} is the clock feed-through and charge injection voltage effects of offset storage switches S_1 and S_2 . Left-ver V_{inj} errors are reduced by designing g_{ma}/g_m to be small.

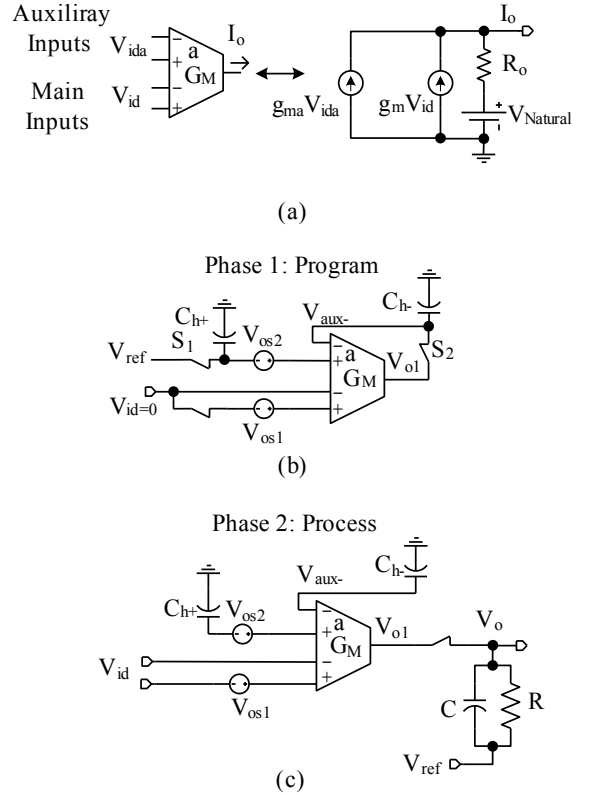


Fig. 3. Summing transconductor's (a) Norton-equivalent model and respective (b) offset programming and (c) signal processing phases.

The matching accuracy of the foregoing circuit, as with all dynamic offset-cancellation techniques, is limited by feed-through and charge injection V_{inj} , which can be reduced (i.e., shunted), but not eliminated, by employing differential hold capacitors and switches [3] and increasing the size of holding capacitors C_{h+} and C_{h-} . The remaining input-referred offset of the main pair is

$$\begin{aligned} V_{res-in} &\approx \left(\frac{g_{ma}}{g_m} \right) V_{inj} + \left(\frac{1}{g_m R_o g_{ma} R_o} \right) (V_{ref} - V_{Unloaded}) \\ &\quad + \left(\frac{1}{g_{ma} R_o} \right) V_{os1} + \left(\frac{1}{g_m R_o} \right) V_{os2} \end{aligned}, \quad (3)$$

where $V_{Unloaded}$ is not necessarily equal to V_{ref} . $V_{Unloaded}$ is in

fact dependent on circuit topology and supply and input common-mode voltage through supply- and common-mode rejection ratios CMRR and PSRR. As a result, because of finite values of CMRR and PSRR, remaining offset V_{res_in} varies slightly with changes in supply and common-mode input voltages, even after the $V_{Unloaded}$ error term is substantially attenuated by $g_m R_o g_{ma} R_o$.

B. Output Transient Glitches

When the output is ping-ponged from one summing transconductor to the other, transient glitches occur because their respective output voltages are not necessarily equal; in other words, their outputs are uncorrelated during a switching handover event. To study the transitional glitches, a transition from when first transconductor G_{M1} is in the signal path to the state where second transconductor G_{M2} is in the signal path is illustrated in Fig. 4. Before the transition (Fig. 4(a)), G_M -C filter output voltage V_o is equal to G_{M1} output voltage V_{o1} and, after the ping-pong transition (Fig. 4(b)), the G_M -C filter output follows G_{M2} output voltage V_{o2} . Before the transition, V_{o1} is a function of transconductance, bandwidth (i.e., settling behavior), and input voltage (i.e., $V_{o1} = V_{id} \cdot \text{Gain}$) whereas V_{o2} is independent of input voltage and close to the reference voltage (V_{ref}) used in the programming phase of the offset cancellation sequence, assuming initial offset values are in milli-Volts and much smaller than V_{ref} . As a result, at the transition, V_{o2} is not related to the input signal and may therefore be off from its desired target value when connected to the signal path.

Just after G_{M2} is connected in the signal path, the output capacitor charge redistributes and sets the output voltage to somewhere between V_{o1} and V_{o2} , causing an instantaneous error of ΔV_{glitch} (Fig. 4(c)). After the transition, the circuit corrects the systematic handover glitch disturbance, that is, the output voltage converges to its target value, at a rate determined by the circuit's bandwidth, which is in turn a function of R , C , and the parasitic switch-on resistances and capacitances present at the output and the transconductor's output impedance. These impedances can be lumped and modeled by a single equivalent low frequency pole ($1/R_{Eq}C_{Eq}$), the transient response of which induces a momentary error voltage just past the switching transition point:

$$V_{Error} = \Delta V_{Glitch} e^{-\left(\frac{t}{R_{Eq}C_{Eq}}\right)} u(t), \quad (4)$$

where ΔV_{glitch} is the instantaneous glitch.

The value of ΔV_{Glitch} can be quantified by investigating the charge redistribution during the ping-pong transition time. Just before the transition, V_o is equal to V_{o1} , which is a function of the input voltage (i.e., $V_o = V_{o1} = \{V_{in+} - V_{in-}\} \cdot \text{Gain}$) whereas V_{o2} , which is at this point disconnected from the output, is close to V_{ref} (i.e., G_{M2} 's output parasitic capacitor C_{p2} is charged to V_{ref}), assuming its initial milli-Volt offset voltage is much smaller than V_{ref} , which is on the order of Volts. During a handover event, output capacitor C and resistor R are first disconnected from V_{o1} and G_{M2} 's negative auxiliary input disconnected from V_{o2} , and then, C and R are connected to

V_{o2} ; in other words, C_{p2} and C are connected together. Charge is therefore redistributed across these two capacitors, keeping the total charge equal before and after the transition:

$$C(V_o - V_{ref}) + C_{p2}(V_{ref}) = C(V_o - V_{ref} + \Delta V_{glitch}) + C_{p2}(V_o + \Delta V_{glitch}). \quad (5)$$

As a result, the instantaneous output voltage glitch is

$$\Delta V_{glitch} = \left(\frac{C_{p2}}{C + C_{p2}} \right) (V_{ref} - V_o). \quad (6)$$

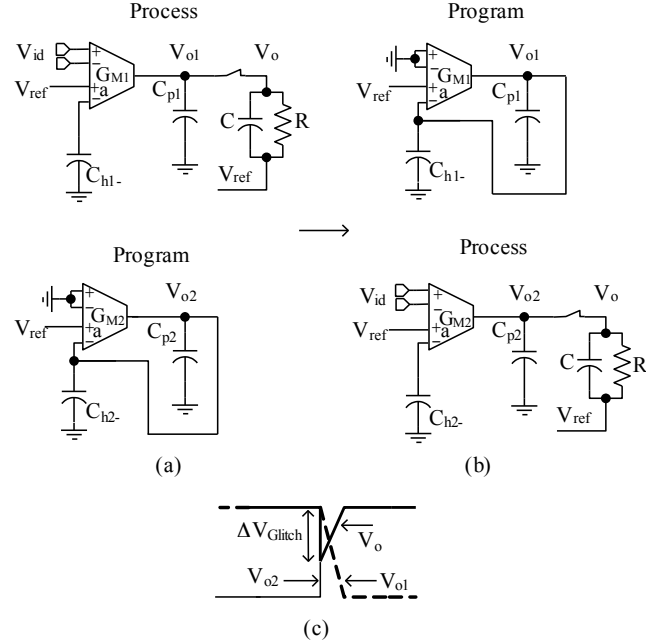


Fig. 4. Glitch performance: (a) G_{M1} in signal path, (b) G_{M2} in signal path, and (c) transient response.

Since output capacitor C is much larger than parasitic capacitor C_{p2} , output glitches are relatively small. For a 60 pF filter capacitor and a 1.33 pF parasitic capacitor combination, for instance, and 0.8 V worst-case difference between V_{ref} and V_o ($V_o = V_{id} \cdot \text{Gain}$), the glitches are theoretically limited to 17 mV. Most of these glitches could be considerably reduced if a more complex set of clocking signals were to be generated that would allow the auto-zeroed comparator to settle to its processed value before connecting it to the output, but the increase in complexity is not desirable in the foregoing application. Switch-on parasitic resistances and gate-drain and -source capacitances further degrade the response with clock feed-through and charge-injection noise, but their effects are overwhelmed by the handover glitches. Similarly, random 1/f, shot, and thermal noise is also overwhelmed by these systematic glitches, especially since auto-zeroing cancels the low frequency components of the random noise and the G_M cell's low filter bandwidth, which is on the order of a few kHz, filters out the higher frequency portion [3].

IV. CIRCUIT DESIGN

A. Programmable Transconductance

In the switching supply circuit shown in Fig. 1, the G_M -C filter must be programmable and highly linear across the rail-to-rail input voltage range. Since the non-inverting input swings from the positive to the negative supply every period, a variation in transconductance (Δg_m) in these two states translates to a systematic input-referred offset error voltage (V_{os_gm}),

$$V_{os_gm} = \frac{\Delta V_o}{g_m R} = \frac{\Delta g_m R}{g_m R} V_{id} = \left(\frac{\Delta g_m}{g_m} \right) V_{id}, \quad (7)$$

where V_{id} is the differential voltage applied to the transconductor. As a result, because polysilicon resistors are many times more linear than transistors and the non-inverting input of the transconductor is connected to a low impedance node (i.e., connected to a source capable of supplying current), a wide input voltage range resistor-dependent current conveyor [16-18], as shown in Fig. 5, can be used in place of a traditional differential pair transconductor. The input terminals of amplifier A_{int} are virtually short-circuited because of negative feedback and the resulting current flowing through series resistor R_1 (I_{R1}) is therefore proportional to the differential input voltage applied to the G_M -C cell (V_{id}),

$$I_{R1} = \frac{V_{id}}{R_1}. \quad (8)$$

This current is then mirrored to the output by current mirror M_1 - M_2 , ultimately defining the transconductance to

$$g_m \equiv \frac{I_o}{V_{id}} = \frac{1}{V_{id}} \left(\frac{V_{id} K}{R_1} \right) = \frac{K}{R_1}, \quad (9)$$

where K is a digitally programmable current-mirror gain. To add the auxiliary pair needed for the auto-zero feature illustrated in Figs. 2 and 3, a separate and more traditional transconductor is connected directly to the output (g_{ma}).

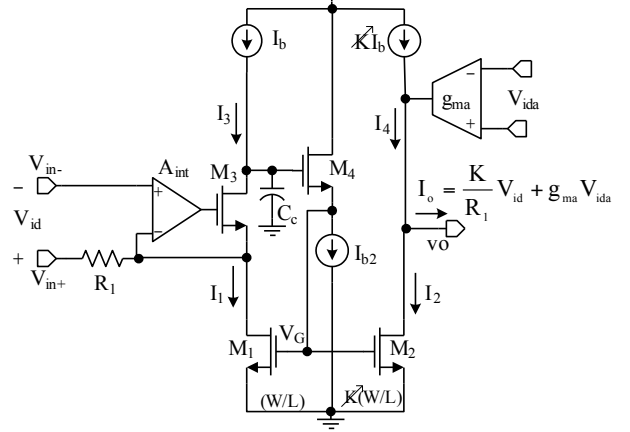


Fig. 5. Linear, dual-input, rail-to-rail transconductance cell (K is tunable).

To ensure M_3 is operating in the saturation region (i.e., ensure the shunt-feedback loop is properly biased), bias current I_b is fed into M_3 and the feedback loop around M_1 , M_3 , and M_4 (I_{b2} biases M_4) forces the gate voltage of M_1 to the exact value necessary to sink I_b and I_{R1} , which is another way of saying M_1 , M_3 , and M_4 comprise a current mirror where the drain and gate voltages of M_1 are decoupled. Additionally, having a constant bias current flowing through M_1 also allows the circuit to process both positive- and negative-flowing I_{R1} currents, that is, process bidirectional currents. Since the current conveyor circuit is highly linear, the overall linearity

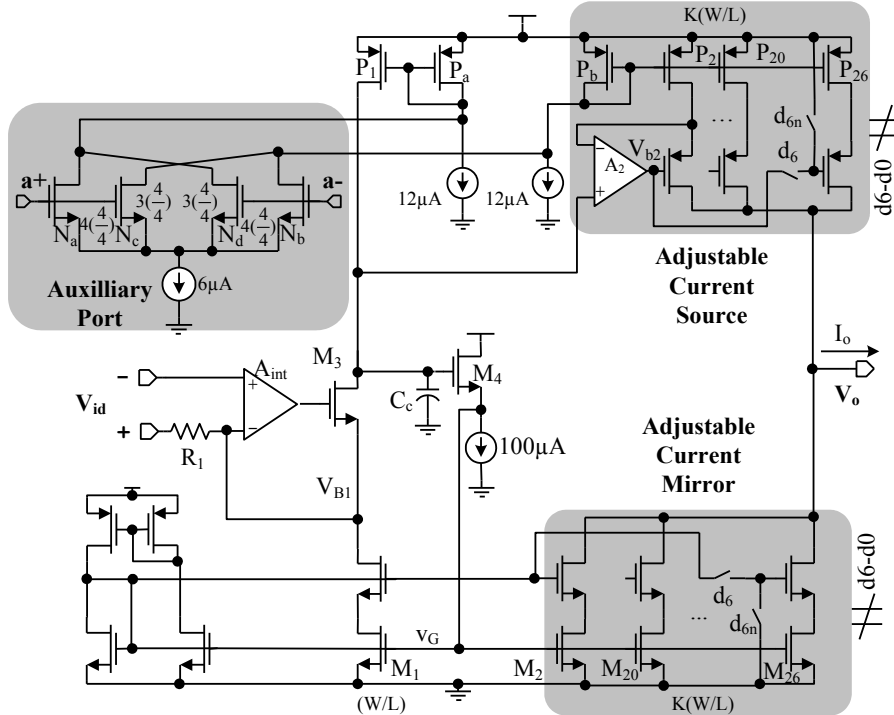


Fig. 6. Full schematic of the G_M cell.

of the circuit is dependent on the mirror, which is why bias current I_b is designed to be significantly higher than I_{R1} (noise and quiescent power are sacrificed for this). Because this current is amplified by the programmable-gain mirror, an equally amplified current is fed to the output of the mirror to ensure I_o is free of any bias current.

The gate of M_4 is high impedance and is therefore the gain- and bandwidth-setting node of the current-mirror's controlling feedback loop. Compensation capacitor C_c ensures the bandwidth-setting pole is at sufficiently low frequencies to prevent parasitic high frequency poles from compromising stability. The unity-gain frequency of this loop, however, adds a parasitic high frequency pole to the signal-flowing path (V_{id} to I_o) approximately at its gain-bandwidth product (g_{m1}/C_c), and C_c is therefore selected to balance stability against high bandwidth. Amplifier A_{int} is a standard two-stage PMOS input, Miller-compensated amplifier [19] with a gain-bandwidth product of 10 MHz.

The programmable K-gain current mirror implemented with M_1 - M_2 and its slave current source KI_b are shown in Fig. 6, where a digital word determines the connectivity of the binarily weighted array of current mirrors. Cascoding devices are added to the current mirrors and sources to increase their respective output impedances and consequently increase the transconductor's overall output impedance. For functional and therefore power and real-estate efficiency, the bias current generator and the auxiliary transconductor are combined into a single circuit via transistor current-mirror pairs P_a - P_1 and P_b - P_2 , where amplifier A_2 equates the drain voltages of P_1 and P_2 to minimize channel-length modulation errors and at the same time properly set the biasing voltage of the gates of the upper cascoding devices. The auxiliary pair consists of current-canceling differential pairs N_a - N_b and N_c - N_d , whose net result is a low transconductance value (g_{ma_d}) [19] that is then multiplied by current gain K with P_b - P_{2x} mirror:

$$g_{ma} = Kg_{ma_d} \quad (10)$$

The g_{ma_d} was designed to be roughly equal to $1/R_1$ (i.e., $4 \mu A/V$).

The variation of the circuit's transconductance across the input common-mode range (ICMR) is mostly dependent on the gain of the M_1 - M_2 current mirror in Fig. 5 and how it varies with current density, which only occurs if there is a mismatch in threshold voltages [17],

$$\frac{I_2}{I_1} = K \frac{(V_{GS} - V_{TH2})^2}{(V_{GS} - V_{TH1})^2}, \quad (11)$$

where M_1 and M_2 are assumed to be in saturation and V_{GS} is the gate-source voltage of M_1 and M_2 , V_{TH1} and V_{TH2} their respective threshold voltages, and K their area ratio. If there is no threshold mismatch, the current gain is K and independent of currents I_1 and I_2 ; otherwise, the gain is dependent on V_{GS} , which is in turn a function of I_1 :

$$V_{GS} = \sqrt{\frac{2I_1}{k'(W/L)}} + V_{TH1}, \quad (12)$$

where k' is the transconductance parameter and (W/L) the

aspect ratio of M_1 . Consequently, since the current flowing through M_1 changes with input V_{in+} (Figs. 1 and 5) as it traverses from rail to rail while V_{in-} remains fixed, current mirror gain and therefore transconductance G_M vary. To mitigate these non-linear effects, bias current I_b is designed to be at least five times greater than the maximum current flowing through resistor R_1 (i.e., $I_b > 5I_{R1}$), so the current variation constitutes only a fraction of the total I_1 current, which for a 10 mV offset in threshold voltage, results in a linearity reduction of 11 dB, as shown in the simulation results of Fig. 7.a and 7.b. The open-loop gain of feedback amplifier A_{int} also changes with ICMR but negative feedback reduces its effects to negligible levels, when compared with the mirror.

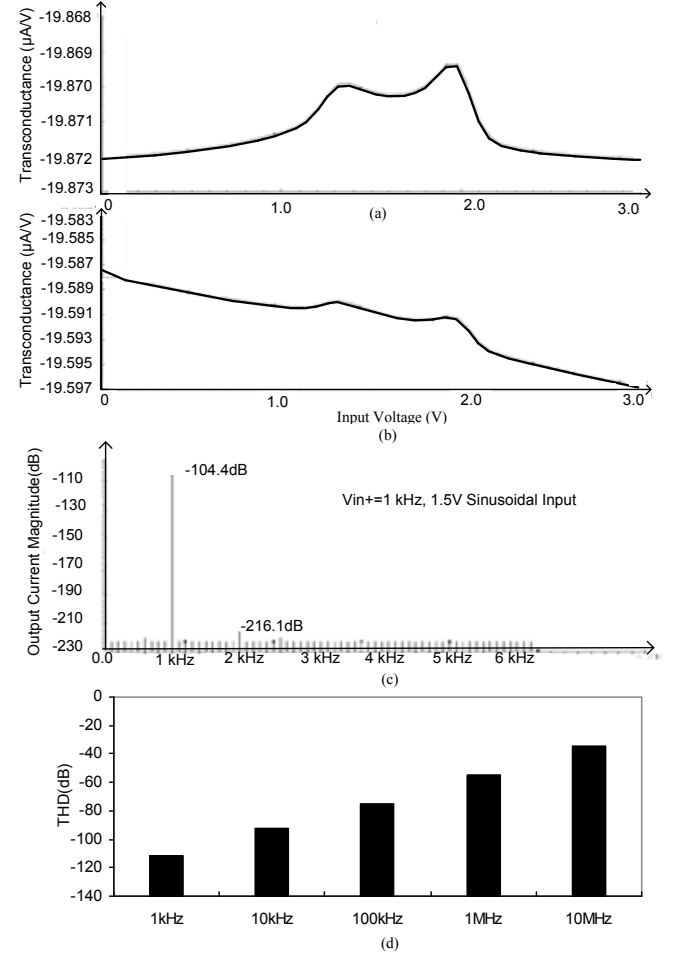


Fig. 7. Transconductance (G_M) variation across ICMR ($0 < V_{in+} < 3V$ and $V_{in-} = 1.5V$) under a 3V supply at a 5A/A current mirror gain (K) with (a) no threshold mismatch and (b) a 10mV threshold mismatch and (c) spectral-output response of transconductance amplifier's output current when a 1 kHz rail-to-rail sinusoidal signal is applied and (d) resulting THD for various input tone frequencies.

Fig. 7(c) shows the simulated spectral-output response of the foregoing transconductance amplifier when applying discrete-Fourier transforms (DFT) on ten cycles of the transient output current when a 1kHz, 1.5V peak (rail-to-rail) sinusoidal signal riding on a 1.5V input common-mode dc voltage is injected into its input while supplied from a 3V source. The output of the transconductance amplifier was connected to a voltage source (to prevent the output voltage from saturating the circuit) and its current monitored, the results of which show that the second harmonic is dominant at

110dB below the fundamental, as expected, given the asymmetrical nature of the circuit topology. The experiment was repeated for different input tones and Fig. 7(d) shows the total harmonic distortion (THD) results for various input frequencies. The circuit is highly linear at low frequencies because the loop gain in the feedback loop comprised of amplifier A_{int} , transistor M_3 , and resistor R_1 is high. As frequency increases and loop gain decreases, however, the linearity decreases and THD increases from approximately -115dB at 1kHz to -40dB at 10MHz.

B. Tunable Resistor R

The bandwidth of the G_M -C filter is tuned by adjusting its shunting load resistance (R in Fig. 1). A $1\text{ k}\Omega/\square$ binarily weighted polysilicon resistor is used for this (Fig. 8). Resistor R_1 from Fig. 5 is not tuned because the parasitic capacitors introduced by the switches limit the overall frequency response of the filter. These parasitic capacitors, on the other hand, have negligible effects when applied to R in Fig. 1 because bandwidth-setting capacitor C is in parallel with R and it is already relatively large.

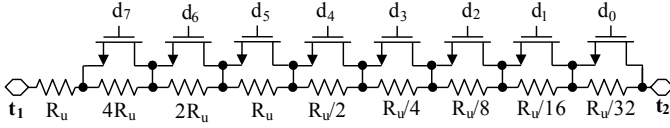


Fig. 8. Programmable and binarily weighted polysilicon resistor R .

Programmability is achieved by decoding a digital word and deciphering the connectivity of controlling NMOS switches d_7 - d_0 from it. When bits d_7 - d_0 are all one, all the switches are closed, short-circuiting the large resistor and resulting in an overall resistance of R_u , the minimum resistance value. As the bit word d_7 - d_0 progresses from all ones to all zeros, the switch resistance increases to $9R_u$ in $R_u/32$ increments. The aspect ratios of the transistors are sufficiently large to prevent their respective switch-on resistances from degrading the resolution of the resistor array (i.e., R_{d0} is significantly lower than $R_u/32$), which in this case is 3.2% of $R_u/32$. Only NMOS devices were used because the supply voltage in the foregoing application was high enough ($> 3\text{ V}$) above the switch terminal voltages ($0.7 - 1.35\text{ V}$) during worst-case conditions to guarantee sufficient gate-drive to short-circuit any resistor in the array. Had the supply voltage been lower or the terminal voltages higher, a PMOS switch would have been placed in parallel with each NMOS device.

C. Non-Overlapping Clocks

Dead time between two clock signals can be inserted by first having each signal sense the other and only allowing a pulse to propagate when the other is off and second by inserting a delay. The NOR gates of the non-overlapping clock generator circuit shown in Fig. 9 perform the sensing and gating function whereas the resistance of weak inverter $I0p1x$ in combination with capacitors C_{d1} and C_{d2} insert a delay of approximately 100 ns between non-overlapping clocks ϕ and ϕ_n . The output signals were designed to have rise and fall times of roughly 10 ns.

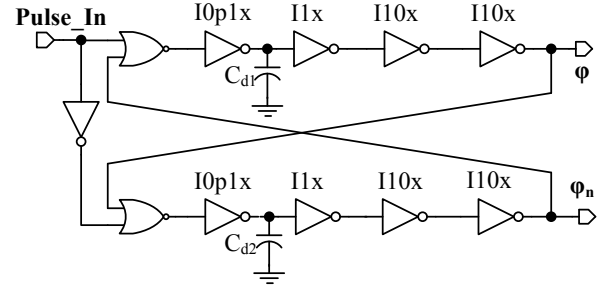


Fig. 9. Non-overlapping clock generator circuit.

The “Pulse_In” is a 1 kHz, 50% duty cycle digital clock signal derived from a single-phase system clock (e.g., ring oscillator). Offset cancellation performance degrades at clock frequencies below 10 Hz because the storage capacitors are discharged by leakage currents and above 10 kHz because the amplifier is not fast enough to settle to its ideal steady-state value during the offset-programming phase [3]. Clock frequency uncertainties resulting from jitter are minimal at low frequencies (e.g., 1 kHz), and even if jitter were present, offset would still be unaffected because at 1 kHz more than enough settling time (i.e., margin) exists for the offset programming phase to settle. The entire system was simulated and verified over the voltage lifespan of a Li-Ion battery (3 – 4.2 V), a military temperature range of -40 to 125 °C, and process corner variations (i.e., slow and fast MOS transistor models and $\pm 20\%$ capacitor, resistor, and bias current variations). Monte Carlo mismatch analysis was also performed to study the offset and linearity performance of the system.

V. EXPERIMENTAL RESULTS

The proposed circuit was designed and fabricated with AMI’s 0.5- μm CMOS process technology. The G_M -C filter die photograph is illustrated in Fig. 10 and its top-level design parameters are summarized in Table 3. Transconductance-setting resistor R_1 is 250 k Ω , bandwidth-setting capacitor C is 60 pF, mirror-gain range is 1-5 with seven bits of resolution, bandwidth-setting resistor range is 325 to 2,900 k Ω with eight bits of resolution, and the auto-zeroing clock frequency is 1 kHz. The DC gain and bandwidth of the filter were adjustable from 1.27 to 29.16 V/V and 1.1 to 6.4 kHz, respectively, partial experimental results of which are shown in Fig. 11.

To minimize clock feed-through and charge-injection errors, hold capacitor pairs C_{h1+} - C_{h1-} and C_{h2+} - C_{h2-} should match and were therefore placed close to each other and laid out using cross-coupling and common-centroid techniques. Similarly, to reduce initial offsets in the transconductor, the same techniques were applied to the transistors used in the current mirror and current source. Transconductance cells G_{M1} and G_{M2} were also placed next to each other and oriented in the same direction for the same reason. For tuning linearity, tuning resistor segments were interdigitated and their periphery surrounded with dummy resistors to reduce etch-induced mismatch effects.

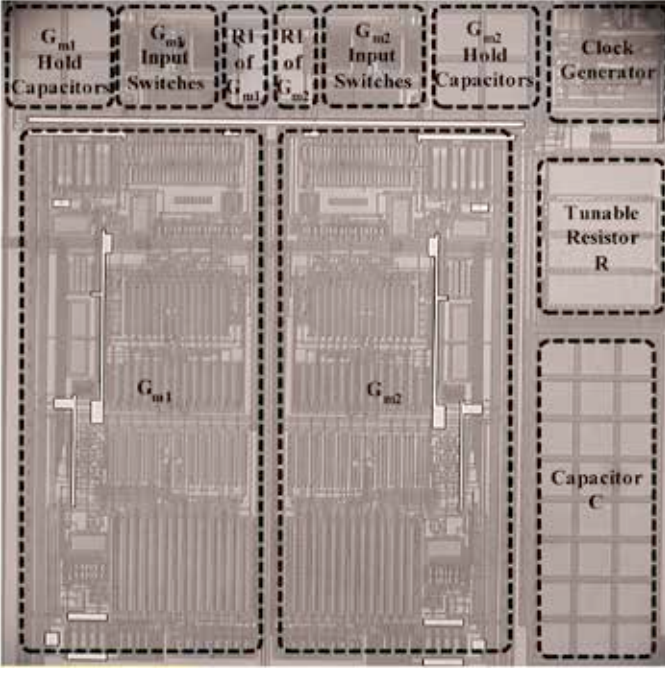


Fig. 10. Die photograph of the 0.5- μm CMOS G_M -C filter (870 μm x 890 μm).

Table 3. Important G_M -C Filter Design Parameters.

Parameter	Value
Transconductance-Setting Resistor (R_1)	250 k Ω
G_M Range ($G_{M-\min}$ - $G_{M-\max}$)	4 – 20 $\mu\text{A/V}$
Minimum Programming Resolution of G_M ($\Delta G_M / G_{M-\min}$)	3.125%
R Range (R_{\min} - R_{\max})	325 - 2,900 k Ω
Minimum Programming Resolution of R ($\Delta R / R_{\min}$)	3.125%
Bandwidth-Setting Capacitor (C)	60 pF
Hold Capacitors (C_{h11} , C_{h12} , C_{h21} , and C_{h22})	6 pF
Auto-Zeroing Clock Frequency	1 kHz

The G_M -C filter was subjected to the low impedance rail-to-rail signal generated by a current-mode switching buck regulator circuit (as shown in Fig. 1) and used to sense and control the regulator's current-mode feedback. The experimental transient results are illustrated in Fig. 12, and as expected, the square wave is integrated into a triangle by the G_M -C filter. The ping-pong "handover" event referred to in the transient glitch analysis section of this paper is highlighted in Fig. 12(b) and shown to be less than 40 mV for worst-case DC output voltage conditions (i.e., largest V_o -to- V_{ref} voltage difference). Although the resulting transient glitch effectively changes the duty cycle of the converter (because its output is used, in part, to control the switching supply), its net effect is negligible and easily compensated within one switching cycle.

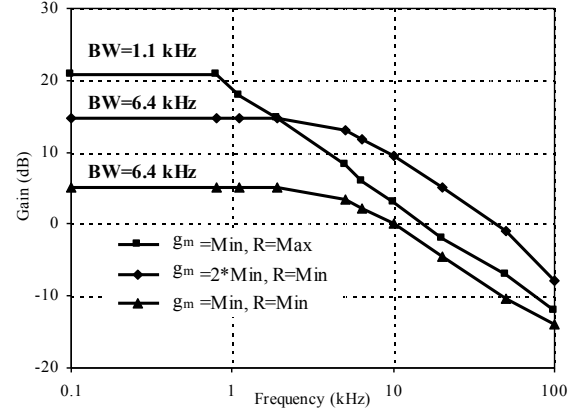


Fig. 11. Experimental frequency response of G_M -C filter.

To verify the offset cancellation capability of the circuit, one of the transconductors was disabled and the other observed, short-circuiting the input and monitoring the output of the transconductor before (V_{o1} in Figs. 2 and 3) and after it is connected to bandwidth-setting capacitor C (V_o) via on-chip buffers, as shown in Fig. 13. The peak-to-peak voltage of V_o represents the cumulative output-referred offset voltage of the summing transconductor because V_o is clamped to V_{ref} when disconnected from the transconductor and auto-zeroed to V_{ref} – ($V_{os}g_mR$) when connected. The resolution of the oscilloscope was unfortunately limited to approximately 5 mV, limiting the measurement's input-referred offset resolution to approximately 500 μV (5 mV / 9.92 V/V).

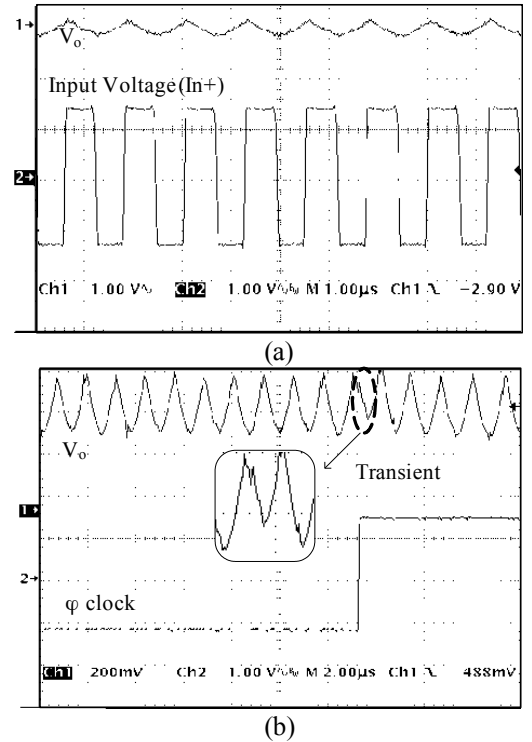


Fig. 12. (a) The G_M -C filter's response to a rail-to-rail square wave and (b) the zoomed-in effects of the ping-pong "handover" transition on the response.

To improve the accuracy of the measurement, the output of the G_M -C filter and therefore the offset of the same were amplified on-chip by 26 dB before measuring it with the oscilloscope, as shown in Fig. 14. Consequently, when G_M -C output V_o is disconnected and clamped to V_{ref} , both inputs of the amplifier in the gain stage are at V_{ref} and the output is therefore zero. However, when the auto-zeroed transconductor is connected, the output voltage difference to V_{ref} is amplified and measured. The clocking sequence of the test setup was as follows: (1) G_M -C filter inputs are short-circuited on-chip and transconductor 1 is auto-zeroed, (2) auto-zero is disabled and transconductor 1 is connected to bandwidth-setting capacitor C with G_M -C filter inputs still short-circuited on-chip, and (3) G_M -C filter inputs are disconnected on-chip but reconnected off-chip.

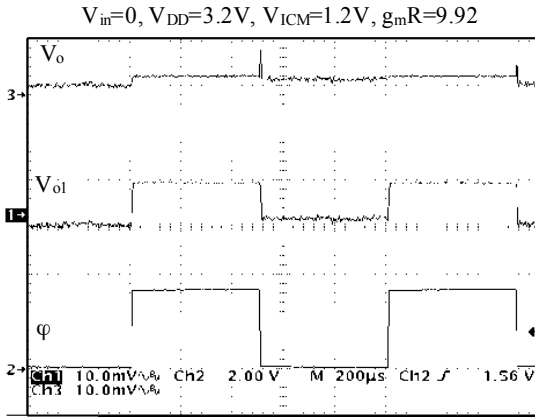


Fig. 13. Ping-ponging between the auto-zeroed transconductor and V_{ref} .

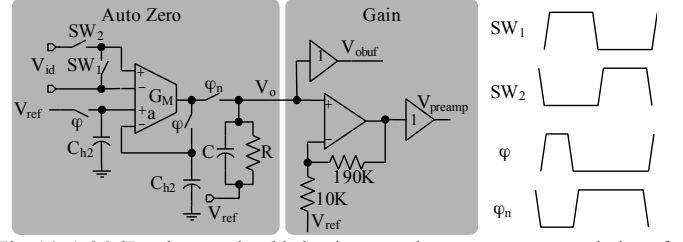


Fig. 14. A 26 dB gain stage is added to increase the measurement resolution of the offset.

Since the circuit is designed to filter the voltage across an off-chip inductor, the voltage difference between the first and third phases of the clocking sequence is the output-referred offset voltage of the transconductor. Because the offset of the additional gain stage is common-mode to all phases and only the differential voltage between phases is measured, the preamplifier's input-referred offset has no effect on the accuracy of the measurements. The amplified output-referred offset under various conditions (power supply of 3 and 4.2 V and input common-mode range of 1, 1.2, and 1.5 V) are shown in Fig. 15. The resulting input-referred offset for three samples was less than $\pm 210 \mu V$ (42 mV divided by the G_M -C filter's gain of 9.92 and pre-amplifier gain of 20). A slight dependence to supply voltage was observed, as anticipated in Eq. 3, for which high PSRR design techniques can be used.

The 40 μV difference between phase 2 and phase 3 input voltages (8 mV divided by the G_M -C filter's gain of 9.92 and pre-amplifier gain of 20) occurs because the off-chip short-

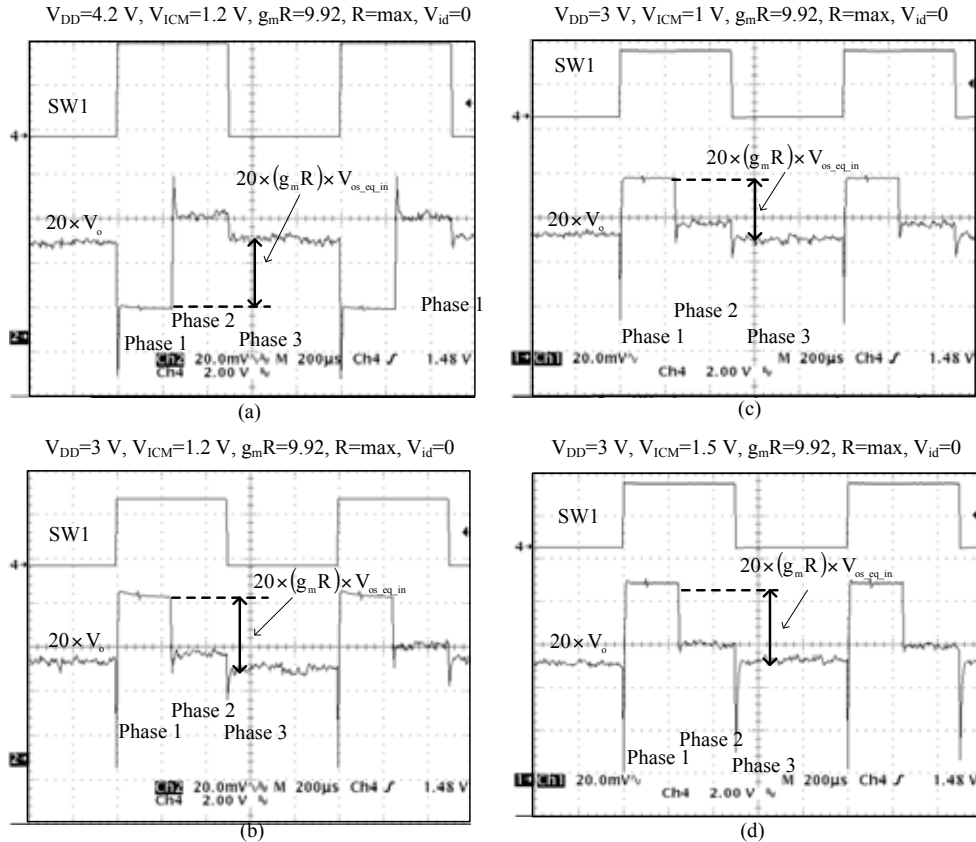


Fig. 15. Offset measurements under various supply and common-mode input voltage conditions.

circuit condition is not ideal. Issues such as thermocouple effects can cause non-zero input voltages at the input of the transconductor during the offset measurement phase.

The circuit was operational for auto-zeroing clock frequencies ranging from 10 Hz to 10 kHz. At higher frequencies, as alluded to earlier, the auto-zeroing properties were diminished because the circuit does not have enough time to settle to its auto-zeroed value. On the other extreme, the hold capacitors limit the amount of time the auto-zeroed voltage is held in the presence of leakage currents from parasitic reverse-biased junction diodes, which is worst at high temperatures where leakage currents are at their highest levels [3, 20]. Since DC offsets are nothing more than low frequency signals, dynamic offset-cancellation schemes also reduce 1/f low frequency noise. Given the low bandwidth nature of the G_M -C filter, output noise is further reduced, and in the foregoing case, the total input-referred noise was measured to be 93 μ V with a filter DC gain of about ten at R_{Max} . The circuit's nonlinearity performance ($\Delta G_M/G_M$) was found to be -57 dB by measuring the resulting common-mode input-induced systematic offset for a rail-to-rail non-inverting input signal. Table 4 summarizes these and the other experimental performance parameters of the circuit.

Table 4. Measured Performance of the Proposed CMOS G_M -C Filter.

Technology	AMI's 0.5- μ m CMOS
Chip Area	870 μ m x 890 μ m
Supply Voltage	3 - 4.2 V
Supply Current	
Min G_{M1}	0.62 mA
Max G_{M1}	1.20 mA
BW (1/RC) Programmability (resolution for worst case – min. R)	1.1 - 6.4 kHz (3.2% resolution)
Gain ($G_{M1}R$) Programmability (resolution for worst case – min. G_{M1})	1.27 - 29.16 V/V (3.2 % resolution)
Input-Referred Offset (Gain = 9.92, max. R, 3 units tested)	< \pm 210 μ V
Power-Supply Rejection Ratio (DC)	74 dB
Common-Mode Rejection Ratio (DC)	83 dB
In- ICMR (V)	0.5 V to ($V_{DD} - 1$)
In+ ICMR (V)	-0.4 V to V_{DD}
Transconductance Non-Linearity ($\Delta G_M/G_M$) Rail-to-Rail V_{in+} , $V_{DD} = 3$ V, $V_{in-} = 1.5$ V	-57 dB
Total Input-Referred Noise (C = 60 pF, Gain = 9.92, max. R)	93 μ V
Second Pole	4 MHz
Ping-Pong ("Handover") Transient Glitches	< 40 mV

VI. CONCLUSIONS

A programmable and linear low offset 0.5- μ m CMOS G_M -C filter has been proposed, designed, fabricated, and evaluated. The experimental offset was measured to be less than \pm 210 μ V for 3 to 4.2 V supply voltages (lithium-ion battery supply range) and 1 to 1.5 V input common-mode voltages. The DC gain and bandwidth were adjustable from 1.1 to 6.4 kHz and 1.27 to 29.16 V/V, respectively, both with better than 3.2% resolution by adjusting the transconductance via the gain of a

current mirror and the resistance of a shunting bandwidth-setting resistor. "Handover" glitches during ping-pong transitions were less than 40 mV while achieving a nonlinearity performance of -57 dB. The low input-referred offset, high linearity, continuity, and programmable features achieved with this design are appealing to a growing number of high performance analog systems, from power-hopped switching power supplies to front-end interface electronics for telemetry applications, and all under the constraints of CMOS integration. Analog filters, however, which are prevalent in most, if not all, applications that interface with the real world, benefit the most from these performance characteristics.

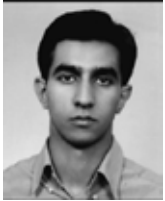
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