# Light-Harvesting CMOS Power-Supply System for 0–10-mW Wireless Microsensors

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***Abstract*—Wireless microsensors in consumer products, homes, hospitals, and factories incorporate sensing, processing, and transmission intelligence that can save money, energy, and lives. Although their tiny batteries deplete quickly, harvesting light energy can replenish what they supply. Still, a 1-mm$^2$ PV cell can only generate up to 150 µW of the mW's that a wireless microsensor can consume. The battery-assisted light-powered harvester presented here therefore draws 10–130 µW from a 1 × 1-mm$^2$ PV cell and assistance from a battery to supply a 10-mW load and recharge the battery with excess PV power. The CMOS system regulates its 1-V output within ±28 mV while supplying 10× more power per 1 mm$^3$ with 94.5% efficiency and 38× with 87.8% efficiency than the best light-harvesting microsystem reported. Unlike others whose efficiencies peak at one power level, efficiency here is 94.5% across $v_{PV}$'s 10–130-µW and $P_{LD}$'s 0.5–10-mW with a 18-µH 3 × 3 × 1.5-mm$^3$ inductor and 87.8% with a 22-µH 1.6 × 0.8 × 0.8-mm$^3$ device.**

***Index Terms*— Ambient light, energy harvester, photovoltaic (PV) cell, CMOS microsystem, switched-inductor converter, wireless microsensor, charger, and power supply.**

## I. Light-Harvesting Microsystems

Advances in the semiconductor industry have made possible the integration of sensors, processors, memory, and transceivers into tiny wireless devices [1]–[3]. Powering these sensors over extended periods remains a challenge, however, because the tiny on-board batteries that these sensors can fit store little energy. Plus, the cost of personnel employed to replace these batteries is often prohibitive. Luckily, ambient light, motion, heat, and radiation can continually replenish the energy that these batteries supply [4]–[8].

Photovoltaic (PV) cells can generate 150 µW/mm$^2$ from sunlight. This is 100× more power than electrostatic or piezoelectric transducers can harvest from motion and thermoelectric generators can generate from heat [4]–[8]. Unfortunately, PV cells output 100× less power with artificial lighting than with sunlight. In other words, mm cells can generate a few µW's indoor and up to 150 µW outdoors.

Although transmissions can require mW's, microsensors seldom transmit in practice. In fact, many sensors mostly idle or sense, so on average they often consume nW's [3]. A system can therefore rely on a µW ambient source to replenish the energy that a battery loses to transmissions. For example [7] cites a pulse oxymeter sensor node that consumes 90 µW to process and transmit data every 15s. Similarly the intraocular sensor node in [3] consumes 240 nW to measure eye pressure. This way, with the assistance of a battery, an ambient source can supply a wireless microsensor almost indefinitely. The battery supplies on demand what the PV cell avails over time, so light ultimately supplies the system.

The charger–supply system in Fig. 1, for example, harvests PV power $P_{PV}$ from a PV source $v_{PV}$. When the system idles, $v_{PV}$ can supply more power than the sensor system demands with $P_{LD}$. The supply system therefore directs excess PV power to the battery $v_B$. During a transmission, however, $P_{PV}$ may be insufficient, so the system draws assistance from $v_B$.

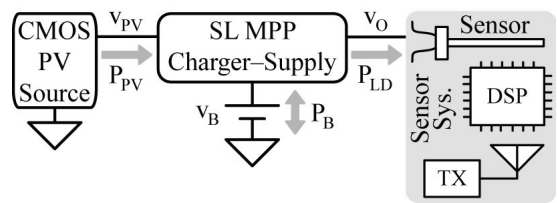


**Fig. 1**. Light-harvesting wireless microsensor.

The charger–supply [9]–[15] should therefore transfer power from $v_{PV}$ to the output $v_O$ and to $v_B$ and from $v_B$ to $v_O$. It should do so with minimal losses and at the maximum power point [16]–[18]. Switched inductors are usually more efficient than switched capacitors because switched capacitors typically need more power-consuming switches [8], [19]. This paper therefore proposes a PV-sourced switched-inductor charger–supply system in Sections II–III whose CMOS implementation Section IV describes. Key aspects that distinguish this technology from the state of the art are integration (small size) and energy management (high power-conversion efficiency). Section V discusses how the prototype built compares with the state of the art. Section VI then draws relevant conclusions.

## II. CMOS PV-Sourced Charger–Supply

### A. CMOS PV Cell

PV cells are essentially PN junctions. In neutral conditions, charge carriers diffuse across the junction, leaving ionized parent atoms behind. So when photons liberate loosely bound electrons in this region, the electric field that these parent atoms establish pull electrons and the holes they leave behind across the region. The net result is a photonic current $i_{PH}$.

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The PN junctions that are normally available in standard CMOS technologies are shallow $P^+$ regions in N well, N-well regions over a P substrate, and $N^+$ regions over a P substrate. To stack cells over the same substrate, neither terminal can connect to the substrate. This is why only shallow $P^+$ regions in an N well like Fig. 2 shows can stack. Unfortunately, these devices incorporate $P^+$–N well–P substrate BJTs that leak too much power to the substrate [20]–[21].

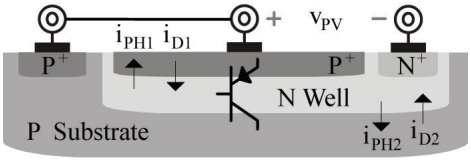


**Fig. 2**. $P^+$ in N well photovoltaic (PV) cell.

Still, this device incorporates two PN junctions with separate depletion regions that together can collect more of the electron–hole pairs that photons liberate. By connecting the junctions in parallel, sunlight can generate more $i_{PH}$ [18]. The diodes that these PN junctions also establish, however, divert some $i_{PH}$ away as $i_D$. As a result, $v_{PV}$ outputs with $i_{PV}$ the difference $i_{PH} - i_D$.

The power that $i_{PH}$ generates $P_{PH}$ and the power that $i_D$ consumes $P_D$ both hinge on $v_{PV}$. So PV power $P_{PV}$ in Fig. 3 rises with $v_{PV}$ *until* $P_D$'s incremental loss $-\Delta P_D$ cancels $P_{PH}$'s gain $+\Delta P_{PH}$. The maximum power point $P_{MPP}$ happens when these incremental variations balance and increases with light intensity. The $v_{PV}$ that outputs $P_{MPP}$ can be 400–500 mV.

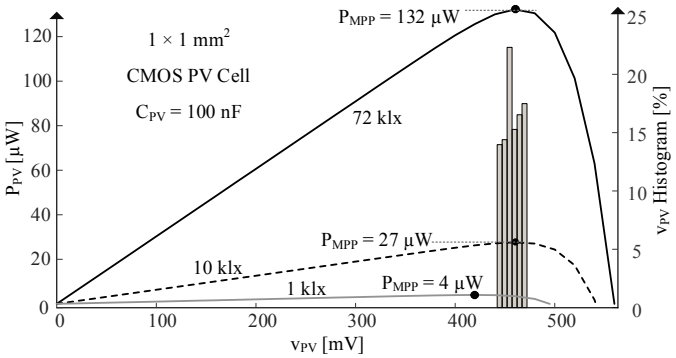


**Fig. 3**. Measured photovoltaic power and histogram in the system.

## B. Power Stage

The power stage should draw power from the PV cell $v_{PV}$ to feed the sensor system at $v_O$. Excess PV power should replenish the battery $v_B$. When PV power cannot sustain the sensor, the system should draw assistance from $v_B$. In other words, the power stage proposed draws power from $v_{PV}$ and $v_B$ and supplies $v_O$ and $v_B$, depending on operating conditions.

Although the sensor system consumes less power with a lower supply voltage $v_O$, the supply system and other analog electronics stop working below a headroom level that is often about 1 V [3]. Breakdown voltage, which in this case is 1.8 V, is another limit that constrains $v_B$. So the power stage proposed in Fig. 4 boosts $v_{PV}$'s 350–500 mV to $v_O$'s 1 V and $v_B$'s 1.8 V and bucks $v_B$'s 1.8 V to $v_O$'s 1 V.

Unfortunately, on-chip inductors usually suffer from low inductance $L_X$ and high resistance $R_L$. This is a double challenge because low $L_X$ holds less energy with a given current $i_L$. So $i_L$ is usually high, and with a high $R_L$, ohmic power is that much higher. A higher switching frequency $f_{SW}$ can keep $i_L$ from reaching such a high level. The problem with this is that controlling and switching the network at higher $f_{SW}$ requires more power. Luckily, commercially available off-chip inductors with $sL_X$-to-$R_L$ ratios (i.e., quality factors) of 50–100 can be as small as 1 mm³ [13]. But since they are still bulky, the system in Fig. 4 proposes to use only one inductor.

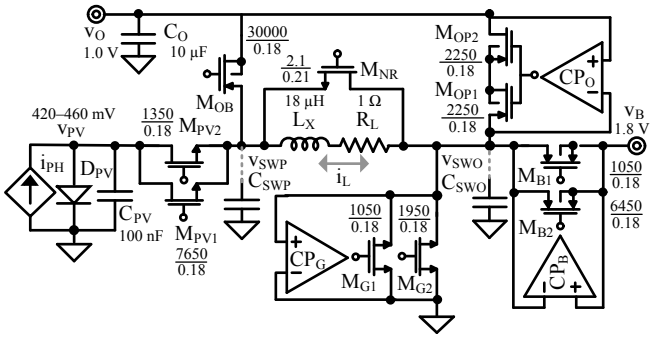


**Fig. 4**. CMOS PV-sourced charger–supply stage.

Inductors energize with positive voltages and drain with negative voltages. So with transistors $M_{PV1}$ and $M_{PV2}$ closed, $M_{G1}$ in Fig. 4 and Fig. 5 closes to magnetize $L_X$ from $v_{PV}$. $M_{G1}$ then opens and $M_{OP1}$–$M_{OP2}$ closes to apply the negative voltage that drains $L_X$ into $v_O$. If the load does not need energy, $M_{B1}$ closes instead to drain $L_X$ into $v_B$. But if the load still needs energy after draining $L_X$ into $v_O$, $M_{PV1}$–$M_{PV2}$ opens and $M_{OB}$ closes. With $M_{OB}$ closed, $M_{B1}$–$M_{B2}$ then closes to energize $L_X$ from $v_B$ into $v_O$ and $M_{G1}$–$M_{G2}$ later close to drain $L_X$ into $v_O$. $M_{G1}$-$M_{G2}$'s and $M_{B1}$-$M_{B2}$'s source terminals swap positions because current can flow in both directions.

MOSFETs burn ohmic power $P_{MR}$ and require gate-drive power $P_{MG}$ to switch. Since $P_{MR}$ and $P_{MG}$ both climb with longer channels, channel lengths in Fig. 2 are the shortest possible that can sustain 1.8 V. On the other hand, $P_{MR}$ falls and $P_{MG}$ rises with wider channels. So overall losses fall with wider transistors until the rise in $P_{MG}$ cancels the fall in $P_{MR}$. In other words, transistors consume the least power when their channels are optimally wide for the current they conduct.

This is why some transistors in Fig. 4 are in parallel. For example, $M_{B1}$ alone closes to drain $L_X$ into $v_B$ the energy that $v_{PV}$ supplies and $M_{B1}$ and $M_{B2}$ together close to energize $L_X$ from $v_B$ because $v_B$ delivers more power than $v_{PV}$. $M_{G1}$ alone closes to energize $L_X$ from $v_{PV}$ and $M_{G1}$ and $M_{G2}$ together close to drain $L_X$ into $v_O$ the energy that $v_B$ supplies for the same reason. $M_{PV2}$ is optimally sized to deliver PV power $P_{PV}$. But since $v_{PV}$ is always connected to $L_X$ when the system is over-sourced, $M_{PV2}$ does not require $P_{MG}$. So paralleling $M_{PV1}$ in this mode reduces resistance without sacrificing $P_{MG}$.

$M_{OP1}$ and $M_{OP2}$ are in series so their body diodes block one another. This way, body diodes cannot conduct current when the combined switch is off. With only one transistor, the bulk would connect to $v_O$ to keep the body diode from engaging when the switching node $v_{SWO}$ falls. This, however, keeps $v_{SWO}$ from climbing above $v_O$ to $v_B$ when directing $i_L$ to $v_B$.

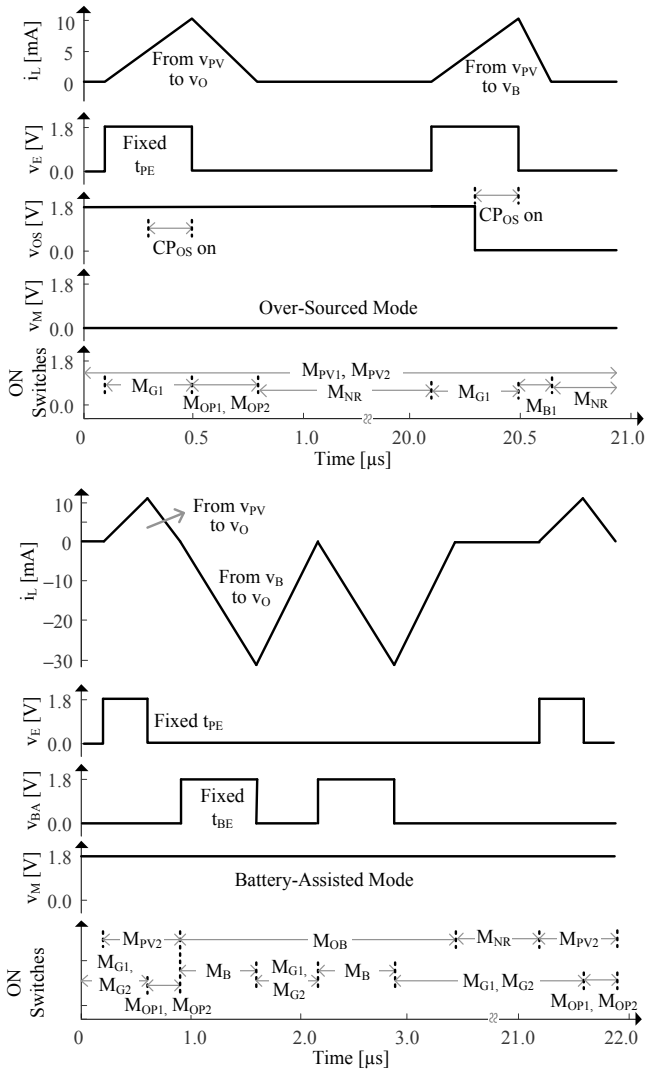


**Fig. 5**. Timing diagram (a) over-sourced (b) battery-assisted.

To remain at the maximum power point $P_{MPP}$ in Fig. 3, $v_{PV}$ should be steady. Similarly, $v_O$ should be steady for the wireless microsensor to operate optimally and reliably. The supply system, however, switches $L_X$ between input and output terminals, so the current pulled from $v_{PV}$ and steered into $v_O$ change abruptly from zero to $i_L$. The purpose of capacitors $C_{PV}$ and $C_O$ is to reduce the voltage fluctuations that these abrupt current changes produce.

Between transfers, remnant energy in $L_X$ drains into parasitic switch-node capacitances $C_{SWP}$ and $C_{SWO}$ and cycle back to $L_X$ in resonant fashion. $L_X$ and $C_{SW}$'s exchange energy back and forth until resistances burn the energy. The purpose of $M_{NR}$ is to burn this energy *quickly* so the oscillations and noise that $L_X$ and $C_{SW}$'s would otherwise produce fade faster.

The controller decides which transistors to close. The controller also determines which energizing switches to open. Draining output switches, however, can open like diodes, when they stop receiving $L_X$'s current $i_L$. For this, comparators $CP_B$, $CP_O$, and $CP_G$ open $M_{B1}$, $M_{OP1}$–$M_{OP2}$, and $M_{G1}$–$M_{G2}$ when $v_{SWO}$ falls below $v_B$ or $v_O$ or $v_{SWO}$ rises above ground. To save power, these comparators activate after the controller closes the switches and power off after the comparators open them. $CP_G$, $CP_B$, and $CP_O$ are trimmed so their offsets and delays balance to keep efficiency from suffering. Since $M_{G1}$ is also an energizing switch when drawing PV power $P_{PV}$, the controller opens $M_{G2}$ when $M_{G1}$ energizes.

## III. CMOS Controller

The controller proposed in Fig. 6 draws enough power from the PV cell to keep $v_{PV}$ near the maximum power point peak $v_{MPP}$. It also steers enough of that power, and if necessary, additional power from the battery $v_B$ to keep $v_O$ near its 1-V target $v_R$. In other words, the controller regulates $v_{PV}$ and $v_O$. $v_{PV}$ is programmable with $v_{MPP}$ and $v_O$ with $v_R$.

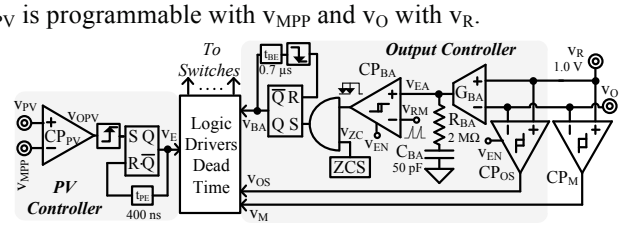


**Fig. 6**. CMOS controller.

The controller decomposes into four sections: PV, output, mode, and logic control. When gate signals to the transistors that connect to $v_{SWP}$ and $v_{SWO}$ in Fig. 4 crisscross, switches close and the supply nodes to which they connect short-circuit. This is a problem that the logic avoids by inserting dead time between the gate signals of adjacent switches. The logic also includes drivers large enough and quick enough to drive the large capacitive gates that power transistors present.

The controller consumes quiescent power $P_Q$ that climbs with switching frequency $f_{SW}$. To limit this loss, $f_{SW}$ should be low. Except, energizing and draining $L_X$ across long periods delivers more power than the sensor system requires. So the charger–supply here draws and delivers infrequent energy packets that are large enough to sustain the system. In other words, $L_X$ conducts discontinuously.

This way, the switching network excludes the inductor pole and out-of-phase right-half-plane zero that boosting switched inductors normally exhibit [22]–[23]. This is important because, in the absence of other poles and zeros, $C_{PV}$ and $C_O$ establish the only dominant poles in the loops that the PV and output controllers close. As a result, their respective loop gains reach 0 dB with 90° of phase margin, so the loops are stable.

### A. Photovoltaic Regulation

When open-circuited, the PV cell's photonic current $i_{PH}$ in Fig. 4 feeds parasitic diode $D_{PV}$ until $v_{PV}$ reaches 500–600 mV. At this level, $i_{PV}$, and in consequence, $P_{PV}$ are zero. The purpose of the PV controller in Fig. 6 is to draw enough power from $v_{PV}$ to keep $v_{PV}$ at the level that $i_{PV}$ with $v_{PV}$ output the highest power $P_{MPP}$. In steady state, $v_{PV}$ should be 350–500 mV [18].

Since transistors consume the least power when they conduct a particular current, the system draws PV energy packets $E_{PV}$'s that always peak to the same level. For this, $L_X$ energizes across the 400 ns that the fixed-pulse block $t_{PE}$ in Fig. 6 sets. $M_{PV1}$, $M_{G1}$, $M_{B1}$, and $M_{OP1}$–$M_{OP2}$ in Fig. 4 are optimally sized to conduct this energy. The controller adjusts $P_{PV}$ by adjusting the frequency $f_{PV}$ of the packets.

For this, comparator $CP_{PV}$ commands $L_X$ to draw an $E_{PV}$ when $v_{PV}$ surpasses its targeted maximum power-point peak $v_{MPP}$. Drawing $E_{PV}$ (at 20 ms in Fig. 7) pulls $v_{PV}$ below $v_{MPP}$. Excess $i_{PH}$ then charges $C_{PV}$ until $v_{PV}$ again surpasses $v_{MPP}$, at which point $CP_{PV}$ prompts $L_X$ to draw another packet that discharges $C_{PV}$. $v_{PV}$ rises and falls this way about its optimal average level $v_{PV(AVG)}$. Although this rippling behavior shifts $v_{PV}$ from its absolute optimal setting, like the histogram in Fig. 3 shows, $C_{PV}$ limits the variation to such a degree that $P_{PV}$ is still within 1% of $P_{MPP}$.

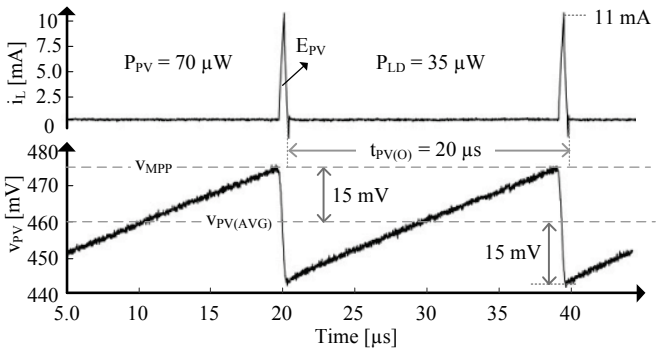


**Fig. 7**. Measured inductor current and photovoltaic voltage.

Operationally, $CP_{PV}$ sets a flip-flop whose output commands the logic to energize $L_X$ across the 400 ns that $t_{PE}$ sets. $v_{MPP}$ is the output of a lookup table that determines which setting is optimal for the light intensity received. The advantage of the look-up table over open-circuiting the PV cell to sense the cell's state is that the latter cannot output power across the open-circuit interruption. The look-up table that generates $v_{MPP}$ is set externally. The look-up table that sets $v_{MPP}$ adjusts $v_{PV}$ so the PV cell remains at the maximum power point, irrespective of process and operating conditions. Since $i_{PH}$ is higher for more intense light and a higher $i_{PH}$ can supply a larger $E_{PV}$, $i_{PH}$ and $E_{PV}$ charge and discharge $C_{PV}$ faster. In other words, packet frequency $f_{PV}$ in Fig. 8 is proportional to the PV power that light intensity establishes.

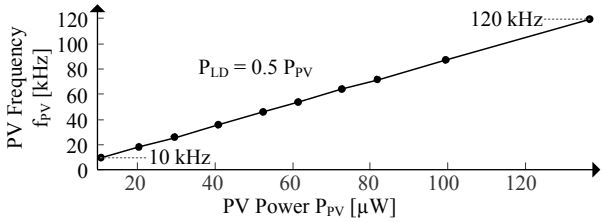


**Fig. 8**. Measured PV packet frequency.

## B. Output Regulation

Over-Sourced: When PV power $P_{PV}$ surpasses the needs of the sensor system, comparator $CP_{OS}$ determines when to steer excess power to the battery $v_B$. For this, $CP_{OS}$ compares the output $v_O$ with the targeted 1-V reference $v_R$. So as long as the load pulls $v_O$ below $v_R$, $CP_{OS}$ commands the logic, switches, and $L_X$ to draw and steer PV energy packets $E_{PV}$'s (at 15 ms in Fig. 9) to $v_O$. $CP_{OS}$ prompts $L_X$ to direct excess $E_{PV}$'s to $v_B$ (at 30 ms in Fig. 9) when $v_O$ rises above $v_R$.

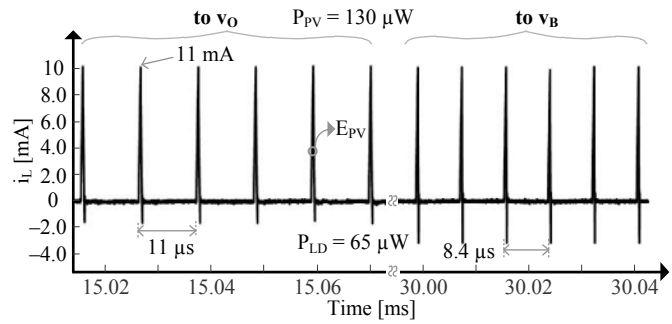


**Fig. 9**. Measured over-sourced inductor current.

Since $v_O$'s 1 V is lower than $v_B$'s 1.8 V, $L_X$ drains more slowly with $v_O$ than with $v_B$. So although the PV controller's fixed-pulse block $t_{PE}$ always energizes $L_X$ across the same 400 ns to 11 mA, $L_X$'s $i_L$ falls more slowly when directed to $v_O$ (at 15 ms). Interestingly, $v_{PV}$ delivers more power to $v_O$ this way because $L_X$ drains into $v_O$ while still connected to $v_{PV}$. But since the $P_{MPP}$ that light intensity sets does not change, the PV controller delivers packets to $v_O$ less often. This is why $v_O$ in Fig. 9 receives $E_{PV}$'s every 11 µs and $v_B$ every 8.4 µs.

To keep noise from inadvertently tripping the comparator, $CP_{OS}$ incorporates hysteresis. This means that $v_O$ does not stop receiving $E_{PV}$'s until $v_O$ in Fig. 10 falls 28 mV below $v_R$'s 1 V. Similarly, but in the opposite direction, $v_O$ does not begin to receive $E_{PV}$'s until $v_O$ climbs 28 mV above $v_R$'s 1 V. To save power, $CP_{OS}$ only activates when the system is over-sourced, and only while energizing $L_X$. Hysteresis is built into $CP_{OS}$ and designed to be higher than 20 mV to suppress the effects of +/−5 m-V noise when tolerance is up to +/−50%.

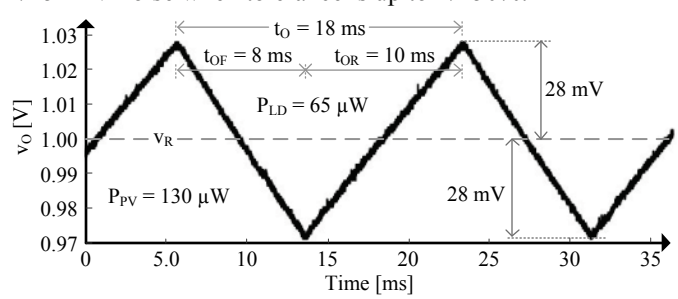


**Fig. 10**. Measured over-sourced output voltage.

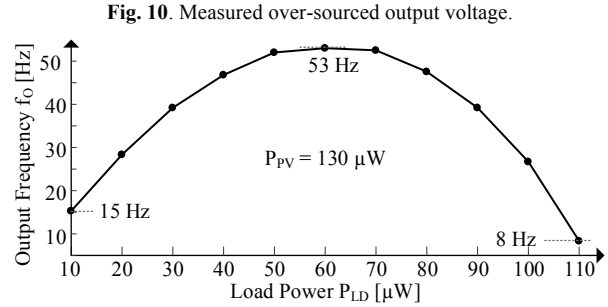


**Fig. 11**. Measured output frequency.

$C_O$'s charge and discharge times $t_{OR}$ and $t_{OF}$ set $v_O$'s output frequency $f_O$. The system load $P_{LD}$ discharges $C_O$ (between 6 and 14 ms in Fig. 10) because $L_X$ disconnects from $v_O$ when directing $E_{PV}$'s to $v_B$. When receiving $E_{PV}$'s, however, excess PV power charges $C_O$ (between 14 and 24 ms). Since this excess energy is greater with lighter loads and *vice versa*, $t_{OR}$ and $t_{OF}$ shift in opposite directions with $P_{LD}$. In Fig. 11, for example, $t_{OR}$ and $t_{OF}$ balance and $f_O$ peaks at 53 Hz when $P_{LD}$

is 60 μW. Lighter loads extend $t_{OF}$ more than excess PV power shortens $t_{OR}$, so $f_O$ falls to 15 Hz with 10 μW. Heavier loads, on the other hand, shorten $t_{OF}$ less than excess power lengthens $t_{OR}$, so $f_O$ similarly falls to 8 Hz with 110 μW.

Battery-Assisted: When PV power $P_{PV}$ is not enough to feed the sensor system, the logic automatically delivers $v_{PV}$'s energy packet $E_{PV}$ to $v_O$ and another packet $E_B$ from $v_B$. Transconductor $G_{BA}$ closes the feedback loop that determines how much additional power $v_B$ delivers.

Since transistors consume the least power when they conduct a particular current, the system draws energy packets that peak to the same level. For this, $L_X$ energizes across the time that the fixed-pulse block $t_{BE}$ in Fig. 6 sets. Since the load can pull up to 10 mW and the PV cell can only supply up to 130 μW, $v_B$ must be able to supply more power than $v_{PV}$. This is why $t_{BE}$ is 300 ns longer than $t_{PE}$, so $L_X$ can peak to 31 mA in Fig. 12, and with 31 mA, deliver a larger energy packet $E_B$. $M_{B1}$ and $M_{B2}$, $M_{G1}$ and $M_{G2}$, and $M_{OB}$ in Fig. 4 are optimally sized for this energy level. The controller adjusts $P_B$ by adjusting the number of packets delivered between $E_{PV}$'s.

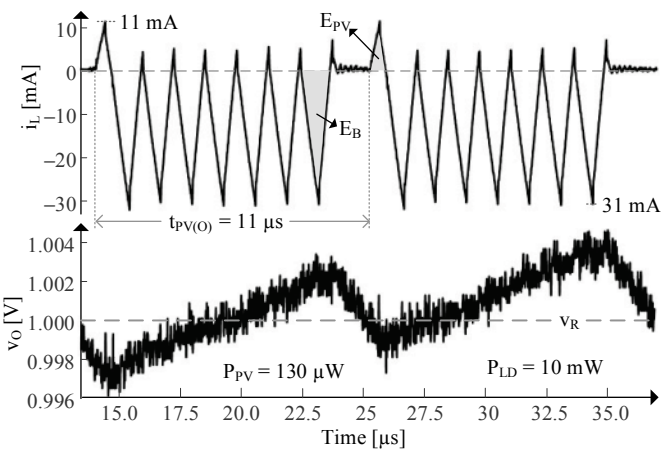


**Fig. 12**. Measured battery-assisted inductor current and output voltage.

For this, $G_{BA}$ senses and amplifies the error $v_{EA}$ between $v_O$ and the targeted $v_R$. $CP_{BA}$ then compares $v_{EA}$ to $v_{RM}$'s saw-tooth ramp to determine how long the system should deliver $E_B$'s. When $v_O$ falls below $v_R$, for example, $v_{EA}$ rises and $CP_{BA}$ waits longer for $v_{RM}$ to reach this higher $v_{EA}$. In the interim, the zero-current sensor ZCS, which resets after every $E_B$, continues to set the flip-flop that triggers new $E_B$'s. The system delivers consecutive $E_B$'s this way until $CP_{BA}$ trips.

To save power, $G_{BA}$ activates only when the system enters battery-assisted mode. $CP_{BA}$ is on only while delivering $E_B$'s. More specifically, $CP_{BA}$ activates after $L_X$ sends $E_{PV}$ and powers off after $L_X$ sends the last $E_B$.

To avoid conflicting $L_X$ commands from the PV and output controllers, the logic inserts a 1.5-μs blank time before every $E_{PV}$. This way, $E_B$'s and $E_{PV}$'s never overlap. Incidentally, since $E_{PV}$ is not high enough to supply the load, $C_O$ does not begin to charge until $L_X$ delivers the first $E_B$. This is why $v_O$ in Fig. 12 only rises when receiving $E_B$'s.

When an integer number of $E_B$'s across one $t_{PV}$ does not match the steady-state needs of the system, the system oversupplies and undersupplies $E_B$'s in alternate $t_{PV}$ cycles so the average number of $E_B$'s is the fraction that matches the load. In Fig. 13, for example, the system delivers two sets of 7 $E_B$'s between every set of 6, which is 6.67 $E_B$'s on average. This variation in $E_B$'s produces the subtle sub-harmonic fluctuation seen in $v_O$ in Figs. 11 and 12.

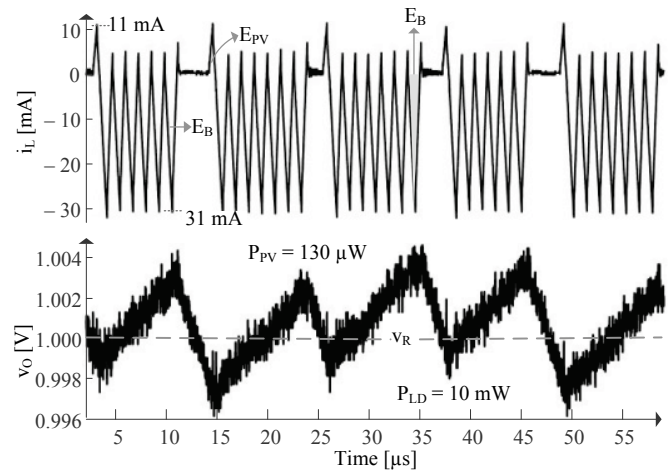


**Fig. 13**. Measured output when alternating the number of battery packets.

Without $R_{BA}$ and $C_{BA}$, $G_{BA}$'s high output resistance sets a low-frequency pole $p_{EA}$ that along with $C_O$'s pole $p_O$ can reduce the loop gain to 0 dB with 0° of phase margin. Although $C_{BA}$ pulls $p_{EA}$ to lower frequency, $R_{BA}$ current-limits $C_{BA}$'s current to remove the effects of the dominant pole:

$$p_{EA} = \frac{1}{2\pi(R_{EA}+R_{BA})C_{BA}}, \quad (1)$$

with a zero:

$$z_{BA} = \frac{1}{2\pi R_{BA} C_{BA}}. \quad (2)$$

$R_{BA}$'s then establishes a pole $p_{BA}$ with $v_{EA}$'s parasitic capacitance $C_{EA}$ that is greater than the 0-dB frequency $f_{0dB}$ that $p_O$ (without the effects of $p_{EA}$) sets. The output load $R_O$ and effective inductor impedance $R_L$ along with $C_O$ sets the output pole:

$$p_O = \frac{1}{2\pi(R_L \| R_O)C_O}. \quad (3)$$

In other words, $z_{BA}$ cancels $p_{EA}$ and $p_{BA}$ is higher than $f_{0dB}$, so the system is stable.

### *C. Mode Regulation*

Comparator $CP_M$ in Fig. 6 ultimately determines whether battery assistance is needed or not. In other words, $CP_M$ determines which mode of operation the system should adopt. For this, $CP_M$ compares $v_O$ to its targeted $v_R$ and incorporates hysteresis whose threshold limits are well above and well below the $v_O$ peaks that $CP_{OS}$ and $G_{BA}$ produce when they regulate $v_O$. So if $E_{PV}$'s alone (when $CP_{OS}$ regulates $v_O$) cannot sustain the load $P_{LD}$, excess $P_{LD}$ discharges $C_O$ from cycle to cycle. When $v_O$ reaches $CP_M$'s lower threshold, $CP_M$ trips high into battery-assisted mode. Similarly, if one $E_B$ (when $G_{BA}$ regulates $v_O$) oversupplies $P_{LD}$, excess $P_B$ charges $C_O$ to $CP_M$'s upper threshold, where $CP_M$ trips low into over-sourced mode.

Static and dynamic components ultimately dictate $CP_M$'s hysteretic limits. Because when $v_O$ reaches $CP_M$'s lower static threshold, the system does not respond until a propagation

delay later. As a result, $v_O$ rises or falls an additional amount. This dynamic effect diminishes, however, with slow variations in $v_O$. When load power $P_{LD}$ in Fig. 14 suddenly falls from 5 mW to 50 µW, for example, excess battery power $P_B$ charges $C_O$ slowly until $v_O$ reaches $CP_M$'s upper 60-mV threshold. When $P_{LD}$ suddenly rises back to 5 mW, however, excess $P_{LD}$ discharges $v_O$ so quickly that the system does not react until after $v_O$ falls below the 60-mV threshold by another 12 mV.

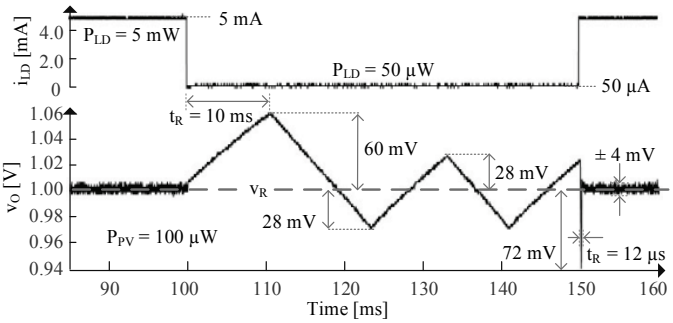


**Fig. 14**. Measured output when subjected to mode-swinging load dumps.

## IV. Prototype Implementation

The 1 × 1-mm$^2$ and 0.9 × 0.9-mm$^2$ CMOS dies in Fig. 15 integrate the PV cell, power transistors, and controller blocks in Figs. 2, 4, and 5. Test circuits and power passives $L_X$, $C_{PV}$, and $C_O$ in Fig. 4 are off-chip on the two-layer board shown. $L_X$ is either 18 µH with 1 Ω of dc resistance and 3 × 3 × 1.5 mm$^3$ in volume or 22 µH with 2 Ω and 1.6 × 0.8 × 0.8 mm$^3$. Although the former occupies more space, its resistance burns less power. $C_{PV}$ is 100 nF and occupies 1.0 × 0.5 × 0.5 mm$^3$ and $C_O$ is 10 µF and occupies 1.6 × 0.8 × 0.8 mm$^3$.

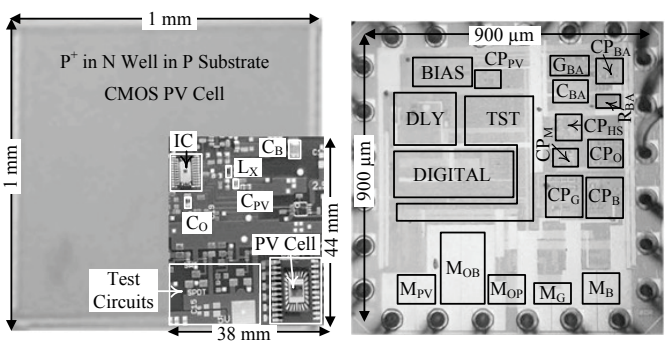


**Fig. 15**. PV-cell and charger–supply dies and test board.

### A. PV Power

The P$^+$ in N well on P substrate PV cell outputs up to 4, 27, and 131 µW with 1, 10, and 72 klx of light intensity like Fig. 3 shows. These maximum levels result when $v_{PV}$ is 420, 460, and 460 mV. But since $L_X$ draws discrete energy packets, $v_{PV}$ ripples about this optimum point. So like the histogram in Fig. 3 and waveform in Fig. 7 illustrate, $v_{PV}$ ripples from 442 to 476 mV with 72 klx. This small variation keeps $P_{PV}$ within 1% of $P_{MPP}$ in Fig. 3. The frequency of PV packets $f_{PV}$ is 10–120 kHz when $P_{PV}$ is 10–130 µW. Note that reducing $C_{PV}$ increases $v_{PV}$'s ripple, which increases $P_{PV}$'s deviation from $P_{MPP}$. In other words, a lower $C_{PV}$ reduces $P_{PV}$. But since sensitivity near $P_{MPP}$ is low, a higher $C_{PV}$ has little effect.

### B. Output Regulation

$L_X$ delivers 11-mA packets from the PV cell in Figs. 6 and 10 and 31-mA packets from the battery in Fig. 12. When over-sourced, $CP_{OS}$ keeps $v_O$ in Figs. 8 and 12 within ±28 mV of $v_R$'s 1 V. Output frequency $f_O$ in this mode is 8–53 Hz (when the load $P_{LD}$ in Fig. 11 is 10–110 µW). $G_{BA}$ keeps $v_O$ in Fig. 14 within ±4 mV of $v_R$. Overall, $CP_M$ keeps $v_O$ in Fig. 14 within +60 and –72 mV of $v_R$ when $P_{LD}$ suddenly changes 5 mW.

### C. Power Consumption and Conversion

Losses: Table I details how the system consumes power. PV and mode comparators $CP_{PV}$ and $CP_M$ and the bias block are always on, consuming 540, 630, and 810 nW. $L_X$'s $R_L$ burns 1.6 µW when over-sourced and loaded with 35 µW and burns 101 µW when battery-assisted and loaded with 5 mW. Switches burn 5.6 µW when similarly over-sourced and 142 µW when similarly battery-assisted. Ohmic power is generally higher when battery-assisted because the system transfers more power when loaded to the extent that assistance is needed.

$CP_{OS}$, $CP_O$, and $CP_B$ consume 560, 770, and 550 nW when over-sourced. $G_{BA}$, $CP_{BA}$, $CP_G$, and $CP_O$ dissipate 3.6, 6.7, 2.3, and 0.62 µW when battery-assisted. $G_{BA}$, $CP_{BA}$, and $CP_G$ are off when over-sourced and $CP_{OS}$ and $CP_B$ are off when battery-assisted. Battery-assisted components need more power because the system switches faster when battery-assisted, and to react quicker, components need more power.

TABLE I: Measured Losses

| | **Over-Sourced**: $P_{PV}$ = 70 µW, $P_{LD}$ = 35 µW | | **Battery-Assisted**: $P_{PV}$ = 70 µW, $P_{LD}$ = 5 mW | |
|---|---|---|---|---|
| | **Energy/Cycle** | **Avg. Power** | **Energy/Cycle** | **Avg. Power** |
| Bias | 12.5 pJ | 810 nW$^A$ | 15.6 pJ | 810 nW$^A$ |
| $CP_{PV}$ | 8.3 pJ | 540 nW$^A$ | 10.4 pJ | 540 nW$^A$ |
| $CP_M$ | 9.7 pJ | 630 nW$^A$ | 12.1 pJ | 630 nW$^A$ |
| $R_L$ | 24 pJ | 1.6 µW | 2.0 nJ | 101 µW |
| Switches | 85 pJ | 5.6 µW | 2.7 nJ | 142 µW |
| $CP_{OS}$ | 8.6 pJ | 560 nW | – | – |
| $CP_O$ | 12 pJ | 770 nW | 12 pJ | 620 nW |
| $CP_B$ | 8.4 pJ | 550 nW | – | – |
| $G_{BA}$ | – | – | 69 pJ | 3.6 µW$^A$ |
| $CP_{BA}$ | – | – | 130 pJ | 6.7 µW$^A$ |
| $CP_G$ | – | – | 44 pJ | 2.3 µW |
| **Total** | **169 pJ** | **11 µW** | **5.0 nJ** | **260 µW** |

$^A$Simulated values.

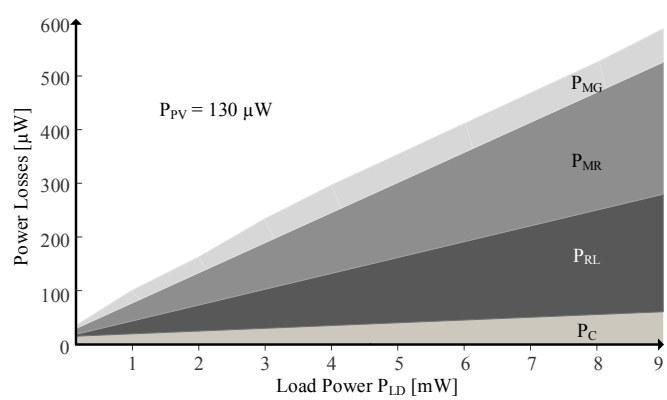


**Fig. 16**. Measured losses when battery-assisted.

Irrespective of the load $P_{LD}$, the system transfers PV power $P_{PV}$ when over-sourced. Losses therefore do not change much with $P_{LD}$ in this mode. Battery assistance, on the other hand, increases with $P_{LD}$. So ohmic losses in $L_X$'s $R_L$ and the switches $P_{RL}$ and $P_{MR}$ climb with $P_{LD}$ when battery-assisted like Fig. 16 shows. Gate-drive losses $P_{MG}$ also increase with $P_{LD}$ because transistors switch more often when they deliver more battery packets. Controller losses $P_C$ also climb because system components similarly activate more often.

When optimally sized, ohmic and charge losses $P_{MR}$ and $P_{MG}$ in a transistor balance. Here, however, $P_{MR}$ is greater than $P_{MG}$ because $P_{MR}$ also includes the ohmic power that bond wires dissipate. This difference is apparent because bond wires are nearly as resistive as switches in the network.

Efficiency: Power-conversion efficiency $\eta_C$ is the fraction of input power $P_{IN}$ that a system outputs with $P_O$. $P_{IN}$ ultimately supplies $P_O$ and losses in the system $P_{LOSS}$. $P_O$ is therefore the $P_{IN}$ that $P_{LOSS}$ does not dissipate, which is why $\eta_C$ ultimately hinges on fractional losses $P_{LOSS}/P_{IN}$:

$$\eta_C \equiv \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_{LOSS}} = \frac{P_{IN} - P_{LOSS}}{P_{IN}} = 1 - \frac{P_{LOSS}}{P_{IN}} . \quad (4)$$

The PV controller keeps the size of PV energy packets $E_{PV}$ constant and adjusts their frequency $f_{PV}$ to keep track of PV power $P_{PV}$. Ohmic, gate-drive, and controller losses $P_{RL}$ and $P_{MR}$, $P_{MG}$, and $P_C$ scale with $f_{PV}$ because switches and components engage only when delivering $E_{PV}$'s. Losses $P_{LOSS}$ therefore scale with the $f_{PV}$ that draws $P_{PV}$. So at any given load $P_{LD}$, both $P_{IN}$ and $P_{LOSS}$ scale with $P_{PV}$. This is why $\eta_C$ is fairly independent of $P_{PV}$ in Fig. 17.

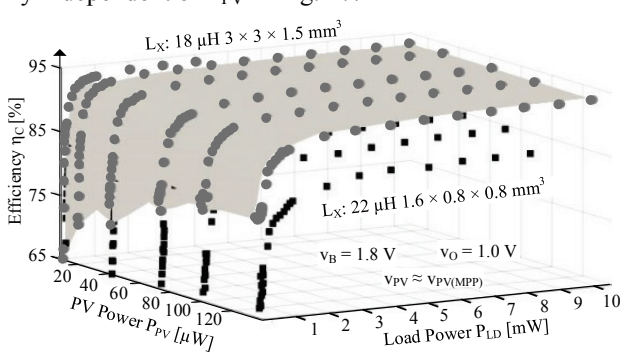


**Fig. 17**. Measured power-conversion efficiency.

When battery-assisted, $v_{PV}$ and $v_B$ supply $P_{IN}$ and the load sinks $P_O$. $P_{IN}$ therefore includes PV and battery power $P_{PV}$ and $P_B$, $P_O$ is the load $P_{LD}$, $P_{IN}$ supplies $P_{LD}$ and $P_{LOSS}$, and $\eta_C$ is

$$\eta_{C(BA)} = \left.\frac{P_O}{P_{IN}}\right|_{BA} = \frac{P_{LD}}{P_{PV} + P_B} = \frac{P_{LD}}{P_{LD} + P_{LOSS}} . \quad (5)$$

Since all losses scale with $P_{LD}$ in Fig. 16, $\eta_C$ in Fig. 17 is fairly constant across $P_{LD}$ in this mode (when $P_{LD}$ is 0.13–10 mW). $\eta_C$ is also high at 94.5% because all switches are optimally sized for the energy packets they deliver, system components activate only when needed, and the resistance of the 3 × 3 × 1.5-mm$^3$, 18-μH inductor used is only 1 Ω. $\eta_C$ falls to 87.8% when using a 1.6 × 0.8 × 0.8-mm$^3$, 22-μH inductor because, with less volume, resistance is 2× higher.

When over-sourced, $v_{PV}$ supplies $P_{LD}$ and recharges $v_B$. So $P_{IN}$ is $P_{PV}$, $P_O$ includes $P_{LD}$ and $P_B$, $P_O$ is the $P_{PV}$ that $P_{LOSS}$ does not dissipate, and $\eta_C$ is

$$\eta_{C(OS)} = \left.\frac{P_O}{P_{IN}}\right|_{OS} = \frac{P_{LD} + P_B}{P_{PV}} = \frac{P_{PV} - P_{LOSS}}{P_{PV}} . \quad (6)$$

Although the system transfers the same $P_{PV}$ that light intensity avails in this mode, $P_{LOSS}$ still changes with $P_{LD}$. This is because the power that $M_{OP1}$–$M_{OP2}$ in Fig. 4 steers into $v_O$ and $M_{B1}$ channels into $v_B$ vary with $P_{LD}$. So as $P_{LD}$ falls, $M_{OP1}$–$M_{OP2}$ burns less power, but not to the same extent that $M_{B1}$ burns more power. This is why $\eta_C$ in Fig. 17 falls to 64.3% with the larger $L_X$ and 54.2% with the smaller $L_X$ when $P_{LD}$ is below 130 μW, which is when the system is over-sourced. To improve efficiency in over-sourced mode the supply system switches only when $C_{PV}$ accumulates enough energy to reach $v_{MPP}$, $CP_{OS}$ remains on only when $L_X$ energizes and, $CP_O$ and $CP_B$ remains on only when $L_X$ drains to output or battery.

## V. Relative Performance

Table II summarizes the overall performance of this and other light-harvesting power-supply systems in literature. The system here uses a 14-mm$^3$ 22-μH inductor to draw up to 140 μW from a 1-mm$^2$ PV cell and supply up to 10 mW with 64.3%–94.5% efficiency. With a 1-mm$^3$ 18-μH inductor, efficiency is 54.2%–87.8%.

The switched inductor in [14] draws and supplies the same power, but with a 9.7× larger inductor, 38× larger PV cell, and 11% lower peak efficiency. The one in [24] supplies 20 mW with up to 95% efficiency, but with a 7.0× larger inductor and 740× larger PV cell. [13] uses a 14-mm$^3$ inductor to draw up to 100 μW, but only supplies up to 1 mW with 8% lower peak efficiency and a 9× larger PV cell. [15] does not report the size of the inductor or PV cell that were used to supply up to 1 μW. The switched capacitor in [12] uses a 0.07-mm$^2$ PV cell to only draw up to 80 nW and supply 90 nW.

$v_{PV}$'s and $v_O$'s capacitors $C_{PV}$ and $C_O$ are normally off-chip because on-chip capacitors are 2.5 nF/mm$^3$ [18] and off-chip capacitors can be 10 μF/mm$^3$. This is because the manufacturing process for off-chip capacitors is optimal for capacitors and that of on-chip capacitors is optimal for integrated circuits, not capacitors. Unfortunately, literature does not always report the dimensions of $C_{PV}$ and $C_O$. But since many off-chip capacitors occupy about 1 mm$^3$, assuming $C_{PV}$ and $C_O$ each occupies 1 mm$^3$ is reasonable.

Literature normally only quotes area for PV cells and silicon dies. This is because height is usually uniform and ultimately dictated by packaging. For the sake of comparison, normalizing cell and die height to 1 mm is reasonable.

When combining the volumes of the transfer inductor, PV cell, and integrated circuit and adding 1 mm$^3$ for $C_{PV}$ and another 1 mm$^3$ for $C_O$, the system prototyped here outputs 561 μW/mm$^3$ with the larger inductor and 2.08 mW/mm$^3$ with the smaller one. Whereas, [14], [13], and [24] output 55.2, 39.4, and 23.7 μW/mm$^3$. So the system here supplies 10× more power per cubic millimeter with 94.5% efficiency and 38× with 87.8% than the best light-harvesting microsystem reported. Effective power density is 3.8× higher in the latter

TABLE II: PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

| | JSSC '15 [14] | TPE '16 [13] | JSSC '16 [24] | JSSC '16 [15] | This Work |
|---|---|---|---|---|---|
| PV Cell | 24 × 1.6 $mm^2$ | 3 × 3 × 1 $mm^3$ | 24 × 31 $mm^2$ | | 1 × 1 × 1 $mm^3$ |
| IC Silicon Area | 2.15 × 2.15 $mm^2$ | 0.6 × 0.6 $mm^2$ | 0.9 × 0.9 $mm^2$ | 3 × 3 $mm^2$ | 0.9 × 0.9 $mm^2$ |
| Min. Channel Length | 180 nm | 180 nm | 500 nm | 180 nm | 180 nm |
| Transfer Inductor | 10 µH | 47 µH | 4.7 µH | | 18(22) µH |
| | 136 $mm^3$ | 14 $mm^3$ | 98 $mm^{3A}$ | | 14(1.0) $mm^3$ |
| | | 2 Ω | 20 mΩ | | 1(2) Ω |
| Battery Voltage | 3 V | 1.8 V | 3.3 V | 3.0 V | 1.8 V |
| PV Voltage | | 0.27–0.32 V | 1.5–5.5 V | 0.14–0.62 V | 0.42–0.46 V |
| PV Capacitor | | 220 nF | 4.7 µF | | 100 nF |
| | | 1.6 × 0.8 × 0.8 $mm^3$ | | | 1 × 0.5 × 0.5 $mm^3$ |
| PV Ripple | 10 mV | 30 mV | 20 mV | | 30 mV |
| PV Power | < 100 µW | < 100 µW | 40 µW | 50 nW–1 µW | 10–140 µW |
| Output Voltage | 1 V, 1.8 V | 1 V | 1–3.3V | 1 V | 1 V |
| Load Power | 1 µW–10 mW | 0–1 mW | 0–20 mW | | 0–10 mW |
| Static Output Ripple | 10 mV | 10 mV | 10 mV | 10 mV | 10 mV |
| Output Capacitor | 10 µF | 2.2 µF | 10 µF | | 10 µF |
| | | 1.6 × 0.8 × 0.8 $mm^3$ | | | 1.6 × 0.8 × 0.8 $mm^3$ |
| Load Dumps | | 0.10–1.0 mW | | | 0.10–1.0 mW |
| Dynamic Output Ripple | –?/+? mV | –24/+25 mV | –66/+33 mV | | –28/+28 mV |
| Controller Power | < 400 nW | 3–30 µW | 2.8 µW | 3.2 nW | 3–66 µW |
| Power-Conversion Efficiency | 68%–83% | 63%–86% | 80%–95% | 40%–87% | 64.3%–94.5% (54.2%–87.8%) |
| Effective Power Density[B] | 55.2 µW/$mm^3$ | 39.4 µW/$mm^3$ | 23.7 µW/$mm^3$ | | 561 (2080) µW/$mm^3$ |

[A]Estimate. [B]Max. Load Power ÷ Total Volume (of inductor, PV cell, IC silicon die, 1 $mm^3$ for the PV capacitor, and 1 $mm^3$ for the output capacitor).

because the 22-uH inductor used is 14× smaller than the 18-uH inductor in the former. Effective power density is higher here mostly because of integration: because the PV cell, power stage, and controller are all on chip.

Another key feature of this design that the table cannot describe very well is how efficiency scales with PV and load power $P_{PV}$ and $P_{LD}$. Like Fig. 17 shows, efficiency here is nearly 94.5% across $P_{PV}$'s 10–130-µW and $P_{LD}$'s 0.5–10-mW with the larger inductor and 87.8% with the smaller inductor. Like typical power supplies with small (lossy) inductors, efficiency in [12]–[15] and [24] peaks at one load level and drops with other loads. Efficiency here is constant because $CP_{OS}$, $G_{BA}$, and $CP_M$ regulate $v_O$ in such a way that $L_X$'s energy packets always carry the same energy. Typical control schemes [13]-[14] regulate $v_O$ in ways that do not achieve this.

## VI. CONCLUSION

The light-powered CMOS system presented here draws 10–130 µW from a 1 × 1-$mm^2$ PV cell and assistance from a battery to supply a 10-mW microsystem and recharge the battery with excess PV power. It outputs 10× more power per cubic millimeter than the best light-harvesting microsystem reported with 94.5% efficiency and 38× with 87.8%. Unlike others whose efficiencies peak at one power level, efficiency here is 94.5% across the cell's 10–130-µW and the load's 0.5–10-mW with a 3 × 3 × 1.5-$mm^3$ 18-µH inductor and 87.8% with a 1.6 × 0.8 × 0.8-$mm^3$ 22-µH inductor. The key enabling features are integration and energy management. Power switches are optimally sized, components activate only when needed, and the controller tracks power by adjusting frequency. Delivering more power with less space is vital because the mW's that wireless microsensors can demand can easily overwhelm the power that small onboard sources can sustain.

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