Light-Harvesting CMOS Power-Supply System for 0–10-mW Wireless Microsensors

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Abstract—Wireless microsensors in consumer products, homes, hospitals, and factories incorporate sensing, processing, and transmission intelligence that can save money, energy, and lives. Although their tiny batteries deplete quickly, harvesting light energy can replenish what they supply. Still, a 1-mm² PV cell can only generate up to 150 μW of the mW's that a wireless microsensor can consume. The battery-assisted light-powered harvester presented here therefore draws 10–130 μW from a 1 × 1-mm² PV cell and assistance from a battery to supply a 10-mW load and recharge the battery with excess PV power. The CMOS system regulates its 1-V output within ±28 mV while supplying 10× more power per 1 mm² with 94.5% efficiency and 38× with 87.8% efficiency than the best light-harvesting microsystem reported. Unlike others whose efficiencies peak at one power level, efficiency here is 94.5% across vPV's 10–130-μW and PLD's 0.5–10-mW with a 18-μH 3 × 3 × 1.5-mm³ inductor and 87.8% with a 22-μH 1.6 × 0.8 × 0.8-mm³ device.

Index Terms—Ambient light, energy harvester, photovoltaic (PV) cell, CMOS microsystem, switched-inductor converter, wireless microsensor, charger, and power supply.

I. LIGHT-HARVESTING MICROSYSTEMS

Advances in the semiconductor industry have made possible the integration of sensors, processors, memory, and transceivers into tiny wireless devices [1]–[3]. Powering these sensors over extended periods remains a challenge, however, because the tiny on-board batteries that these sensors can fit store little energy. Plus, the cost of personnel employed to replace these batteries is often prohibitive. Luckily, ambient light, motion, heat, and radiation can continually replenish the energy that these batteries supply [4]–[8].

Photovoltaic (PV) cells can generate 150 μW/mm² from sunlight. This is 100× more power than electrostatic or piezoelectric transducers can harvest from motion and thermoelectric generators can generate from heat [4]–[8]. Unfortunately, PV cells output 100× less power with artificial lighting than with sunlight. In other words, mm cells can generate a few μW's indoor and up to 150 μW outdoors.

Although transmissions can require mW's, microsensors seldom transmit in practice. In fact, many sensors mostly idle or sense, so on average they often consume nW's [3]. A system can therefore rely on a μW ambient source to replenish the energy that a battery loses to transmissions. For example [7] cites a pulse oxymeter sensor node that consumes 90 μW to process and transmit data every 15s. Similarly, the intraocular sensor node in [3] consumes 240 nW to measure eye pressure. This way, with the assistance of a battery, an ambient source can supply a wireless microsensor almost indefinitely. The battery supplies on demand what the PV cell avails over time, so light ultimately supplies the system.

The charger–supply system in Fig. 1, for example, harvests PV power Ppv from a PV source vPV. When the system idles, vPV can supply more power than the sensor system demands with Pld. The supply system therefore directs excess PV power to the battery vB. During a transmission, however, Ppv may be insufficient, so the system draws assistance from vB.

Fig. 1. Light-harvesting wireless microsensor.

The charger–supply [9]–[15] should therefore transfer power from vPV to the output VO and to vB and from vB to VO. It should do so with minimal losses and at the maximum power point [16]–[18]. Switched inductors are usually more efficient than switched capacitors because switched capacitors typically need more power-consuming switches [8], [19]. This paper therefore proposes a PV-sourced switched-inductor charger–supply system in Sections II–III whose CMOS implementation Section IV describes. Key aspects that distinguish this technology from the state of the art are integration (small size) and energy management (high power-conversion efficiency). Section V discusses how the prototype built compares with the state of the art. Section VI then draws relevant conclusions.

II. CMOS PV-SOURCED CHARGER–SUPPLY

A. CMOS PV Cell

PV cells are essentially PN junctions. In neutral conditions, charge carriers diffuse across the junction, leaving ionized parent atoms behind. So when photons liberate loosely bound electrons in this region, the electric field that these parent atoms establish pull electrons and the holes they leave behind across the region. The net result is a photonic current iPH.
The PN junctions that are normally available in standard CMOS technologies are shallow P+ regions in N well, N-well regions over a P substrate, and N+ regions over a P substrate. To stack cells over the same substrate, neither terminal can connect to the substrate. This is why only shallow P+ regions in an N well like Fig. 2 shows can stack. Unfortunately, these devices incorporate P′–N well–P substrate BJTs that leak too much power to the substrate [20]–[21].

Still, this device incorporates two PN junctions with separate depletion regions that together can collect more of the electron–hole pairs that photons liberate. By connecting the junctions in parallel, sunlight can generate more $i_{PH}$ [18]. The diodes that these PN junctions also establish, however, divert some $i_{PH}$ away as $i_{D}$. As a result, $v_{PV}$ outputs with $i_{PH}$ the difference $i_{PH} - i_{D}$.

The power that $i_{PH}$ generates $P_{PH}$ and the power that $i_{D}$ consumes $P_{D}$ both hinge on $v_{PV}$. So PV power $P_{PV}$ in Fig. 3 rises with $v_{PV}$ until $P_{D}$’s incremental loss $-\Delta P_{D}$ cancels $P_{PH}$’s gain $+\Delta P_{PH}$. The maximum power point $P_{MPP}$ happens when these incremental variations balance and increases with light intensity. The $v_{PV}$ that outputs $P_{MPP}$ can be 400–500 mV.

![Fig. 2. P’ in N well photovoltaic (PV) cell.](image)

![Fig. 3. Measured photovoltaic power and histogram in the system.](image)

**B. Power Stage**

The power stage should draw power from the PV cell $v_{PV}$ to feed the sensor system at $v_{O}$. Excess PV power should replenish the battery $v_{B}$. When PV power cannot sustain the sensor, the system should draw assistance from $v_{B}$. In other words, the power stage proposed draws power from $v_{PV}$ and $v_{B}$ and supplies $v_{O}$ and $v_{B}$, depending on operating conditions.

Although the sensor system consumes less power with a lower supply voltage $v_{O}$, the supply system and other analog electronics stop working below a headroom level that is often about 1 V [3]. Breakdown voltage, which in this case is 1.8 V, is another limit that constrains $v_{B}$. So the power stage proposed in Fig. 4 boosts $v_{PV}$’s 350–500 mV to $v_{O}$’s 1 V and $v_{B}$’s 1.8 V and bucks $v_{B}$’s 1.8 V to $v_{O}$’s 1 V.

Unfortunately, on-chip inductors usually suffer from low inductance $L_{X}$ and high resistance $R_{L}$. This is a double challenge because low $L_{X}$ holds less energy with a given current $i_{L}$. So $i_{L}$ is usually high, and with a high $R_{L}$, ohmic power is that much higher. A higher switching frequency $f_{SW}$ can keep $i_{L}$ from reaching such a high level. The problem with this is that controlling and switching the network at higher $f_{SW}$ requires more power. Luckily, commercially available off-chip inductors with $s_{L_{X}}$-to-$R_{L}$ ratios (i.e., quality factors) of 50–100 can be as small as $1 \text{ mm}^{2}$ [13]. But since they are still bulky, the system in Fig. 4 proposes to use only one inductor.

![Fig. 4. CMOS PV-sourced charger–supply stage.](image)

Inductors energize with positive voltages and drain with negative voltages. So with transistors $M_{PV1}$ and $M_{PV2}$ closed, $M_{G1}$ in Fig. 4 and Fig. 5 closes to magnetize $L_{X}$ from $v_{PV}$, $M_{G1}$ then opens and $M_{OP1}$–$M_{OP2}$ closes to apply the negative voltage that drains $L_{X}$ into $v_{O}$. If the load does not need energy, $M_{B1}$ closes instead to drain $L_{X}$ into $v_{B}$. But if the load still needs energy after draining $L_{X}$ into $v_{O}$, $M_{PV1}$–$M_{PV2}$ opens and $M_{OB}$ closes. With $M_{OB}$ closed, $M_{B1}$–$M_{B2}$ then closes to energize $L_{X}$ from $v_{B}$ into $v_{O}$ and $M_{G1}$–$M_{G2}$ later close to drain $L_{X}$ into $v_{O}$. $M_{G1}$–$M_{G2}$’s and $M_{B1}$–$M_{B2}$’s source terminals swap positions because current can flow in both directions.

MOSFETs burn ohmic power $P_{MR}$ and require gate-drive power $P_{MG}$ to switch. Since $P_{MR}$ and $P_{MG}$ both climb with longer channels, channel lengths in Fig. 2 are the shortest possible that can sustain 1.8 V. On the other hand, $P_{MR}$ falls and $P_{MG}$ rises with wider channels. So overall losses fall with wider transistors until the rise in $P_{MG}$ cancels the fall in $P_{MR}$. In other words, transistors consume the least power when their channels are optimally wide for the current they conduct.

This is why some transistors in Fig. 4 are in parallel. For example, $M_{B1}$ alone closes to drain $L_{X}$ into $v_{B}$ the energy that $v_{PV}$ supplies and $M_{B1}$ and $M_{B2}$ together close to energize $L_{X}$ from $v_{B}$ because $v_{B}$ delivers more power than $v_{PV}$. $M_{G1}$ alone closes to energize $L_{X}$ from $v_{PV}$ and $M_{G1}$ and $M_{G2}$ together close to drain $L_{X}$ into $v_{O}$ the energy that $v_{B}$ supplies for the same reason. $M_{PV2}$ is optimally sized to deliver PV power $P_{PV}$. But since $v_{PV}$ is always connected to $L_{X}$ when the system is over-sourced, $M_{PV2}$ does not require $P_{MG}$. So paralleling $M_{PV1}$ in this mode reduces resistance without sacrificing $P_{MG}$.

$M_{OP1}$ and $M_{OP2}$ are in series so their body diodes block one another. This way, body diodes cannot conduct current when the combined switch is off. With only one transistor, the bulk would connect to $v_{O}$ to keep the body diode from engaging when the switching node $v_{SWO}$ falls. This, however, keeps $v_{SWO}$ from climbing above $v_{O}$ to $v_{B}$ when directing $i_{L}$ to $v_{B}$.
To remain at the maximum power point \( P_{\text{MPP}} \) in Fig. 3, \( v_{\text{PV}} \) should be steady. Similarly, \( v_{\text{O}} \) should be steady for the wireless microsensor to operate optimally and reliably. The supply system, however, switches \( L_X \) between input and output terminals, so the current pulled from \( v_{\text{PV}} \) and steered into \( v_{\text{O}} \) change abruptly from zero to \( i_L \). The purpose of capacitors \( C_{\text{PV}} \) and \( C_{\text{O}} \) is to reduce the voltage fluctuations that these abrupt current changes produce.

Between transfers, remnant energy in \( L_X \) drains into parasitic switch-node capacitances \( C_{\text{SWP}} \) and \( C_{\text{SWO}} \) and cycle back to \( L_X \) in resonant fashion. \( L_X \) and \( C_{\text{SW}} \)'s exchange energy back and forth until resistances burn the energy. The purpose of \( M_{\text{NR}} \) is to burn this energy quickly so the oscillations and noise that \( L_X \) and \( C_{\text{SW}} \)'s would otherwise produce fade faster.

The controller decides which transistors to close. The controller also determines which energizing switches to open. Draining output switches, however, can open like diodes, when they stop receiving \( L_X \)'s current \( i_L \). For this, comparators \( C_{\text{PB}}, C_{\text{PO}}, \) and \( C_{\text{P}} \) open \( M_{\text{B1}}, M_{\text{OP1}}-M_{\text{OP2}}, \) and \( M_{\text{G1}}-M_{\text{G2}} \) when \( v_{\text{SWO}} \) falls below \( v_{\text{B}} \) or \( v_{\text{O}} \) or \( v_{\text{SWO}} \) rises above ground.

To save power, these comparators activate after the controller closes the switches and power off after the comparators open them. \( C_{\text{G}}, C_{\text{B}}, \) and \( C_{\text{O}} \) are trimmed so their offsets and delays balance to keep efficiency from suffering. Since \( M_{\text{G1}} \) is also an energizing switch when drawing PV power \( P_{\text{PV}} \), the controller opens \( M_{\text{G2}} \) when \( M_{\text{G1}} \) energizes.

III. CMOS CONTROLLER

The controller proposed in Fig. 6 draws enough power from the PV cell to keep \( v_{\text{PV}} \) near the maximum power point peak \( v_{\text{MPP}} \). It also steers enough of that power, and if necessary, additional power from the battery \( v_{\text{B}} \) to keep \( v_{\text{O}} \) near its 1-V target \( v_{\text{R}} \). In other words, the controller regulates \( v_{\text{PV}} \) and \( v_{\text{O}} \). \( v_{\text{PV}} \) is programmable with \( v_{\text{MPP}} \) and \( v_{\text{O}} \) with \( v_{\text{R}} \).

The controller decomposes into four sections: PV, output, mode, and logic control. When gate signals to the transistors that connect to \( v_{\text{SWP}} \) and \( v_{\text{SWO}} \) in Fig. 4 crisscross, switches close and the supply nodes to which they connect short-circuit. This is a problem that the logic avoids by inserting dead time between the gate signals of adjacent switches. The logic also includes drivers large enough and quick enough to drive the large capacitive gates that power transistors present.

The controller consumes quiescent power \( P_{\text{Q}} \) that climbs with switching frequency \( f_{SW} \). To limit this loss, \( f_{SW} \) should be low. Except, energizing and draining \( L_X \) across long periods delivers more power than the sensor system requires. So the charger–supply here draws and delivers infrequent energy packets that are large enough to sustain the system. In other words, \( L_X \) conducts discontinuously.

A. Photovoltaic Regulation

When open-circuited, the PV cell’s photonic current \( i_{\text{PV}} \) in Fig. 4 feeds parasitic diode \( D_{\text{PV}} \) until \( v_{\text{PV}} \) reaches 500–600 mV. At this level, \( i_{\text{PV}} \), and in consequence, \( P_{\text{PV}} \) are zero. The purpose of the PV controller in Fig. 6 is to draw enough power from \( v_{\text{PV}} \) to keep \( v_{\text{PV}} \) at the level that \( i_{\text{PV}} \) with \( v_{\text{PV}} \) output the highest power \( P_{\text{MPP}} \). In steady state, \( v_{\text{PV}} \) should be 350–500 mV [18].

Since transistors consume the least power when they conduct a particular current, the system draws PV energy packets \( E_{\text{PV}} \)’s that always peak to the same level. For this, \( L_X \) energizes across the 400 ns that the fixed-pulse block \( t_{\text{PE}} \) in Fig. 6 sets. \( M_{\text{PV1}}, M_{\text{G1}}, M_{\text{B1}}, \) and \( M_{\text{OP1}}-M_{\text{OP2}} \) in Fig. 4 are optimally sized to conduct this energy. The controller adjusts \( P_{\text{PV}} \) by adjusting the frequency \( f_{\text{PV}} \) of the packets.
For this, comparator CPV commands LX to draw an EPV when vPV surpasses its targeted maximum power-point peak vMPP. Drawing EPV (at 20 ms in Fig. 7) pulls vPV below vMPP. Excess iPV then charges CPV until vPV again surpasses vMPP, at which point CPV prompts LX to draw another packet that discharges CPV. vPV rises and falls this way about its optimal average level vPV(AVG). Although this rippling behavior shifts vPV from its absolute optimal setting, like the histogram in Fig. 3 shows, CPV limits the variation to such a degree that PPV is still within 1% of PMP.

Operationally, CPV sets a flip-flop whose output commands the logic to energize LX across the 400 ns that tPE sets. vMPP is the output of a lookup table that determines which setting is optimal for the light intensity received. The advantage of the look-up table over open-circuiting the PV cell to sense the cell’s state is that the latter cannot output vO with the targeted 1-V reference vR. So as long as the system load PLD discharges vO (between 14 and 1 ms), CPV commands the logic to energize LX across the 400 ns that tPE always energizes LX across the same 400 ns to 11 mA, LX’s iL falls more slowly when directed to vO (at 15 ms). Interestingly, vPV delivers more power to vO this way because LX drains into vO while still connected to vPV. But since the vMPP that light intensity sets does not change, the PV controller delivers packets to vO less often. This is why vO in Fig. 9 receives EPV’s every 11 µs and vB every 8.4 µs.

To keep noise from inadvertently tripping the comparator, CPV incorporates hysteresis. This means that vO does not stop receiving EPV’s until vO in Fig. 10 falls 28 mV below vR’s 1 V. Similarly, but in the opposite direction, vO does not begin to receive EPV’s until vO climbs 28 mV above vR’s 1 V. To save power, CPV only activates when the system is over-sourced, and only while energizing LX. Hysteresis is built into CPV and designed to be higher than 20 mV to suppress the effects of +/-5 m-V noise when tolerance is up to +/-50%.

Since vO’s 1 V is lower than vB’s 1.8 V, LX drains more slowly with vO than with vB. So although the PV controller’s fixed-pulse block tPE always energizes LX across the same 400 ns to 11 mA, LX’s iL falls more slowly when directed to vO (at 15 ms). Interestingly, vPV delivers more power to vO this way because LX drains into vO while still connected to vPV. But since the vMPP that light intensity sets does not change, the PV controller delivers packets to vO less often. This is why vO in Fig. 9 receives EPV’s every 11 µs and vB every 8.4 µs.

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is 60 µW. Lighter loads extend tOF more than excess PV power shortens tOR, so f0 similarly falls to 8 Hz with 110 µW.

Battery-Assisted: When PV power PPV is not enough to feed the sensor system, the logic automatically delivers vPV’s energy packet EPV to vO and another packet EB from vB. Transconductor GBA closes the feedback loop that determines how much additional power vB delivers.

Since transistors consume the least power when they conduct a particular current, the system draws energy packets that peak to the same level. For this, LX energizes across the time that the fixed-pulse block tBE in Fig. 6 sets. Since the load can pull up to 10 mW and the PV cell can only supply up to 130 µW, vB must be able to supply more power than vPV. This is why tBE is 300 ns longer than tRE, so LX can peak to 31 mA in Fig. 6, and with 31 mA, deliver a larger energy packet EB. MB1 and MB2, MG1 and MG2, and M0B in Fig. 4 are optimally sized for this energy level. The controller adjusts PB by adjusting the number of packets delivered between EPV’s.

To save power, GBA activates only when the system enters battery-assisted mode. Similarly, if one EB (when GBA’s high output resistance sets a low-frequency pole pEA that along with CO’s pole po can reduce the loop gain to 0 dB with 0° of phase margin. Although CBA pulls pEA to lower frequency, RBA current-limits the system is stable.

Comparing the transfer functions of (2) and (3), we see that the frequency of the output is proportional to the gain, which is independent of the load. Hence, we can use the transfer function to design a controller that will maintain the system in a steady-state condition. The controller is designed to have a gain of 1 and a phase margin of 45°.

C. Mode Regulation

Comparator CPm in Fig. 6 ultimately determines whether battery assistance is needed or not. In other words, CPm determines which mode of operation the system should adopt. For this, CPm compares vO to its targeted vR and incorporates hysteresis whose threshold limits are well above and well below the vO peaks that CPs and GBA produce when they regulate vO. So if EPV’s alone (when CPs regulates vO) cannot sustain the load PLD, excess PLD discharges CO from cycle to cycle. When vO reaches CPm’s lower threshold, CPm trips high into battery-assisted mode. Similarly, if one EB (when GBA regulates vO) oversupplies PLD, excess EB charges CO to CPm’s upper threshold, where CPm trips low into over-sourced mode.

Static and dynamic components ultimately dictate CPm’s hysteretic limits. Because when vO reaches CPm’s lower static threshold, the system does not respond until a propagation
delay later. As a result, \( V_O \) rises or falls an additional amount. This dynamic effect diminishes, however, with slow variations in \( V_O \). When load power \( P_LD \) in Fig. 14 suddenly falls from 5 mW to 50 \( \mu \)W, for example, excess battery power \( P_B \) charges \( C_O \) slowly until \( V_O \) reaches \( C_M \)'s upper 60-mV threshold. When \( P_LD \) suddenly rises back to 5 mW, however, excess \( P_LD \) discharges \( V_O \) so quickly that the system does not react until after \( V_O \) falls below the 60-mV threshold by another 12 mV.

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**B. Output Regulation**

\( L_X \) delivers 11-mA packets from the PV cell in Figs. 6 and 10 and 31-mA packets from the battery in Fig. 12. When over-sourced, \( CP_O \) keeps \( V_O \) in Figs. 8 and 12 within \( \pm 28 \) mV of \( V_R \). Output frequency \( f_O \) in this mode is 8–53 Hz (when the load \( P_LD \) in Fig. 11 is 10–110 \( \mu \)W). \( G_BA \) keeps \( V_O \) in Fig. 14 within \( \pm 4 \) mV of \( v_R \). Overall, \( C_M \) keeps \( V_O \) in Fig. 14 within +60 and –72 mV of \( v_R \) when \( P_LD \) suddenly changes 5 mW.

**C. Power Consumption and Conversion**

**Losses:** Table I details how the system consumes power. PV and mode comparators \( CP_PV \) and \( CP_M \) and the bias block are always on, consuming 540, 630, and 810 nW. \( L_X \)'s \( R_L \) burns 1.6 \( \mu \)W when over-sourced and loaded with 35 \( \mu \)W and burns 101 \( \mu \)W when battery-assisted and loaded with 5 mW. Switches burn 5.6 \( \mu \)W when similarly over-sourced and 142 \( \mu \)W when similarly battery-assisted. Ohmic power is generally higher when battery-assisted because the system transfers more power when loaded to the extent that assistance is needed.

\( CP_O \), \( CP_B \), and \( CP_A \) consume 560, 770, and 550 nW when over-sourced. \( G_BA \), \( CP_BA \), \( CP_A \), and \( CP_O \) dissipate 3.6, 6.7, 2.3, and 0.62 \( \mu \)W when battery-assisted. \( G_BA \), \( CP_BA \), and \( CP_A \) are off when over-sourced and \( CP_O \) and \( CP_B \) are off when battery-assisted. Battery-assisted components need more power because the system switches faster when battery-assisted, and to react quicker, components need more power.

**IV. PROTOTYPE IMPLEMENTATION**

The 1 \( \times \) 1-mm\(^2\) and 0.9 \( \times \) 0.9-mm\(^2\) CMOS dies in Fig. 15 integrate the PV cell, power transistors, and controller blocks in Figs. 2, 4, and 5. Test circuits and power passives \( L_X \), \( CP_V \), and \( C_O \) in Fig. 4 are off-chip on the two-layer board shown. \( L_X \) is either 18 \( \mu \)H with 1 \( \Omega \) of dc resistance and 3 \( \times \) 3 \( \times \) 1.5 mm\(^3\) in volume or 22 \( \mu \)H with 2 \( \Omega \) and 1.6 \( \times \) 0.8 \( \times \) 0.8 mm\(^3\). Although the former occupies more space, its resistance burns less power. \( C_P \) is 100 nF and occupies 1.0 \( \times \) 0.5 \( \times \) 0.5 mm\(^3\). \( C_O \) is 10 \( \mu \)F and occupies 1.6 \( \times \) 0.8 \( \times \) 0.8 mm\(^3\).

**A. PV Power**

The \( P \) in N well on P substrate PV cell outputs up to 4, 27, and 131 \( \mu \)W with 1, 10, and 72 klx of light intensity like Fig. 3 shows. These maximum levels result when \( V_{PV} \) is 420, 460, and 460 mV. But since \( L_X \) draws discrete energy packets, \( V_{PV} \) ripples about this optimum point. So like the histogram in Fig. 3 and waveform in Fig. 7 illustrate, \( V_{PV} \) ripples from 442 to 476 mV with 72 klx. This small variation keeps \( P_{PV} \) within 1\% of \( P_{MPP} \) in Fig. 3. The frequency of PV packets \( f_{PV} \) is 10–120 kHz when \( P_{PV} \) is 10–130 \( \mu \)W. Note that reducing \( C_P \) increases \( V_{PV} \)'s ripple, which increases \( P_{PV} \)'s deviation from \( P_{MPP} \). In other words, a lower \( C_P \) reduces \( P_{PV} \). But since sensitivity near \( P_{MPP} \) is low, a higher \( C_P \) has little effect.
Irrespective of the load $P_{LD}$, the system transfers PV power $P_{PV}$ when over-sourced. Losses therefore do not change much with $P_{LD}$ in this mode. Battery assistance, on the other hand, increases with $P_{LD}$. So ohmic losses in $L_X$’s $R_L$ and the switches $P_{RL}$ and $P_{MR}$ climb with $P_{LD}$ when battery-assisted like Fig. 16 shows. Gate-drive losses $P_{MG}$ also increase with $P_{LD}$ because transistors switch more often when they deliver more battery packets. Controller losses $P_{C}$ also climb because system components similarly activate more often.

When optimally sized, ohmic and charge losses $P_{MR}$ and $P_{MG}$ in a transistor balance. Here, however, $P_{MR}$ is greater than $P_{MG}$ because $P_{MR}$ also includes the ohmic power that bond wires dissipate. This difference is apparent because bond wires are nearly as resistive as switches in the network.

**Efficiency**: Power-conversion efficiency $\eta_C$ is the fraction of input power $P_{IN}$ that a system outputs with $P_O$. $P_{IN}$ ultimately supplies $P_O$ and losses in the system $P_{LOSS}$. $P_O$ is therefore the $P_{IN}$ that $P_{LOSS}$ does not dissipate, which is why $\eta_C$ ultimately hinges on fractional losses $P_{LOSS}/P_{IN}$:

$$\eta_C = \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_{LOSS}} = \frac{P_{IN} - P_{LOSS}}{P_{IN}} = 1 - \frac{P_{LOSS}}{P_{IN}}. \quad (4)$$

The PV controller keeps the size of PV energy packets $E_{PV}$ constant and adjusts their frequency $f_{PV}$ to keep track of PV power $P_{PV}$. Ohmic, gate-drive, and controller losses $P_{RL}$ and $P_{MR}$, $P_{MG}$, and $P_{C}$ scale with $f_{PV}$ because switches and components engage only when delivering $E_{PV}$’s. Losses $P_{LOSS}$ therefore scale with the $f_{PV}$ that draws $P_{PV}$. So at any given load $P_{LD}$, both $P_{IN}$ and $P_{LOSS}$ scale with $P_{PV}$. This is why $\eta_C$ is fairly independent of $P_{PV}$ in Fig. 17.

![Fig. 17. Measured power-conversion efficiency.](image)

When battery-assisted, $v_{PV}$ and $v_B$ supply $P_{IN}$ and the load sinks $P_O$, $P_{IN}$ therefore includes PV and battery power $P_{PV}$ and $P_B$. $P_O$ is the load $P_{LD}$, $P_{IN}$ supplies $P_{LD}$ and $P_{LOSS}$, and $\eta_C$ is

$$\eta_{C(BA)} = \frac{P_O}{P_{IN}} = \frac{P_{LD}}{P_{PV} + P_B} = \frac{P_{LD}}{P_{PV} + P_{LOSS}}. \quad (5)$$

Since all losses scale with $P_{LD}$ in Fig. 16, $\eta_C$ in Fig. 17 is fairly constant across $P_{LD}$ in this mode (when $P_{LD}$ is 0.13–10 mW). $\eta_C$ is also high at 94.5% because all switches are optimally sized for the energy packets they deliver, system components activate only when needed, and the resistance of the $3 \times 3 \times 1.5$-mm$^3$, 18-µH inductor used is only 1 Ω. $\eta_C$ falls to 87.8% when using a $1.6 \times 0.8 \times 0.8$-mm$^3$, 22-µH inductor because, with less volume, resistance is 2× higher.

When over-sourced, $v_{PV}$ supplies $P_{LD}$ and recharges $v_B$. So $P_{IN}$ is $P_{PV}$, $P_O$ includes $P_{LD}$ and $P_B$, $P_O$ is the $P_{PV}$ that $P_{LOSS}$ does not dissipate, and $\eta_C$ is

$$\eta_{C(OS)} = \frac{P_O}{P_{IN}} = \frac{P_{LD} + P_B}{P_{PV}} = \frac{P_{PV} - P_{LOSS}}{P_{PV}}. \quad (6)$$

Although the system transfers the same $P_{PV}$ that light intensity avails in this mode, $P_{LOSS}$ still changes with $P_{LD}$. This is because the power that $M_{O1}–M_{O2}$ in Fig. 4 steers into $v_O$ and $M_{B1}$ channels into $v_B$ vary with $P_{LD}$. So as $P_{LD}$ falls, $M_{O1}–M_{O2}$ burns less power, but not to the same extent that $M_{B1}$ burns more power. This is why $\eta_C$ in Fig. 17 falls to 64.3% with the larger $L_X$ and 54.2% with the smaller $L_X$ when $P_{LD}$ is below 130 µW, which is when the system is over-sourced. To improve efficiency in over-sourced mode the supply system switches only when $C_{PV}$ accumulates enough energy to reach $v_{MPP}$. $C_{POS}$ remains on only when $L_X$ energizes and, $C_{PO}$ and $C_{PB}$ remain on only when $L_X$ drains to output or battery.

V. RELATIVE PERFORMANCE

Table II summarizes the overall performance of this and other light-harvesting power-supply systems in literature. The system here uses a 14-mm$^3$ 22-µH inductor to draw up to 140 µW from a 1-mm$^3$ PV cell and supply up to 10 mW with 64.3%–94.5% efficiency. With a 1-mm$^3$ 18-µH inductor, efficiency is 54.2%–87.8%.

The switched inductor in [14] draws and supplies the same power, but with a 9.7× larger inductor, 38× larger PV cell, and 11% lower peak efficiency. The one in [24] supplies 20 mW with up to 95% efficiency, but with a 7.0× larger inductor and 740× larger PV cell. [13] uses a 14-mm$^3$ inductor to draw up to 100 µW, but only supplies up to 1 mW with 8% lower peak efficiency and a 9× larger PV cell. [15] does not report the size of the inductor or PV cell that were used to supply up to 1 µW. The switched capacitor in [12] uses a 0.07-mm$^2$ PV cell to only draw up to 80 nW and supply 90 nW.

$v_{PV}$’s and $v_{C}$’s capacitors $C_{PV}$ and $C_O$ are normally off-chip because on-chip capacitors are 2.5 nF/mm$^3$ [18] and off-chip capacitors can be 10 µF/mm$^3$. This is because the manufacturing process for off-chip capacitors is optimal for capacitors and that of on-chip capacitors is optimal for integrated circuits, not capacitors. Unfortunately, literature does not always report the dimensions of $C_{PV}$ and $C_O$. But since many off-chip capacitors occupy about 1 mm$^3$, assuming $C_{PV}$ and $C_O$ each occupies 1 mm$^3$ is reasonable.

Literature normally only quotes area for PV cells and silicon dies. This is because height is usually uniform and ultimately dictated by packaging. For the sake of comparison, normalizing cell and die height to 1 mm is reasonable.

When combining the volumes of the transfer inductor, PV cell, and integrated circuit and adding 1 mm$^3$ for $C_{PV}$ and another 1 mm$^3$ for $C_O$, the system prototyped here outputs 561 µW/mm$^3$ with the larger inductor and 2.08 mW/mm$^3$ with the smaller one. Whereas, [14], [13], and [24] output 55.2, 39.4, and 23.7 µW/mm$^3$. So the system here supplies 10× more power per cubic millimeter with 94.5% efficiency and 38× with 87.8% than the best light-harvesting microsystem reported. Effective power density is 3.8× higher in the latter.
because the 22-μH inductor used is 14× smaller than the 18-
μH inductor in the former. Effective power density is higher
here mostly because of integration: because the PV cell, power
stage, and controller are all on chip.

Another key feature of this design that the table cannot
describe very well is how efficiency scales with PV and load
power $P_{PV}$ and $P_{LD}$. Like Fig. 17 shows, efficiency here is
nearly 94.5% across $P_{PV}$’s 10–130-μW and $P_{LD}$’s 0.5–10-mW
with the larger inductor and 87.8% with the smaller inductor.
Like typical power supplies with small (lossy) inductors,
efficiency in [12]–[15] and [24] peaks at one load level and
drops with other loads. Efficiency here is constant because
$\text{CP}_O$, $\text{G}_{BA}$, and $\text{CP}_M$ regulate $V_O$ in such a way that $L_X$’s
energy packets always carry the same energy. Typical control
schemes [13]–[14] regulate $V_O$ in ways that do not achieve this.

VI. CONCLUSION

The light-powered CMOS system presented here draws 10–
130 μW from a 1 × 1-mm$^2$ PV cell and assistance from a
battery to supply a 10-mW microsystem and recharge the
battery with excess PV power. It outputs 10× more power per
cubic millimeter than the best light-harvesting microsystem
reported with 94.5% efficiency and 38× with 87.8%. Unlike
others whose efficiencies peak at one power level, efficiency
here is 94.5% across the cell’s 10–130-μW and the load’s 0.5–
10-mW with a 3 × 3 × 1.5-mm$^3$ 18-μH inductor and 87.8%
with a 1.6 × 0.8 × 0.8-mm$^3$ 22-μH inductor. The key enabling
features are integration and energy management. Power
switches are optimally sized, components activate only when
needed, and the controller tracks power by adjusting
frequency. Delivering more power with less space is vital
because the mW’s that wireless microsensors can demand can
easily overwhelm the power that small onboard sources can
sustain.

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TABLE II: PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

<table>
<thead>
<tr>
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<th></th>
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<tbody>
<tr>
<td>PV Cell</td>
<td>24 × 1.6 mm$^2$</td>
<td>3 × 3 × 1 mm$^3$</td>
<td>24 × 31 mm$^2$</td>
<td>1 × 1 × 1 mm$^3$</td>
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<tr>
<td>IC Silicon Area</td>
<td>2.15 × 2.15 mm$^2$</td>
<td>0.6 × 0.6 mm$^2$</td>
<td>0.9 × 0.9 mm$^2$</td>
<td>3 × 3 mm$^3$</td>
<td>0.9 × 0.9 mm$^2$</td>
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<tr>
<td>Min. Channel Length</td>
<td>180 nm</td>
<td>180 nm</td>
<td>500 nm</td>
<td>180 nm</td>
<td>180 nm</td>
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<tr>
<td>Transfer Inductor</td>
<td>10 μH</td>
<td>47 μH</td>
<td>4.7 μH</td>
<td>18(22) μH</td>
<td></td>
</tr>
<tr>
<td></td>
<td>136 mm$^3$</td>
<td>14 mm$^3$</td>
<td>98 mm$^3$A</td>
<td>14(1.0) mm$^3$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 Ω</td>
<td>20 mΩ</td>
<td>(2) Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery Voltage</td>
<td>3 V</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>3.0 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>PV Voltage</td>
<td>0.27–0.32 V</td>
<td>1.5–5.5 V</td>
<td>0.14–0.62 V</td>
<td>0.42–0.46 V</td>
<td></td>
</tr>
<tr>
<td>PV Capacitor</td>
<td>220 nF</td>
<td>4.7 μF</td>
<td>100 nF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.6 × 0.8 × 0.8 mm$^3$</td>
<td>1 × 0.5 × 0.5 mm$^3$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PV Ripple</td>
<td>10 mV</td>
<td>30 mV</td>
<td>20 mV</td>
<td>30 mV</td>
<td></td>
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<tr>
<td>PV Power</td>
<td>&lt; 100 μW</td>
<td>&lt; 100 μW</td>
<td>40 μW</td>
<td>50 nW–1 μW</td>
<td>10–140 μW</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>1 V, 1.8 V</td>
<td>1 V</td>
<td>1–3.3 V</td>
<td>1 V</td>
<td>1 V</td>
</tr>
<tr>
<td>Load Power</td>
<td>1 μW–0.1 mW</td>
<td>0–1 mW</td>
<td>0–20 mW</td>
<td>0–10 mW</td>
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<tr>
<td>Static Output Ripple</td>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
<td></td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>10 μF</td>
<td>2.2 μF</td>
<td>10 μF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.6 × 0.8 × 0.8 mm$^3$</td>
<td>1.6 × 0.8 × 0.8 mm$^3$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Dumps</td>
<td>0.10–1.0 mW</td>
<td>0.10–1.0 mW</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic Output Ripple</td>
<td>–24/+25 mV</td>
<td>–66/+33 mV</td>
<td>–26/+28 mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Controller Power</td>
<td>&lt; 400 nW</td>
<td>3–30 μW</td>
<td>2.8 μW</td>
<td>3.2 nW</td>
<td>3–66 μW</td>
</tr>
<tr>
<td>Power-Conversion Efficiency</td>
<td>68%–83%</td>
<td>63%–86%</td>
<td>80%–95%</td>
<td>40%–87%</td>
<td>64.3%–94.5% (54.2%–87.8%)</td>
</tr>
<tr>
<td>Effective Power Density$^b$</td>
<td>55.2 μW/mm$^3$</td>
<td>39.4 μW/mm$^3$</td>
<td>23.7 μW/mm$^3$</td>
<td>561 (2080) μW/mm$^3$</td>
<td></td>
</tr>
</tbody>
</table>

$^a$Estimate. $^b$Max. Load Power ÷ Total Volume (of inductor, PV cell, IC silicon die, 1 mm$^3$ for the PV capacitor, and 1 mm$^3$ for the output capacitor).
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