A High Efficiency WCDMA RF Power Amplifier with Adaptive, Dual-Mode Buck–Boost Supply and Bias-Current Control

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***Abstract*— Power efficiency during heavy- and light-loading conditions in wireless portable applications is critical for extended battery life. The power amplifier (PA), as it turns out, is often the most power-consuming block in the system and its efficiency is therefore the subject of growing interest. A 1.96 GHz, 25 dBm SiGe HBT WCDMA RF PA is presented and experimentally validated to show how PA efficiency is improved with a 0.5-µm CMOS dynamically adaptive, dual-mode buck-boost power supply and bias-current control circuit. The supply voltage and bias current are dynamically adjusted from 0.4 to 4.5 V and 25 to 220 mA, respectively, over an output power range of −50 to 25 dBm, meeting adjacent and alternate channel leakage ratio (ACLR) specifications with less than 10% of error vector magnitude (EVM). The average efficiency of the dynamically adaptive system (13.67%) was *seven times* better than the corresponding fixed-supplied, fixed-biased scheme (1.95%), with the same HBT PA.**

***Index Terms*— adaptive supply, PA, adaptive bias, battery life, dynamic supply, dynamic bias, stand-by performance, WCDMA.**

I. Introduction

HIGH efficiency during both heavy and light-to-moderate loads in portable battery-powered systems is critical for extended battery life. As such, point-of-load schemes and dedicated power supplies have and will continue to proliferate in next generation wireless systems [1]. In state-of-the-art code-division-multiple-access (CDMA) power management systems, as many as eleven different power supplies are used [2]. Incorporating additional intelligence (e.g., dynamically self-adjusting features) into already existing dedicated power supplies is only logical, and especially appealing to radio frequency (RF) power amplifiers (PAs) because of the power budget they command and consume. A comparative evaluation of state-of-the-art PA efficiency enhancement schemes with boost [3], buck [4], and buck-boost [5] power supplies are offered in [5].

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Extending battery life implies high power efficiency across all operational modes of the system, especially those that have high probability of occurrence like stand-by and idle, which is why low quiescent current is an important parameter [6]. Unfortunately, conventional pulse-width modulated (PWM) power supply circuits suffer from high switching power losses during light loading conditions, not to mention relatively high quiescent current flow, the latter of which results from the relative complexity of the supply. The driving novelty of this paper is the simultaneous use of (1) a dual-mode dynamic power supply circuit to decrease both switching losses and quiescent current flow during light loading conditions and (2) an adaptive PA bias-current generator to further reduce power losses in the PA itself, maintaining in the process high PA power efficiency over a wide output power range. The dual-mode buck-boost power supply operates under PWM control during moderate-to-high load levels and under pulse-frequency modulation (PFM) during light loading conditions, thereby decreasing the switching frequency and its associated power losses. As a result, average power efficiency and subsequently system battery life are improved.

II. The Proposed System

The biasing conditions of the proposed PA track the average power demands of the system, which are in turn set by an outer power control loop through a digital-signal processor (DSP), as shown in Fig. 1. The output of the DSP is decoded into an analog signal by a digital-to-analog (DAC) converter and fed into the power management unit. The supply and bias current of the proposed PA then dynamically decrease with falling output power levels, but only as much as linearity performance specifications will allow.

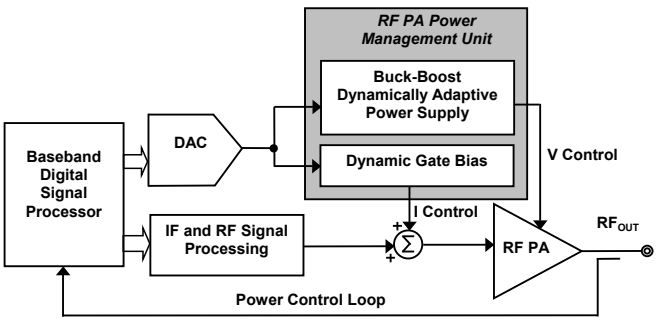


Fig. 1. Proposed dynamically adaptive RF PA power management system.

Simply stated, the output power transmitted to the load is the ratio of the square of peak output voltage V and load resistance R (V^2/R), as seen by the PA, where V is the voltage swing across the transistor's drain node. As the output power falls, the system proportionately decreases the PA's supply voltage from 4.5 to 0.5 V and bias current from 220 to 25 mA. The corresponding 5 to 25 dBm output power variation yields a power-control range of 20 dB, below which the PA supply and bias current are designed to remain unchanged. The power range is therefore partitioned in two, the dynamically adaptive high power region where a fast high power PWM DC-DC supply circuit is quick enough to track the 1-dB power step changes demanded by the base station's control signal and the constant low power region where a slow responding low power PFM DC-DC converter circuit supplies a steady, unchanging voltage. As the PA supply voltage traverses from 0.5 to 4.5 V, a noninverting buck-boost converter is needed to utilize the popular a Lithium-ion battery over its entire voltage range of 2.7 to 4.2 V. The dynamic power supply essentially operates in three regions: PFM buck (step-down) for low, PWM buck for moderate, and PWM boost (step-up) for high power levels.

III. Hardware Implementation

The proposed power management system was designed and fabricated using AMI's 0.5 μm CMOS process and then applied to a 1.96 GHz silicon-germanium (SiGe) hetero-junction bipolar transistor (HBT) WCDMA RF PA using an evaluation board from Sirenza Microdevices, as shown in Fig. 2. HBT_1 is the RF PA and HBT_2-HBT_3-R_{BIAS} combination comprise a β-helped Widlar current mirror, in other words, the dynamic current-driven bias-current generator circuit. The dynamic bias block is a transconductor whose input V_{CON} and therefore output current are proportional to the output power of the PA, as discussed in Section II.

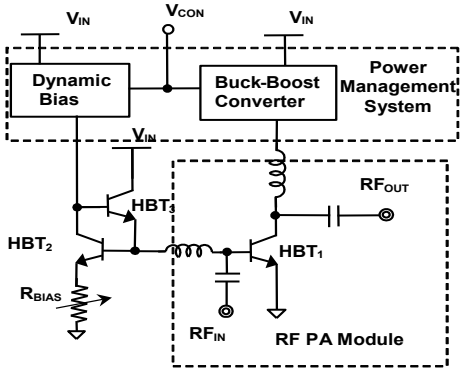


Fig. 2. Proposed embodiment of the dynamically adaptive voltage- and current-biased PA system.

The dynamically adaptive dual-mode buck-boost switching supply circuit is shown in Fig. 3. The power stage is comprised of a 1 μH power inductor, 20 μF output capacitor with an equivalent series resistance (ESR) of 10 mΩ, a 47 μF input capacitor with an ESR of 5 mΩ, and five integrated 0.5 μm power field-effect transistors (FETs) and their respective body diodes. The feedback loop is closed through a PWM or a PFM control path, depending on the output power level of the PA (i.e., MODE), via a multiplexing control-signal generator that introduces dead-time between switching transitions to prevent short-circuit conditions from occurring. A 2-zero/3-pole, type III external filter network is used to ensure the feedback control loop is stable across all possible operating conditions. Further details of the design and implementation of the dual-mode power supply, however, are not presented here for brevity, but [7] presents the relevant details of the circuit and its power efficiency performance.

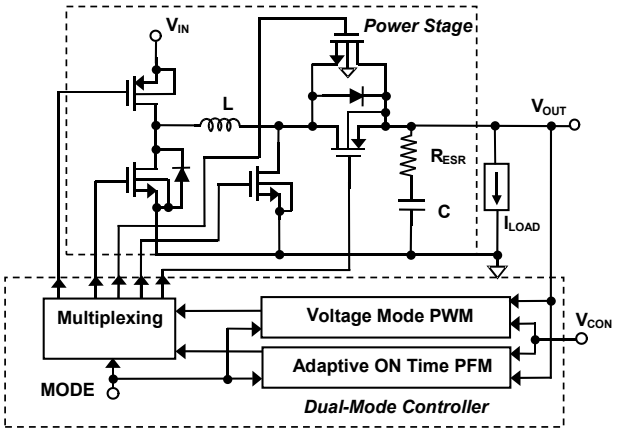


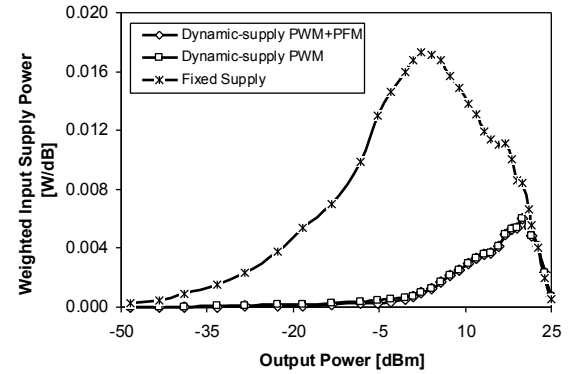
Fig. 3. Dual-mode buck-boost switching power supply prototype.

IV. Experimental Results and Discussion

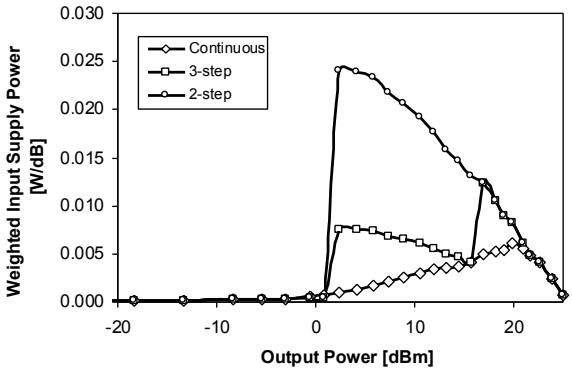
The dynamically adaptive PA system was tested with a 1.96 GHz center frequency, 3.84 MHz bandwidth, hybrid phase-shift keying (HPSK) modulated, wide-band code-division multiple access (WCDMA) signal. The measured adjacent and alternate channel leakage ratios of the PA were -35 and -58 dBc, respectively, satisfying WCDMA requirements. Over the transmitter's output power range, EVM degraded less than 10%, indicating in the process acceptable bit-error rate (BER) performance.

The average input supply power for the proposed dual-mode dynamically adaptive system, which is the area under the weighted input supply power trace [5] shown in Fig. 4(a), was significantly lower than its fixed supply counterpart. The weighting function applied is determined by the probability of occurrence of a given output power level. The resulting average power efficiency [5] of the dynamically biased PA with the dual-mode (PWM–PFM) DC-DC switching supply was *seven times greater* than in the fixed-supplied scheme, which translates to extended battery life.

In addition to continuously adapting the biasing point of the PA, a discrete two- or there-step approach [8] can be adopted for simplicity. For example, the entire output power range can be divided in two or three, each having a fixed pre-determined supply voltage. Although the PA would not *always* be ideally biased, its average power efficiency would increase with increasing quantizing levels, as validated with the experimental results shown in Fig. 4(b). Higher resolution improves overall PA efficiency, but of course, with increasing circuit complexity.



(a)



(b)

Fig. 4. Experimental weighted supply power profile performance as a function of output power for the proposed (a) continuous and (b) two- and three-step versions of the dynamically adaptive biasing scheme.

The overall PA efficiency of the HBT PA system with the dynamically adaptive buck-boost switching supply and bias-current control CMOS IC prototyped outperforms the state-of-the-art, when assuming the urban output transmitted power probability distribution of [5], as shown in Table I. A key feature of the proposed dual-mode control scheme is efficiency over a wide output power range, especially during light-to-moderate loading conditions, which is where probability of occurrence is highest. The two- and three-step control alternatives, although simpler to implement, are not nearly as power efficient as the continuous version. Even though a buck-boost converter is necessarily less efficient compared to a buck converter because of higher complexity, the proposed buck-boost supply outperforms the best reported buck-only approach is especially significant.

Battery life (normally in hours) is determined by the ratio of usable capacity (in Watt□hours) to the total average power, which includes both stand-by and active power. For the purpose of evaluating the proposed scheme against other state-of-the-art solutions, a reference battery capacity of 2,000 mW·h (e.g., 1.5 V and 800 mA·h) is assumed, while taking into account measured stand-by (quiescent) PFM and PWM currents of 140 μA and 800 μA, respectively. Consequently, the battery life of the proposed adaptive, dual-mode PA system is almost *twice* as long as the adaptive PWM-only PA supply system because of the lower power losses associated with the PFM circuit and the prevalence of the lower power levels of the urban probability distribution of transmitted output power.

TABLE I: COMPARING THE PROPOSED DYNAMICALLY ADAPTIVE DUAL-MODE PA SUPPLY WITH CONTINUOUS AND DISCRETE ADJUSTEMENTS WITH STATE-OF-THE-ART SOLUTIONS.

	PA Scheme	Maximum Output Power	Fixed-Supplied Efficiency	Dynamic-Supply Efficiency
Reported work	Buck conver ter supplied AlGaAs/InG aAs MESFET PA [4]	28 dBm	2.2%	11.2%
	Boost conve rter supplied GaAs MESFET PA [3]*	26 dBm	3.89%	6.38%
	Buck-boost converter supplied LDMOS PA [5]	27 dBm	1.53%	6.78%
This work	V-I Controlled, buck-boost converter supplied HBT PA (Continuous)	25 dBm	1.95%	13.67%
	V-I Controlled, b uck-boost converter supplied HBT PA (3 -step)	25 dBm	1.95%	7.87%
	V-I Controlled, b uck-boost converter supplied HBT PA (2 -step)	25 dBm	1.95%	3.24%

* Output power probability distribution profile used in [3] is different.

V. CONCLUSION

The key feature of the dynamically adaptive, dual-mode buck-boost PA-supplied system designed, built, evaluated, and presented in this paper is light-to-moderate power efficiency performance, which is critical in battery-powered wireless applications, given the preponderance of low power levels in portable electronics. The 1.96 GHz, 3.84 MHz baseband bandwidth, 25 dBm WCDMA RF PA with the 0.5 μm CMOS dual-mode power management IC prototype met all the linearity requirements of the system while simultaneously extending battery life *five times* over the fixed-supplied PA and *two times* over the PWM-only dynamically biased PA.

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