Stability and Design Limits of Hysteretic Current-Mode Switched-Inductor Converters

Carlos J. Solis, and Gabriel A. Rincón-Mora

Abstract—**Emerging wireless microsystems rely on tiny batteries and intermittent energy-harvesting sources for energy and power. To sense, process, and report numerous events across extended periods, they often idle and wake to full-power conditions. Their power supplies must therefore be compact and efficient and respond quickly to sudden wide load changes. Hysteretic current-mode switched-inductor dc–dc converters are good for this application space because they are compact, efficient, and fast. Although also widely stable, they are nevertheless subject to instabilities. This paper explains how input and output voltages and load dumps limit stability, and as a result, bandwidth and response time. Measurements of a 200-mA, 1-V, 0.18-µm CMOS hysteretic current-mode buck with 95% peak power-conversion efficiency show how increasing the load-dump step by 140 mA and decreasing the input voltage by 400 mV compromise stability.**

Index Terms— **Design, analysis, stability, high bandwidth, dc–dc power supply, and hysteretic current-mode control.**

I. Powering Wireless Microsystems

Emerging wireless microsystems sense, process, and report information that can save money, energy, and lives [1]. With so much functionality and so little space, however, their onboard batteries deplete easily. So to conserve energy, they idle when possible and wake only on demand, and often quickly and to high-power states. Power supplies must therefore be compact, efficient, and fast.

Switched-inductor dc–dc power supplies are popular in many applications because they can deliver over 90% of the power they draw [2–4]. When pulse-width-modulated (PWM), they normally require multiple switching cycles to respond and recover after sudden load dumps [5]. Hysteretic converters are faster because they can slew the inductor's current uninterruptedly until the current can satisfy the load and replenish the output capacitor [6]. Slewing the inductor this way is the fastest possible way that a switched inductor can respond to load variations.

Although already analyzed in different ways and from different perspectives in literature [7–9], stability requirements for these hysteretic power supplies remain largely algebraic, abstract, and theoretical (without experimental validation). This brief explains and demonstrates with experiments how those requirements relate to the inductor and the load dumps it supports. With this insight, a designer can more readily stabilize and identify under which operating conditions a hysteretic power supply will remain stable. To explain this, Sections 2–5 describe circuit operation, stability requirements, validating measurements, and relevant conclusions.

II. Hysteretic Current-Mode Converter

1. Operation

The hysteretic current-mode buck dc–dc converter in Fig. 1 closes a feedback loop that, in keeping output v_O near reference v_R, supplies the current that the load requires. Transconductor G_{OSC} is an oscillator that ripples inductor

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L_O's current i_L across a window that comparator CP_{OSC}'s hysteretic thresholds set and about a level that amplifier A_E dictates with v_{ERR}. So together, A_E compares v_O and v_R to generate an error v_{ERR} that adjusts the level about which G_{OSC} oscillates i_L to match and supply the current i_{LD} that the load demands.

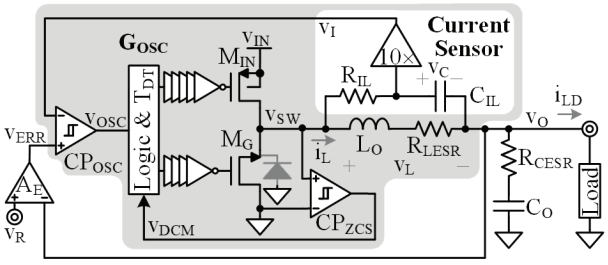

Fig. 1. Hysteretic current-mode buck.

The system delivers power by energizing and draining L_O from the input v_{IN} into v_O in alternating phases of the oscillating period t_{OSC}. When transistor M_{IN} energizes L_O with energizing voltage v_E or $v_{IN} - v_O$, i_L in Fig. 2 rises across energizing period t_E. i_L similarly falls when switch M_G drains L_O with drain voltage v_D or $-v_O$ across drain period t_D. i_L ripples this way about the load level the feedback loop sets with v_{ERR}.

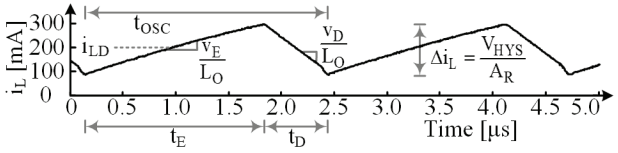

Fig. 2. Measured inductor current in continuous conduction mode (CCM).

When L_O's and C_{IL}'s corner frequencies with R_{IL} and R_{LESR} are well below the oscillating frequency f_{OSC}, sL_O and R_{IL} overwhelm R_{LESR} and $1/sC_{IL}$ near f_{OSC}. So L_O's voltage v_L is $i_L sL_O$, v_C is $v_L/sR_{IL}C_{IL}$ or $i_L L_O/R_{IL}C_{IL}$, and v_I is $i_L(10L_O/R_{IL}C_{IL})$ or $i_L A_R$ where current sense gain A_R equals:

$$A_R = \frac{v_I}{i_L} = 10\left(\frac{L_O}{R_{IL}C_{IL}}\right). \quad (1)$$

v_I therefore rises and falls with i_L, and when v_I reaches comparator CP_{OSC}'s upper threshold, CP_{OSC} trips low to open M_{IN} and close M_G, and that way, end t_E. The opposite happens when v_I falls to CP_{OSC}'s lower threshold to end t_D. i_L oscillates this way across the window that CP_{OSC}'s hysteresis V_{HYS} sets with V_{HYS}/A_R and about the level that v_{ERR} sets with v_{ERR}/A_R. Together, R_{IL}, C_{IL}, CP_{OSC}, M_{IN}, M_G, and L_O realize an oscillator G_{OSC} that oscillates i_L about i_{LD}.

When load current i_{LD} falls below half of i_L's ripple Δi_L, i_L can reverse, and that way, burn unnecessary power. Comparator CP_{ZCS} keeps this from happening by sensing and opening M_G when i_L reaches zero. In this way, like Fig. 3 shows, i_L falls to zero and remains at zero in discontinuous-conduction mode (DCM) until the next cycle. But since Δi_L is less than prescribed by V_{HYS}/A_R, v_O must rise above v_R to trip CP_{OSC}. In other words, v_O rises slightly when i_{LD} falls in DCM.

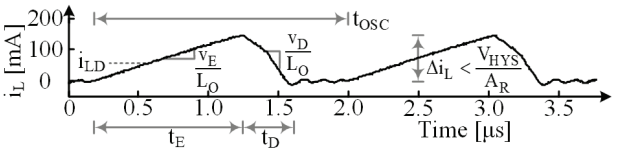

Fig. 3. Measured inductor current in discontinuous conduction mode (DCM).

2. Variants

The voltage-mode counterpart of the hysteretic current-mode buck is the most compact hysteretic buck because v_O and v_R feed directly into CP_{OSC} like Fig. 4 shows [10], without using A_E or a current sensor. Unfortunately, the circuit requires a resistive C_O, the equivalent series resistance (ESR) of which produces higher ripple in v_O. Adding a current sensor without gain and feeding its output v_I into CP_{OSC} remove this requirement [11–12]. This way, CP_{OSC} keeps v_O near v_R because v_I is $v_O + v_C$. v_C's $i_L L_O/R_{IL}C_{IL}$, however, appears as an offset in v_O. The purpose of A_E in Fig. 1 is to eliminate this offset. The state of the art adds peripheral blocks to Fig. 1 to keep the oscillating frequency constant [11–13]. These additions, however, do not alter the stability limits and effects of the hysteretic core.

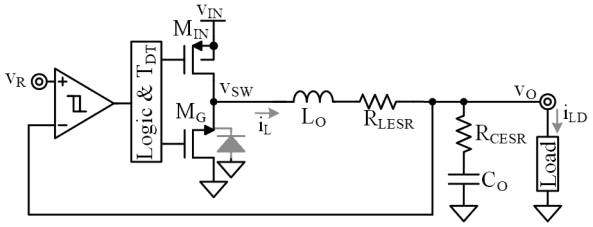

Fig. 4. Voltage-mode hysteretic control for buck converters.

Hysteretic current-mode boost and buck–boost configurations are also possible. What changes in these

configurations are the voltages v_E and v_D that energize and drain L_O. v_E, for example, is v_{IN} instead of $v_{IN} - v_O$, and v_D in the boost is $v_{IN} - v_O$ instead of just $-v_O$ [14]. So as long as the analysis is with respect to v_E and v_D, the mechanics explained here apply to all configurations. The output diode or switch in boost and buck–boost topologies, however, produce the effect of an out-of-phase, right-hand-plane (RHP) zero z_{RHP} that does not appear in buck converters [14]. But as long as the unity-gain frequency f_{0dB} is below z_{RHP}, which is a necessary requirement for these converters, all stability conditions are the same.

III. STABILITY

For the feedback loop that controls v_O to stabilize, the loop gain A_{LG} must reach unity (at f_{0dB}) with less than 180° of phase shift. Across the loop (in Fig. 5), G_{OSC}'s bandwidth establishes one pole p_G and output capacitor C_O shunts v_O to produce another pole p_O. C_O's series resistance R_{CESR} limits C_O's shunting current to eliminate the effects of p_O past zero z_{CESR}. But R_{CESR} for low-ripple applications is so low that z_{CESR} is negligibly high [15]. And C_O is so high that p_O is low and dominant. A phase margin of 45° balances speed and stability by limiting the number of damped oscillating rings to three or less [16]. So to maintain 45° of phase margin PM, f_{0dB} should be at or below p_G:

$$PM = 180^{o} - \mathrm{Tan}^{-1}\left(\frac{f_{0dB}}{p_O}\right) - \mathrm{Tan}^{-1}\left(\frac{f_{0dB}}{p_G}\right). \qquad (2)$$

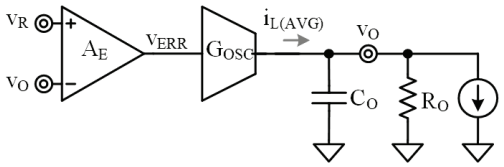

Fig. 5. System-level block diagram modeling current loop as transconductance G_{OSC}.

p_G is another way to quantify G_{OSC}'s delay time t_D [17]. In the case of hysteretic current-mode converters, t_D is the time L_O requires to slew i_L across a load dump Δi_{LD}. Because i_L climbs faster with higher L_O voltage v_L ($v_{SW} - v_O$ in Fig. 1), t_D is longer and p_G is lower when energizing and drain v_L voltages v_E and v_D are lower and Δi_{LD} is higher. And since i_L requires about four time constants $4\tau_G$ to reach 98% of its target, t_D is roughly $4\tau_G$ or τ_G is $t_D/4$ and p_G is no less than the lowest v_L and highest Δi_{LD} dictate:

$$p_G = \frac{1}{2\pi\tau_G} \approx \left(\frac{1}{2\pi}\right)\left(\frac{4}{t_D}\right) = \left(\frac{1}{2\pi}\right)\left(\frac{4}{\Delta i_{LD}}\right)\left(\frac{v_L}{L_O}\right). \qquad (3)$$

At worst case conditions, this yields:

$$p_{G(MIN)} = \frac{4\mathrm{Min}\left|v_E, v_D\right|}{2\pi\Delta i_{LD(MAX)} L_O}. \qquad (4)$$

In practice, the application defines v_{IN}, v_O, and Δi_{LD} and volume, power-rating, and conversion-efficiency constraints limit L_O. So for the fastest 45° response, C_O should be just high enough to define a p_O that keeps f_{0dB} near the minimum p_G or $p_{G(MIN)}$ that these parameters set. To quantify this, first consider that A_{LG} is the gain across A_E and G_{OSC} into the output impedance that R_O and C_O in parallel establish:

$$p_O = \frac{1}{2\pi R_O C_O} \qquad (5)$$

$$\begin{aligned} A_{LG} &= A_E G_{OSC}\left(R_O \parallel \frac{1}{sC_O}\right)\Bigg|_{p_O << f_{0dB} \le p_{G(MIN)}} \\ &\approx A_E G_{OSC0} R_O\left(\frac{p_O}{f_{0dB}}\right) \end{aligned}, \qquad (6)$$

where G_{OSC0} is G_{OSC}'s low-frequency translation $1/A_R$:

$$G_{OSC0} = \frac{i_l}{v_{err}} \approx \frac{1}{A_R}. \qquad (7)$$

Since p_G's effect on A_{LG} near f_{0dB} is small and A_{LG} at f_{0dB} is one, f_{0dB} is roughly equivalent to A_{LG}'s gain–bandwidth product:

$$\begin{aligned} f_{0dB} &\approx A_{LG0} p_O = \left(A_E G_{OSC0} R_O\right) p_O \\ &= \frac{A_E G_{OSC0} R_O}{2\pi R_O C_O} = \left(\frac{A_E}{A_R}\right)\left(\frac{1}{2\pi C_O}\right) \le p_{G(MIN)} \end{aligned}, \qquad (8)$$

where A_{LG0} is A_{LG}'s low-frequency translation $A_E G_{OSC0} R_O$. The Bode plot in Fig. 6 illustrates pole locations and the small-signal dynamics needed for stable conditions.

When worst-case extremes for v_{IN}, v_O, Δi_{LD}, and L_O in the buck of Fig. 1 are 1.1 V, 1 V, 150 mA, and 3.3 µH, v_E's $v_{IN} - v_O$ or 100 mV is lower than v_D's v_O or 1 V. So p_G

can be 130 kHz, and for 45° of phase margin, f_{0dB} should not exceed p_G's 130 kHz. C_O should therefore be no less than 15 µF when A_E is 12 V/V, R_{IL} is 33 kΩ, and C_{IL} is 1 nF, which means A_R is 1 Ω.

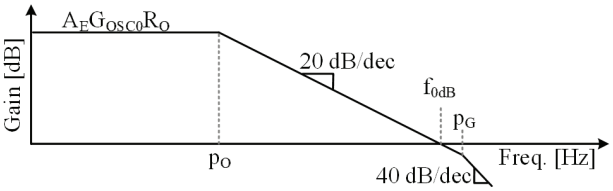

Fig. 6. Loop-gain response.

Relative to the state of the art, the analysis in [7] requires a model of the system in the form of complex state-space matrices. Although [8] and [9] decompose the system into transfer functions, their expressions are still complex. So drawing intuition to understand how each component in the system affects stability is challenging.

The analysis presented here is much easier to understand and implement. Expressions are insightful and correspond directly to components in the system. The analysis does not require state-space matrices. And thanks to its segmentation, the analysis is scalable with respect to additional gain stages with poles and zeros.

IV. PROTOTYPE

1. Hardware

The 0.6-mm^2 0.18-µm CMOS die in Fig. 7 integrates the error amplifier A_E, oscillating comparator CP_{OSC}, dead-time logic, power transistors M_{IN} and M_G and their drivers, and zero-current sensing comparator CP_{ZCS}. The current sensor, inductor L_O, and output capacitor C_O are off chip on the two-layer board alongside test circuits used for experiments. L_O and C_O measure 10.7 × 10 × 5.4 and 1.6 × 0.81 × 0.91 mm^3 and incorporate 15 and 4 mΩ, respectively.

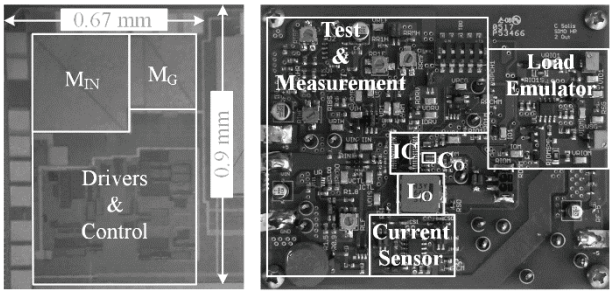

Fig. 7. Prototyped 0.18-µm CMOS die and two-layer board.

Fig. 8 shows the average output voltage v_O across load level i_{LD} at two input voltage v_{IN} operating points. v_O decreases with increasing i_{LD} due to its finite output resistance at a rate, i.e. load regulation, of 77 mV/A. Across the same loading, the worst-case output voltage difference Δv_O is 1.4 mV which results in a line regulation of 4.7 mV/V.

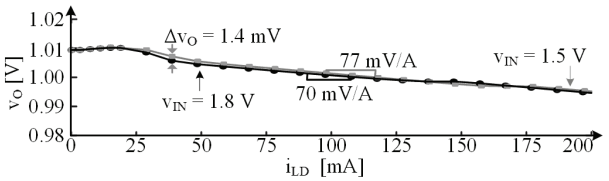

Fig. 8. Measured output voltage regulation across output load and input voltage.

2. Response

The measured output v_O in Fig. 9 ripples 5 to 10 mV and responds within 5.6 µs to rising 40-, 80-, and 180-mA load dumps. Response time t_R is basically how long L_O requires to slew i_L across these load steps. The system responds faster (within 3.4 µs) to similar falling load dumps because L_O's drain voltage v_D is higher at v_O's 1.0 V than L_O's energizing counterpart v_E, which is $v_{IN} - v_O$ or 1.5 – 1.0 V, which is 0.5 V.

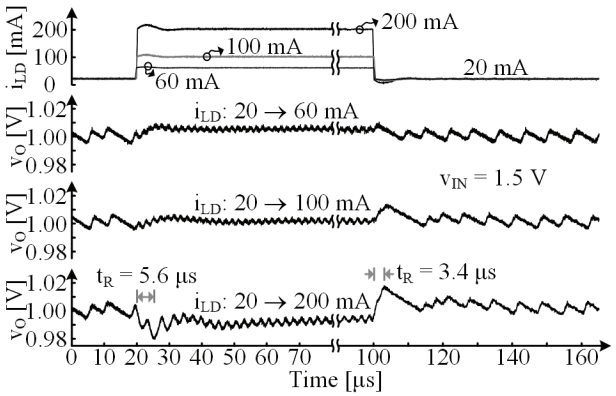

Fig. 9. Measured response to 40-, 80-, and 180-mA load dumps.

Phase margin essentially quantifies the propensity of a feedback loop to oscillate when perturbed. In this case, v_O in Fig. 5 is more prone to ringing when responding to rising than to falling load dumps. This is because L_O requires more time to respond to rising loads. In other words, the bandwidth pole of the oscillator is lower, and as a result, closer to the unity-gain frequency f_{0dB} of the loop. Similarly, the ringing worsens as the load step

increases from 40 to 180 mA because L_O requires more time to slew across wider load steps. Ringing also worsens as input voltage falls in Fig. 10 from 1.8 to 1.4 V for the same reason, because with a lower voltage across L_O, i_L slews more slowly.

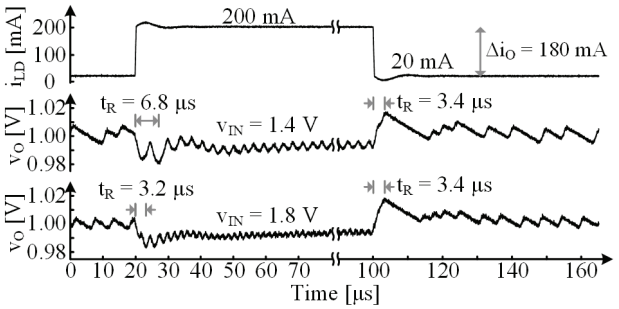

Fig. 10. Measured load-dump response when the input is 1.4 and 1.8 V.

Using equations (2)–(8), phase margins for 40-, 80-, and 180-mA load dumps are 75°, 62° and 40°, respectively. These calculated margins correspond well with Fig. 9. The 40-mA load dump response, for example, is closer to the over-damped response that 90° produces. The under-damped response to the 180-mA load dump rings 2–3 times before settling. This corresponds to the response that 45° produces.

3. Efficiency

A_E, CP_{OSC}, CP_{ZCS}, M_{IN}, M_G, the drivers, and dead-time logic consume quiescent, ohmic, and switching power P_Q, P_R, and P_{SW}. As load current i_{LD} climbs, output power P_O increases linearly, whereas P_R rises quadratically. Up to at least 200 mA, however, P_O outpaces P_R, so power-conversion efficiency η_C in Fig. 11 generally increases with i_{LD}. Although P_R is very low below 5 mA, P_O is also low, so P_Q and P_{SW} become large fractions of P_O. This is why η_C drops below 88% abruptly when i_L is less than 5 mA.

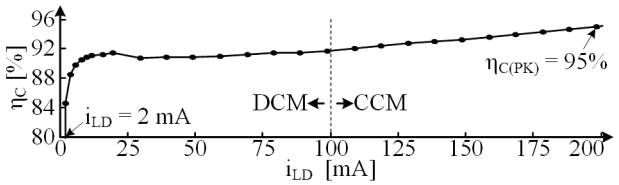

Fig. 11. Measured power-conversion efficiency.

V. CONCLUSIONS

Hysteretic current-mode converters are compact, fast, and efficient, but although widely stable, not immune to instabilities. The bandwidth delay of the oscillating current loop unfortunately introduces a secondary pole that falls with lower inductor voltages and higher load-dump currents. This is why the 200-mA, 1-V, 0.18-µm CMOS buck prototyped here responds more slowly to rising than to falling load dumps and rings more with lower input voltages and higher load steps. Understanding these stability limits is critical when designing hysteretic current-mode power supplies, which given their size, speed, and efficiency benefits, are increasingly prevalent in consumer electronics.

ACKNOWLEDGMENTS

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