A 1.1 V Current-Mode and Piecewise-Linear Curvature Corrected Bandgap Reference

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Abstract

A low voltage, micro-power, curvature-corrected bandgap reference is presented that is capable of working down to input voltages of 1.1 V in a relatively inexpensive process, MOSIS 2 μm technology. This is a vanilla N-well CMOS process technology with an added P-base layer. Second order curvature correction for this reference is accomplished by a versatile piecewise-linear current-mode technique. The 0.595 V precision reference achieved a line regulation performance of 408 ppm/V for input voltages between 1.2 and 10 V. The circuit only used 14 μA of quiescent current flow.

I. Introduction

Reference circuits are necessarily present in many applications ranging from purely analog, mixed-mode, to purely digital circuits. The demand for low voltage references is especially apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops [1]. Consequently, low voltage and low quiescent current flow are intrinsic and required characteristics conducive toward increased battery efficiency and longevity [2]. Low voltage operation is also a consequence of process technology. This is because isolation barriers decrease as the component densities per unit area increase thereby exhibiting lower breakdown voltages [3, 4]. By the year 2004, the power supply voltage is expected to be as low as 0.9 V in 0.14 μm technologies [4, 5]. Unfortunately, this leads to lower dynamic range [6]. As a result, maintaining high dynamic range while operating at reduced power supply voltages demands that the reference circuitry be more accurate. Furthermore, financial considerations also require that these circuits be realized in relatively simple processes, such as standard CMOS, bipolar, and stripped down biCMOS technologies [7].

II. Curvature Correction Method

2.1 Operation

Curvature correction is based on the addition of a nonlinear component to the output of a first order bandgap reference. This is used to offset the nonlinear behavior of V_{be} with respect to temperature [8, 9]. The nonlinear component, in this case, is realized by I_{NL} in the current-mode topology of the circuit described in Figure 1 (a). It is basically a current-mode piecewise-linear form of compensation. The essence of the circuit centers on current subtraction and the characteristics of non ideal transistors. Figure 1 (b) graphically illustrates the operation of the circuit throughout the temperature range. Transistor Mp1 acts like a non ideal current source of a current that is proportional to a base-emitter voltage. For the lower half of the temperature range, the PTAT current (I_{PTAT}) is less than the supplied V_{be} dependent current (I_{Vbe}), if MP1 operates in saturation. As a result, Mp2 is off and Mp1 operates in the linear region and provides only I_{PTAT}. For the upper half of the temperature range, however, I_{PTAT} becomes larger than I_{Vbe}. Consequently, Mp1 becomes saturated and only supplies I_{Vbe} while Mp2 sources the current difference. The resulting current through Mp3 is nonlinear, off during the first half of the temperature range and on during the latter half. This behavior can be described by

$$I_{NL} = \begin{cases} 0 & I_{Vbe} \geq I_{PTAT} \\ K_1 I_{PTAT} - K_2 I_{Vbe} & I_{Vbe} < I_{PTAT} \end{cases}, \quad (1)$$

where K_1 and K_2 are constants defined by mirror ratios.

Curvature correction is achieved by combining the three temperature dependent elements of Figure 1 (b) to yield an output voltage with reduced temperature drift. This is done by partitioning the temperature range in two, the range for which the nonlinear current component is (1) zero and (2) non-zero. As a result, the reference voltage (V_{ref}) can be temperature compensated to exhibit a behavior that is graphically described by Figure 2 (a) and (b). The lower temperature range is essentially a first order bandgap, since the nonlinear component (I_{NL}) is zero. At higher temperatures, the resulting behavior is similar to that of the lower temperatures but the operation is not. The nonlinear behavior of I_{NL} ($K_1 I_{PTAT}$ - $K_2 I_{Vbe}$) attempts to diminish the nonlinear term of I_{Vbe}. Consequently, the addition of currents AI_{Vbe}, BI_{PTAT}, and CI_{NL}, at the upper temperature range, generate a curvature corrected trace whose behavior is depicted by V_{ref} in Figure 2 (b).

2.2 Implementation

The current-mode approach adopted is complemented with a voltage-mode ladder for improved versatility. Figure 3 illustrates the implementation. The current-mode approach offers the possibility of lower reference voltages, while the voltage-mode ladder gives greater temperature compensation maneuverability. The voltage ladder, in this case, is consistent with low voltage since the absolute voltage across all the resistors is small, i.e., 0.2 - 0.6 V across the complete ladder. Hence, a low voltage reference can be designed whose individual temperature components can be optimized during the trimming process. The resulting relation of the reference voltage (V_{ref}) can be described by

$$V_{ref} = AI_{V_{be}}[R_1 + R_2 + R_3] + BI_{PTAT}[R_1 + R_2] + CI_{NL}R_1, \tag{2}$$

where I_{Vbe}, I_{PTAT}, and I_{NL} correspond to the base-emitter, PTAT, and nonlinear temperature dependent currents respectively.

2.3 Trimming Procedure

The topology illustrated in Figure 3 offers greater temperature compensation flexibility than a strictly current or voltage mode topology. The output voltage as well as the temperature coefficients of the individual components can be trimmed by simply changing the resistor ratios at the output. Temperature compensation is achieved by trimming throughout the temperature range. Data points are collected for the voltages at V_{ref}, node "a," and node "b" throughout the temperature sweep. At this point, the currents multiplied by an initial reference resistor can be extrapolated since the voltage across each resistor and corresponding initial resistor ratios are known; thus,

$$AI_{V_{be}}R_{2_{initial}} = \frac{V_{ref} - V_a}{\left\langle \frac{R_3}{R_2} \right\rangle_{initial}}, \tag{3}$$

$$BI_{PTAT}R_{2_{initial}} = \langle V_a - V_b \rangle - AI_{V_{be}}R_{2_{initial}}, \tag{4}$$

and $$CI_{NL} R_{2_{initial}} = \frac{V_b}{\left\langle \frac{R_1}{R_2} \right\rangle_{initial}} - \langle V_a - V_b \rangle, \quad (5)$$

where V_a and V_b correspond to the voltages at nodes "a" and "b." Voltages $I_{Vbe}R_{2initial}$ and $I_{PTAT}R_{2initial}$ exhibit the temperature characteristics of V_{be} and V_{PTAT}. Although the temperature coefficient (TC) of the internal resistors affects V_{be}, the temperature dependence of the resistors in the output ladder is minimized by using the same type of resistors. This is because I_{Vbe} and I_{PTAT} are defined by resistors that are of equal type as those used in the output resistor ladder, i.e.,

$$\frac{\partial}{\partial T}\langle AI_{V_{be}} \cdot R_{out} \rangle = \frac{\partial}{\partial T}\left\langle \frac{AV_{be}}{R(T)} \cdot R_{out}(T) \right\rangle \approx \frac{\partial}{\partial T}\langle AV_{be} \cdot Constant \rangle. \quad (6)$$

This is based on the assumption that the temperature characteristics of the resistors track. If this is the case, then the effect of the resistors' TC on V_{be} is compensated by the trimming procedure. The coefficients of each component can thus be extracted and manipulated to yield proper temperature compensation by means of a computer. Equation (2) can be adjusted to illustrate the appropriate temperature coefficients by using the values derived in equations (3) through (5),

$$V_{ref}\frac{R_{2_{initial}}}{R_2} = AI_{V_{be}}\left\langle \frac{R_1}{R_2} + \frac{R_2}{R_2} + \frac{R_3}{R_2} \right\rangle R_{2_{initial}} +$$

$$BI_{PTAT}\left\langle \frac{R_1}{R_2} + \frac{R_2}{R_2} \right\rangle R_{2_{initial}} + CI_{NL}\left\langle \frac{R_1}{R_2} \right\rangle R_{2_{initial}}, \quad (7)$$

or $$V_{ref}\frac{R_{2_{initial}}}{R_2} = D_1 AI_{V_{be}} R_{2_{initial}} + D_2 BI_{PTAT} R_{2_{initial}} + D_3 CI_{NL} R_{2_{initial}} \quad (8)$$

where D_1, D_2, and D_3 are the extracted coefficients. Once values for these coefficients are obtained, new resistor ratios for R_1/R_2 and R_3/R_2 can be derived.

The next and final step in the trimming procedure is to adjust the magnitude of the output voltage at room temperature or whatever temperature is desired. This can be accomplished by changing the ratio of the initial to the final value of R_2 ($R_{2initial}/R_2$). The ratio is determined by using the resistor ratios previously derived and the voltages obtained at room temperature (V_{ref}, $AI_{Vbe}R_{2initial}$, $BI_{PTAT}R_{2initial}$, and $CI_{NL}R_{2initial}$) in equations (7) and (8) and solving for $R_{2initial}/R_2$. It is noted that knowledge of the absolute value of the resistors is not necessary. Instead, the intrinsic parameters that require control are the ratios of the resistors. It is imperative that the resistors used before and after trimming be the same type as the resistors used to define I_{Vbe} and I_{PTAT} to preserve the temperature profile of V_{be} and the non-linear behavior of I_{NL}. The trimming algorithm has been successfully implemented by a spreadsheet. The procedure can be simplified by measuring V_a, V_b, and V_{ref} with one current source enabled at a time. This eliminates the need to know the initial resistor ratios. However, this method would suffer from lambda effect errors (finite output resistance). The magnitude of the error can, in some cases, be significant enough to notably change the overall accuracy performance of the reference.

III. Circuit Realization

The implementation of the overall circuit is illustrated in Figure 4. The circuit is fabricated in the MOSIS 2 μm N-well CMOS technology with an added P-base layer. The pre-regulated voltage ($V_{pre\text{-}reg}$) stays approximately constant at $2V_{be}$ for input voltages (V_{in}) greater than 1.25 - 1.3 V. When V_{in} falls below this point, the regulator goes into drop-out ($V_{pre\text{-}reg} \approx V_{in} - r_{sd\text{-}on}I_{quiescent}$). Large resistors are necessary and consistent for micro-power design methodologies where quiescent current flow is kept under 20 μA. The resistors can be significantly reduced by allowing more quiescent current to flow. The passive components and the JFET were implemented discretely to enhance testability of the concept. The only purpose of the JFET is to provide some current for the start-up circuit to work, i.e., 0.5 - 5 μA. All the resistors can be made of any material as long as they are all the same type. Base-diffusion resistors (typically having high TCs) can be used to exploit their high sheet resistivities but resistors with low TCs are recommendced. High TCs can significantly alter the temperature profile of V_{be}, which, in turn, affects the drift performance of the overall reference.

The minimum input voltage of the circuit is defined by a source-to-gate voltage and two saturation voltages. In particular, the input voltage is limited by

$$V_{in} \geq V_{ce\text{-}sat} + V_{sg} + V_{sd\text{-}sat}, \quad (9)$$

which can be approximately 1.1 V under weak-to-moderate inversion in the MOSIS technology. The circuit is biased in this region to minimize quiescent current flow and the effects of threshold voltages on the minimum input voltage. This minimum voltage is expected to be approximately 0.95 - 1 V in a process where a buried layer is offered. The buried layer reduces the NPN collector series resistance thereby decreasing the NPN saturation voltage ($V_{ce\text{-}sat}$) from approximately 300 to 150 - 200 mV.

IV. Experimental Results and Discussion

The temperature dependence of the reference voltage is illustrated in Figure 5. The 0.595 V reference achieved a temperature drift of less than 20 ppm/°C (-15 to 90 °C). The trimming scheme included the algorithm described earlier in the text. The circuit achieved a line regulation performance of 408 and 2000 ppm/V for $1.2 \leq V_{in} \leq 10$ V and $1.1 \leq V_{in} \leq 10$ V respectively (shown in Figure 6) with a maximum quiescent current flow of 14 μA (excluding the JFET's current). The circuit operated properly at a minimum power supply voltage of 1.1 V. The temperature dependence and the line regulation of the output simulated to be 6.5 ppm/°C and 120 ppm/V, respectively. The measured temperature performance could have been closer to the simulated value were it not for the parasitic effects of the start-up circuit. Leakage current out of the start-up circuit directly affects the output PTAT current component causing undesired changes in the output voltage. A summary of the results is shown in Table 1.

The temperature drift profile exhibited some evidence of noise in the form of large locally isolated slopes. This jagged response occurs because the reference voltage node has large output resistance. This characteristic impedance and the low quiescent current flow nature of the circuit make the reference inherently noisy. As a result, the temperature drift performance claim of better than 20 ppm/°C is approximately 33 % worse than the actual value measured. The temperature coefficient is

measured by the popular "box-method," where the extreme data points obtained in a measurement define the voltage drift across a given temperature range.

V. Conclusion

A low voltage, micro-power curvature-corrected bandgap circuit has been fabricated in a relatively inexpensive process, MOSIS CMOS 2 μm N-well technology with an added P-base layer. The P-base layer is used to create NPN transistors. However, a vanilla CMOS version of the circuit can also be designed by using lateral PNP transistors and/or junction diodes readily available in the process. The circuit implements a novel current-mode piecewise-linear curvature correction technique. The precision reference achieved a line regulation performance of 408 ppm/V for input voltages between 1.2 and 10 V at a maximum quiescent current flow of 14 μA. The circuit operated down to a minimum input voltage of 1.1 V. This novel curvature correcting scheme can be used in almost any process technology yielding reliable temperature compensation. The additional circuitry required for this correction is compact and is easily implemented. The architecture also lends itself for versatile trimming procedures. The resulting circuit is compatible with low quiescent current flow and with low voltage operation, which is especially important in a market where demand is growing for battery-powered electronics requiring increasing efficiency and longevity.

Acknowledgment

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Table 1. Performance summary.

	Simulated Results	Measured Results
TC	6.5 ppm/°C	< 20 ppm/°C
Line Regulation (1.2 ≤ Vin ≤ 10V)	120 ppm/V	408 ppm/V
Quiescent Current	15 μA	14 μA
Minimum Input Voltage	1.1 V	1.1 V
Active Chip Area (no resistors or capacitors)		798 μm x 280 μm
MOSIS 2 μm N-well technology with added p-base layer ($V_t \approx 0.9$ V)		

Figure Captions

Figure 1. Generation of the nonlinear current component.

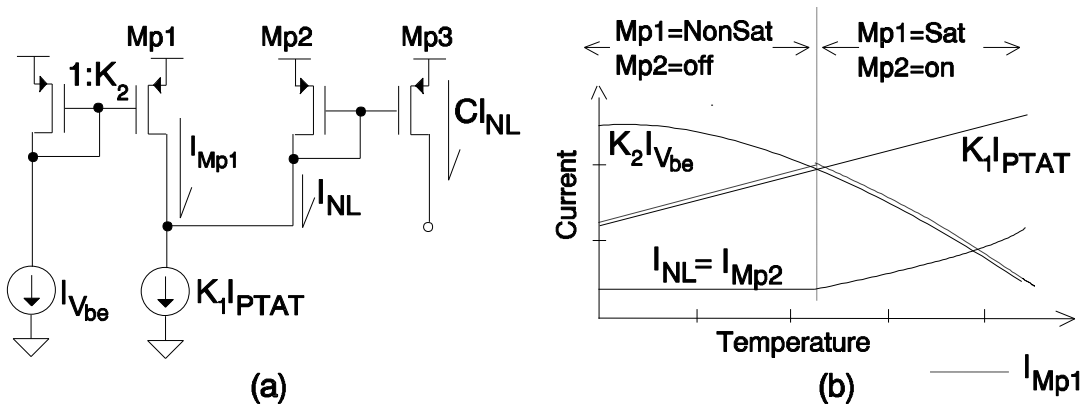
Figure 2. Temperature dependence of the curvature corrected bandgap reference.

Figure 3. Mixed current and voltage-mode architecture.

Figure 4. Low voltage curvature corrected bandgap.

Figure 5. Measured temperature coefficient of the bandgap.

Figure 6. Measured line regulation performance of the bandgap.



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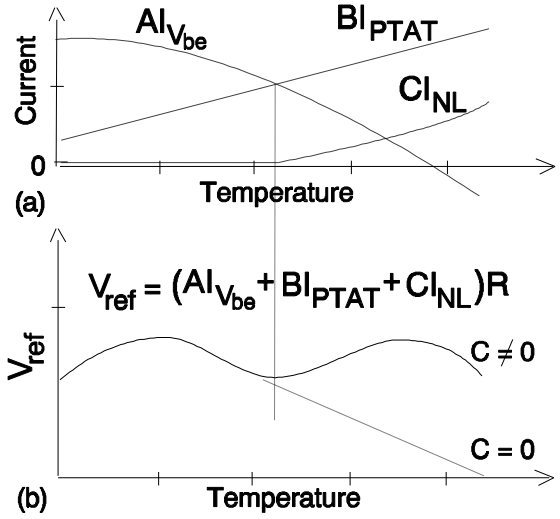

Figure 2. Temperature dependence of the curvature corrected bandgap reference.

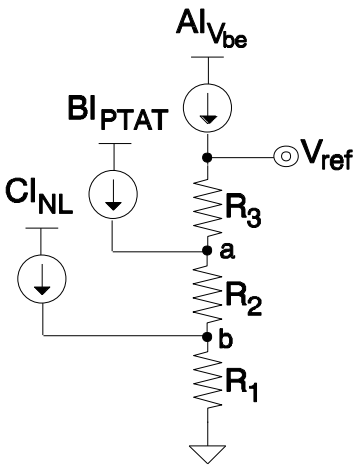

Figure 3. Mixed current and voltage-mode architecture.

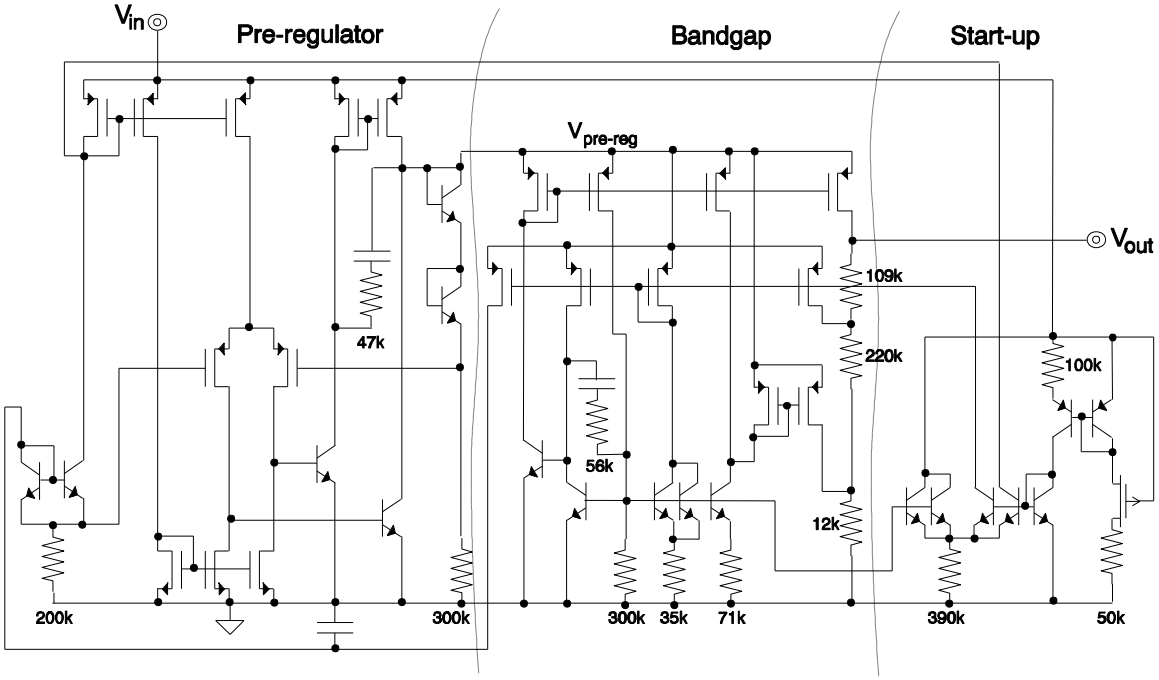

Figure 4. Low voltage curvature corrected bandgap.

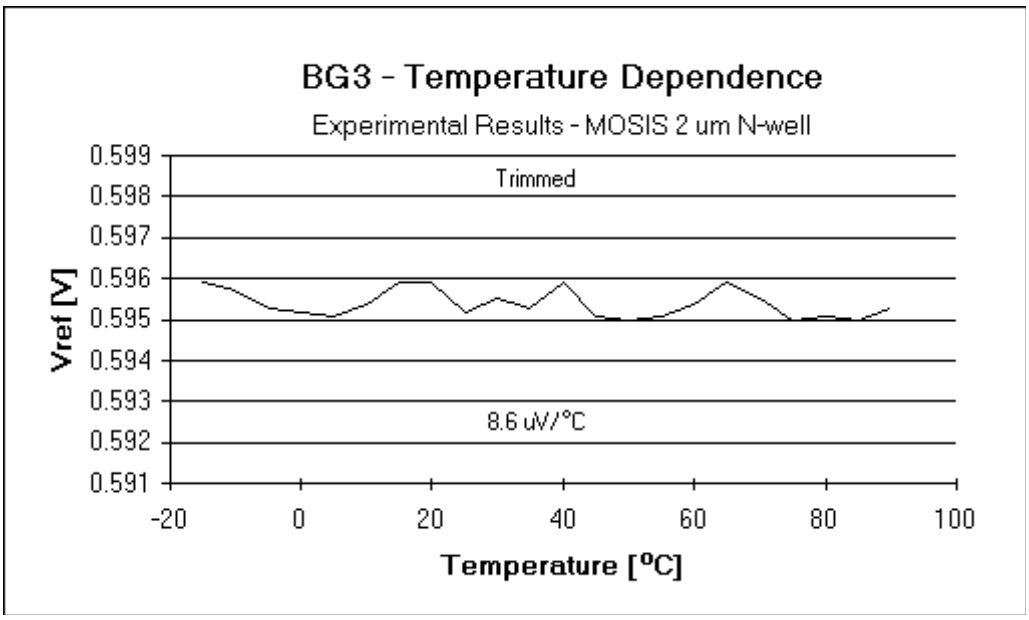

Figure 5. Measured temperature coefficient of the bandgap.

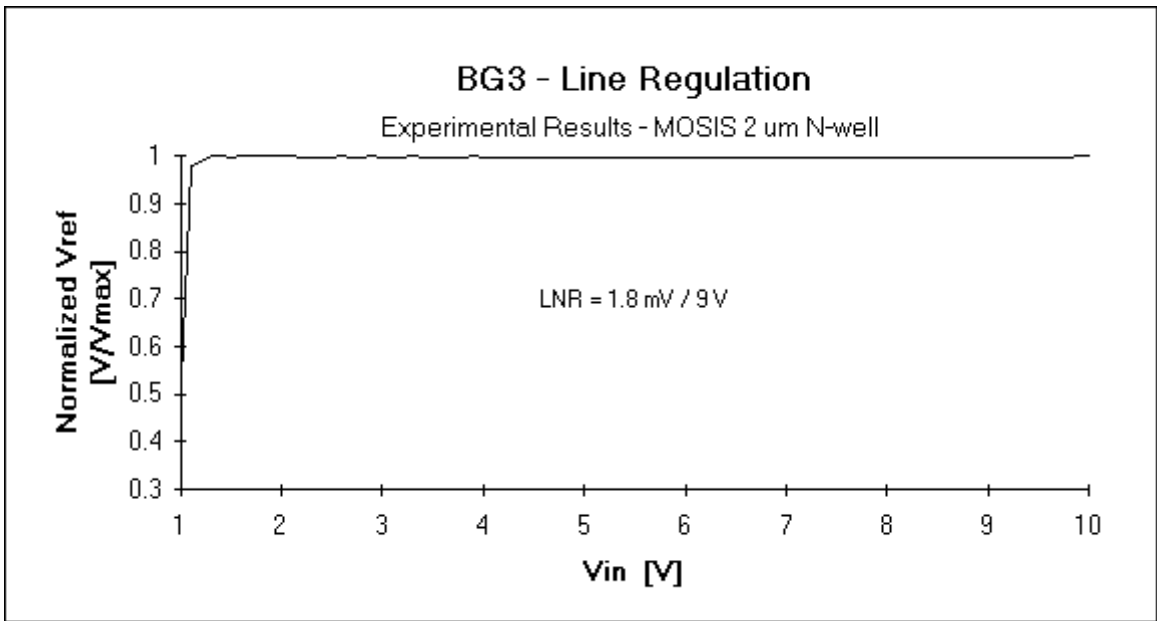

Figure 6. Measured line regulation performance of the bandgap.