180-nm CMOS Wideband Capacitor-free Inductively Coupled

Power Receiver and Charger

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Abstract: Wireless microsystems like biomedical implants and embedded sensors derive energy from tiny in-package sources that, unfortunately, exhaust easily, which means operational life is short. Periodically coupling power wirelessly is one way of replenishing onboard batteries, except small receiver coils suffer from low coupling factors k_C and induce low electromotive-force voltages. Today, receivers store and resonate incoming energy between the receiving coil and an off-chip capacitor until the voltage rises sufficiently high for a diode-bridge rectifier to steer power into a battery. The capacitor, however, requires board space and constrains the source to a particular frequency. The 180-nm CMOS power receiver presented in this paper removes the diode bridge, which establishes a minimum voltage below which the system cannot derive power, so that neither tuning nor a resonating capacitor is necessary. Experimental measurements show that the system draws power from 30-mV signals when k_C is 0.0046 and coil separation is 11.35 mm, and this threshold voltage only changes 13.6 mV across 100 – 150 kHz, which is a 27.1% lower threshold voltage that is 36× less sensitive than its resonating counterpart. The peak efficiency of the receiver when rectifying to 1.2 V is 82% at 224 μW and 125 kHz and average efficiency is 76% for 90 to 386-mV coil voltages.

I. Inductively Coupled Power

Because modern wireless microsystems typically incorporate sensors, transmitters, processors, and other components, they can monitor and add networked intelligence to unreachable and inaccessible places like the human body and outer space [1]–[4]. Small form factors, however, which wireless sensor networks [1], [5] and biomedical implants demand [4], [6], constrain how much energy thin-film Li-ion batteries [7]–[9] and onboard super capacitors [10] store to such an extent that sustaining telemetry and other important functions for extended periods is, in spite of recent advances [11]–[12], considerably difficult. Harvesting energy from thermal gradients [7], [13], vibrations [14]–[15], light [4], [16], and/or radiation [17]–[18] is therefore appealing, but not yet a reality for many applications because miniaturized transducers today only generate microwatts [19]. On the other hand, coupling power inductively from a nearby source, as Fig. 1 depicts, can supply more power than energy harvesters can because the transmitting device is, in relative terms, larger and therefore able to store and deliver vast amounts of power [20]–[23]. As examples, the body sensor network in [24] transfers 12 μW to receiving nodes across 1 cm and the memory card in [25], whose wireless feature renders it waterproof and less prone to contact failure, receives 1 W across 1 mm. In other words, a wireless link can both supply functional blocks and recharge an onboard reservoir [26]–[28], such as C_{RECT} in Fig. 1, so the system can continue to operate between recharge events and interrogations.

Still, the size of the battery limits how long the system can operate between recharge cycles, so the battery should be as large as possible. In other words, integrating as much as possible of the accompanying electronics on chip and in package is paramount. Unfortunately, geometric reductions in the receiving secondary coil L_S in Fig. 1 decrease the fraction of magnetic field perceived by L_S, which means the coupling factor k_C across the coils is low [29].

As a result, reducing the minimum k_C value $k_{C(MIN)}$ from which the system can harness magnetic energy is also imperative. On the positive side, higher levels of integration usually reduces component costs, which is critical when deploying thousands of microsensors per person.

This paper proposes an inductively coupled battery/capacitor-charging system whose aims are to reduce the size of the receiving coil by lowering the minimum k_C above which the system can harness energy and to remove the resonant off-chip capacitor present in the state of the art, which Section II describes. Section III explains how the proposed receiver rectifies the coil current, rather than the voltage, to circumvent the build-up in voltage that L–C resonant converters produce to rectify and draw power from incoming millivolt signals. Although the proposed system, like its resonant counterparts, is a charger and not a supply, its teachings extend to the case of regulated loads. Section IV then details the integrated circuit (IC) designed to implement the system and Section V shows how the built prototype performs across k_C values by way of charging profiles, equivalent input threshold voltages, and power efficiencies across frequency. Section VI ends the paper by drawing relevant conclusions.

II. Resonant Receiver

Inductively coupled systems draw energy from the magnetic field that a distant transmitting primary inductor L_P in Fig. 1 produces about a local secondary coil L_S. The power receiver derives power from the alternating electromotive-force (EMF) voltage induced across L_S: $v_{EMF.S}$. Because secondary coils are small in microsystems, the fraction of magnetic field perceived by L_S is miniscule, so its corresponding coupling factor k_C is low and, as a result, so is its $v_{EMF.S}$:

$$v_{EMF.S} = k_C \sqrt{L_P L_S} \left(\frac{di_P}{dt} \right). \tag{1}$$

Therefore, extending coil separation and reducing coil size, which equates to decreasing the minimum k_C above which the system can harness energy, amounts to lowering the minimum $v_{EMF.S}$ value $v_{EMF.S(MIN)}$ the receiver requires to steer charge into a capacitor C_{RECT} or battery.

In the case of resonant receivers [20]–[22], [30]–[31], as Fig. 2 generally illustrates, L_S and tuned off-chip capacitor C_S swap the energy they derive from L_S's changing magnetic field until the alternating voltage they produce in C_S's v_C is sufficiently high for a diode bridge like D_1 – D_4 to conduct current i_C into C_{RECT}. Since i_C ultimately flows through two diodes and C_{RECT} every time the bridge engages, v_C must rise to two diode voltages $2V_D$ and C_{RECT}'s V_{RECT} before clamping and driving excess L_S–C_S tank energy into C_{RECT}. In other words, the energy in the tank must rise above minimum $E_{LC(MIN)}$ before C_{RECT} can receive power:

$$E_{LC(MIN)} = 0.5C_S\left(2V_D+V_{RECT}\right)^2 \approx 0.5L_S i_{L(PK)}{}^2, \tag{2}$$

where i_L is L_S's current, $i_{L(PK)}$ is i_L's peak, and peak EMF voltage $v_{EMF.S(PK)}$ is considerably below V_{RECT}. Therefore, in sourcing i_L when i_L and $v_{EMF.S}$ are in phase [20], [32], $v_{EMF.S}$ drives EMF power $P_{EMF.S}$ into C_{RECT}:

$$P_{EMF.S} = v_{EMF.S(RMS)} i_{L(RMS)} = \left(\frac{v_{EMF.S(PK)}}{\sqrt{2}}\right)\left(\frac{i_{L(PK)}}{\sqrt{2}}\right) = \frac{v_{EMF.S(PK)}\left(2V_D + V_{RECT}\right)}{2\left(2\pi f_S\right)L_S}, \tag{3}$$

when $v_{EMF.S}$ oscillates at L_S–C_S's natural frequency f_{LC}: $1/2\pi\sqrt{L_S C_S}$. Because i_L and $v_{EMF.S}$ are no longer in phase when $v_{EMF.S(PK)}$ is higher [20], many implementations operate below f_{LC}.

In practice, L_S's equivalent series resistance (ESR) R_S consumes some of the energy in the tank, so without sufficient EMF power, v_C may never rise above the rectifier's threshold voltage. In other words, $v_{EMF.S}$ must increase above a minimum value $v_{EMF.S(MIN)}$ that accounts for R_S's voltage drop and power loss for v_C to reach $2V_D + V_{RECT}$ at resonance $1/2\pi\sqrt{L_S C_S}$:

$$v_C = \frac{v_{EMF.S}\left(1/C_S s\right)}{L_S s + R_S + \left(1/C_S s\right)} = \frac{v_{EMF.S}}{C_S L_S s^2 + C_S R_S s + 1}, \tag{4}$$

so solving for $v_{EMF.S}$ when v_C is $2V_D + V_{RECT}$ at f_{LC} indicates that $v_{EMF.S(MIN)}$ is

$$v_{EMF.S(MIN)} \equiv v_{EMF.S(PK)}\Big|_{v_{C(PK)}=2V_D+V_{RECT}} = \left(2V_D + V_{RECT}\right)\left(\frac{C_S R_S}{\sqrt{L_S C_S}}\right) = \frac{2V_D + V_{RECT}}{Q_{LS}}, \tag{5}$$

where Q_{LS} is L_S's quality factor $2\pi f_{LC}(L_S/R_S)$. Replacing the diodes with diode-connected low-V_{TH} FETs reduces the voltage drop, but not to the extent that comparator-synchronized MOS switches can because of reverse-conduction and overdrive considerations [15], [30], [33]. The comparator-synchronized MOS switches reduce the diode bridge's turn-on voltage from $2V_D + V_{RECT}$ to nearly V_{RECT} because the transistors drop close to zero volts when conducting, whose savings surpasses the quiescent power needs of the comparators that switch at 125 kHz. L_S–C_S then reduces $v_{EMF.S(MIN)}$ by a factor of Q_{LS} when Q_{LS} is greater than one. This reduction, however, results only after tuning L_S and C_S's natural frequency f_{LC} to $v_{EMF.S}$'s oscillating frequency f_O, which means threshold voltage $v_{EMF.S(MIN)}$ is higher at all other frequencies, when f_O is not f_{LC}. Plus, raising Q_{LS} to lower $v_{EMF.S(MIN)}$ also reduces L_S–C_S's boosted bandwidth f_{LC}/Q_{LS} [34], which exacerbates $v_{EMF.S(MIN)}$'s sensitivity to frequency. Unfortunately, tuning f_{LC} to f_O requires test time, the cost of which the proposed technology avoids.

III. PROPOSED CAPACITOR-FREE POWER RECEIVER AND CHARGER

Without the resonant capacitor, the diode bridge does not draw energy from L_S's magnetic field because L_S cannot conduct current i_L until L_S's induced EMF voltage surpasses holding capacitor C_{RECT}'s voltage by some margin. In the proposed capacitor-free receiver of Fig. 3, however, $v_{EMF.S}$ need not exceed a threshold voltage because, with switches S_N^+ and S_N^- closed, L_S can energize from any non-zero value of $v_{EMF.S}$. This way, since L_S's impedance overwhelms R_S near f_O, S_N^+ and S_N^- close across most of $v_{EMF.S}$'s positive half cycle τ_{EN}^+ in Fig. 4 to raise L_S's i_L to

$$\Delta i_L = \int_0^{\tau_{EN}^+} \frac{v_{EMF.S(PK)} \sin(2\pi f_O t)}{L_S} dt \approx \frac{v_{EMF.S(PK)}}{\pi f_O L_S}, \tag{6}$$

drawing energy packet E_{LS} from L_S's magnetic field:

$$E_{LS} = 0.5 L_S \Delta i_L{}^2 = \frac{v_{EMF.S(PK)}{}^2}{2\pi^2 f_O{}^2 L_S}. \tag{7}$$

After τ_{EN}^+, S_N^+ opens and i_L raises v_{SW}^+ almost instantly until diode switch S_D^+ engages and steers i_L into C_{RECT}. After L_S depletes, S_N^+ and S_N^- similarly close during most of v_{EMF}'s negative half cycle across τ_{EN}^-, so i_L falls to Δi_L to energize L_S with another energy packet E_{LS}. S_N^- then opens and i_L raises v_{SW}^- until S_D^- drives E_{LS} into C_{RECT}, after which the entire cycle repeats. Table I summarizes the switching states and timing sequence of the network.

Since C_{RECT} ultimately receives E_{LS} twice every cycle, the converter outputs EMF power

$$P_{EMF.S} = \frac{2E_{LS}}{T_O} = \frac{v_{EMF.S(PK)}{}^2}{\pi^2 f_O L_S}. \tag{8}$$

Although $v_{EMF.S}$ need not surpass a turn-on voltage, $v_{EMF.S}$ must nonetheless supply the conduction, gate-drive, and quiescent bias power that the converter dissipates as P_{LOSS} to generate an output. In other words, $v_{EMF.S}$ must surpass a minimum $v_{EMF.S(MIN)}$ threshold voltage for $P_{EMF.S}$ to exceed P_{LOSS}, or equivalently, $P_{EMF.S(MIN)}$ and generate an output:

$$v_{EMF.S(MIN)} = \pi\sqrt{f_O L_S P_{EMF.S(MIN)}} = \pi\sqrt{f_O L_S P_{LOSS}} \approx \pi\sqrt{f_O L_S \left(E_{GD} f_O + P_{BIAS}\right)}. \tag{9}$$

When k_C and therefore $P_{EMF.S}$ and $v_{EMF.S}$ are small, and as conduction losses P_C in the system scale with $P_{EMF.S}$, then gate-drive and bias losses P_{GD} and P_{BIAS} overwhelm P_C. As a result, since parasitic switch capacitors require gate-drive energy E_{GD} every time the switches engage, gate-drive power is $E_{GD} f_O$ and P_{LOSS} reduces to $E_{GD} f_O$ and P_{BIAS}, all of which says that parasitic capacitors, the controller circuit, and f_O set $v_{EMF.S(MIN)}$.

IV. Circuit Design

A. Power Stage

Since energizing switches S_N^+ and S_N^- in Fig. 3 short to ground, n-channel MOS transistors M_N^+ and M_N^- in the circuit embodiment of Fig. 5 implement them. P-type devices M_P^+ and M_P^-, on the other hand, implement diode switches S_D^+ and S_D^- because they drop considerably lower voltages than diodes when connected to a high voltage, such as reservoir capacitor voltage V_{RECT}. Therefore, CP_D^+ and CP_D^-, like diodes, engage M_P^+ and M_P^- when the transistors' respective source voltages v_{SW}^+ and v_{SW}^- rise above their drain voltage V_{RECT}.

All these switches dissipate Ohmic power $P_{C.MOS}$ when they conduct i_L and require gate-drive energy E_{GD}, or equivalently, power P_{GD} to charge their gates. Therefore, since shortening the channel length reduces both source–drain resistance in $P_{C.MOS}$ and gate capacitance in P_{GD}, all channel lengths should be short at, for example, 180 nm. The same is not true for channel widths because wider MOSFETs reduce resistance, but also raise gate capacitance, so while wider FETs dissipate less $P_{C.MOS}$, they also require more P_{GD}. As a result, reducing losses in the power stage amounts to selecting the optimum channel widths that balance and minimize $P_{C.MOS}$ and P_{GD} [35]. In this regard, considering the symmetry of the circuit and its operation across its positive and negative half cycles, M_N^+'s and M_P^+'s averaged resistances per cycle should match those of M_N^- and M_P^-. But since these NFETs conduct similar currents across considerably longer periods than the PFETs, which means NFETs dissipate substantially more power than PFETs, optimum n-type channels are wider at 1108 μm than optimum p-type channels at 368 μm.

More specifically, L_S's ESR R_S, M_N^+, and M_N^- consume conduction power when the energizing portions of i_L: i_{EN}^+ and i_{EN}^- from Fig. 4, flow through them, as do R_S, M_N^-, and M_P^+ immediately after the positive half cycle and R_S, M_N^+, and M_P^- after the negative half cycle when they carry de-energizing inductor currents i_{DE}^+ and i_{DE}^-, respectively. In other words, in addition to R_S, two NMOS triode resistances dissipate conduction power when L_S energizes and one n- and one p-type resistances when L_S de-energizes:

$$P_C = P_{EN} + P_{DE} = \left(2R_N + R_S\right) i_{L.EN(RMS)}{}^2 + \left(R_N + R_P + R_S\right) i_{L.DE(RMS)}{}^2, \tag{10}$$

where R_N and R_P are M_N and M_P's triode resistances and $i_{L.EN}$ and $i_{L.DE}$ are the energizing and de-energizing components of i_L. Also, since the system charges the gates of M_N^+, M_N^-, M_P^+, and M_P^- to V_{RECT} once per cycle, V_{RECT} supplies gate charge Q_G to all four gate–channel capacitances C_G to consume

$$P_{GD} = Q_G V_{RECT} f_O = \left(C_G V_{RECT}\right) V_{RECT} f_O = \left(2W_N L_N + 2W_P L_P\right) C_{OX}'' V_{RECT}{}^2 f_O, \tag{11}$$

where W_N, W_P, L_N, and L_P are n-/p-type channel widths and lengths, C_{OX}'' is oxide capacitance per area, and $2W_NL_NC_{OX}''$ and $2W_PL_PC_{OX}''$ are two n- and two p-type gate capacitances.

The purpose of NOR gates NOR^+ and NOR^- is to reduce the current–voltage overlap power in M_N^+ and M_N^-. The problem is that, because M_P^+ and M_P^- require time to respond, M_P^+ or M_P^- connects L_S to C_{RECT} past the time needed to drain L_S into C_{RECT}. As a result, C_{RECT} cycles some energy back into L_S, offsetting i_L to a non-zero value at the end of de-energizing times τ_{DE}^+ and τ_{DE}^- in Fig. 4. This means that the instant M_N^+ or M_N^- closes, after M_P^+ or M_P^- disengages and v_{SW}^+ or v_{SW}^- nears V_{RECT}, M_N^+ or M_N^- conducts a non-zero i_L across V_{RECT}. To mitigate the power this current–voltage overlap condition incurs, these NOR gates keep M_N^+ and M_N^- from engaging until i_L discharges v_{SW}^+ and v_{SW}^- below the gates' transition point of $0.5V_{RECT}$, as Fig. 6 shows for the positive half cycle. This way, since the parasitic capacitance at v_{SW}^+ and v_{SW}^- is low, the additional time v_{SW}^+ and v_{SW}^- require to reach zero is short, so M_N^+ and M_N^- close when their drain–source voltages are practically zero, which means they dissipate negligible power. Note that, although a comparator can implement this function more accurately, its power losses can easily negate the energy saved from switching with close to zero volts.

Since M_P^+ and M_P^- emulate diodes, they also dissipate little current–voltage overlap power during their switching transitions. When prompted to engage, for example, the M_P^+ and M_P^- do not conduct until i_L charges parasitic capacitances at v_{SW}^+ and v_{SW}^- to V_{RECT}, when source–drain voltage v_{SD} is low. Similarly, on the other end of their conduction period, they disengage when i_L is low. In other words, because either drain current or v_{SD} is nearly zero during every transition, M_P^+ and M_P^- dissipate negligible power when switching. Note that, without NOR^+ and NOR^- or the diode-switch comparators to implement the nearly zero-voltage or zero-current switching conditions, charging and discharging parasitic capacitances C_{PAR} at v_{SW}^+ and v_{SW}^- to the rectified output V_{RECT} every cycle would require additional energy $C_{PAR}V_{RECT}^2$. At a charging frequency of f_O, this loss would be 2.8 µW, which roughly represents 30% and 6% of all losses in the system when $v_{EMF.S}$ is 40 mV and 390 mV, respectively.

B. Control

The system must synchronize S_N^+ and S_N^- in Fig. 3 to $v_{EMF.S}$'s half cycles for them to engage at the appropriate times. Since $v_{EMF.S}$ is proportional to the rate of change of the emanating primary coil's current i_P, flips in di_P/dt's polarity correspond to those of $v_{EMF.S}$. Flips in polarity can therefore prompt the system to stop energizing L_S and the polarity can indicate with which switch to do it: S_N^+ or S_N^-. For this, comparator CP_{PK} in Fig. 5 trips when i_P via i_PR_{SENSE} rises or falls below an $R_{PK}C_{PK}$-delayed version of itself via v_{DLY} to indicate whether i_P starts rising or falling. Accordingly, CP_{PK}'s output $S_{EMF.S}$, which is high when i_P rises and $v_{EMF.S}$ is high and low otherwise, commands S_N^+ to open when i_P stops rising after L_S energizes across $v_{EMF.S}$'s positive half cycle and S_N^- to open when i_P stops falling after L_S energizes in the other half cycle.

In the circuit realization of Fig. 5, M_N^+ and M_N^- engage every time L_S energizes from $v_{EMF.S}$. When $v_{EMF.S}$ enters its negative half cycle, after i_P stops rising, $S_{EMF.S}$ transitions low to open M_N^+ via two NOR gates and a driving buffer. Since L_S's i_L is non-zero at the end of the energizing period in the positive half cycle, i_L raises v_{SW}^+ until CP_D^+ senses that v_{SW}^+ rises above V_{RECT} and trips to engage M_P^+ and steer i_L into C_{RECT}. When v_{SW}^+ drops to V_{RECT}, which corresponds to i_L and E_{LS} nearing zero, CP_D^+ transitions high to shut M_P^+ and set the SR latch, which again closes M_N^+ to start energizing L_S across the negative half cycle. At the end of the energizing period in the negative half cycle, when i_P stops falling, $S_{EMF.S}$ transitions high to open M_N^- via an inverter, two NOR gates, and a driving buffer. Since L_S similarly energized across the negative half cycle, its non-zero current i_L raises v_{SW}^- until CP_D^- trips to engage M_P^- and drain L_S's E_{LS} into C_{RECT}. When i_L is close to zero, v_{SW}^- drops to V_{RECT} and, as a result, CP_D^- transitions high to shut M_P^- and reset the SR latch, which again closes M_N^- across the following positive half cycle, after which point the entire sequence repeats.

The foregoing scheme assumes that sensing i_P is possible, which is not always the case. Disconnecting L_S across one or two periods to sense and program $v_{EMF.S}$'s transitions for subsequent cycles is another way to synchronize the system. The transmitter can also send this information across L_P–L_S's inductive link. Here, the $S_{EMF.S}$ generator in Fig. 5 is only an example used to assess the efficacy of the power receiver, which is the focus of this work.

C. Diode-switch Comparators

As already mentioned, M_P^+–CP_D^+ and M_P^-–CP_D^- implement diode switches S_N^+ and S_N^- in Fig. 3. Unfortunately, CP_D^+ and CP_D^- require time to respond, so before they engage M_P^+ and M_P^-, the transistors' body diodes conduct L_S's i_L momentarily. To keep the parasitic power loss that i_L dissipates in the diodes low, CP_D^+ and CP_D^- should respond quickly, except fast comparators require considerable power. Fortunately, the system relies on CP_D^+ and CP_D^- to sense v_{SW}^+ and v_{SW}^- only after $v_{EMF.S}$ finishes energizing L_S and through the de-energizing periods, so only enabling CP_D^+ and CP_D^- just before and through τ_{DE}^+ and τ_{DE}^-, respectively, when M_N^+ and M_N^- shut with v_{EN}^+ and v_{EN}^- in Fig. 5, saves energy.

The comparators should also wait until L_S depletes before shutting M_P^+ and M_P^- because, after the switches open, L_S's remnant energy may otherwise raise v_{SW}^+ and v_{SW}^- to the point CP_D^+ and CP_D^- can re-engage M_P^+ and M_P^-. Prompting the transistors to once again conduct not only dissipates additional gate energy but also causes the system to oscillate until L_S fully drains. To avoid this situation, CP_D^+ and CP_D^-'s trip points should incorporate hysteresis, so that CP_D^+ and CP_D^- trip when v_{SW}^+ and v_{SW}^- surpass V_{RECT} and, with an intentional negative offset, when v_{SW}^+ and v_{SW}^- fall below V_{RECT} by some small margin. The hysteresis also suppresses the noise effects that charge-injection and clock feed-through produce when switching M_P^+ and M_P^-.

Bearing these requirements in mind, the comparator of Fig. 7 requires 38 μA to respond in 3 and 62 ns to rising and falling v_{SW} events, respectively, incorporates 32 mV of hysteresis, and operates only when v_{EN} enables it. Here, gate-coupled transistors M_{P1} and M_{P2} derive their source voltages from the terminals of the PMOS switch they sense: from M_P^+ or M_P^- in Fig. 5, so that M_{P1} conducts more current when v_{SW} is higher than V_{RECT} and less current otherwise. That way, since M_{N1}–M_{N2} mirrors twice M_{P2}'s current i_{P2}, M_{P1}'s current i_{P1} raises v_{COMP} when i_{P1} exceeds $2i_{P2}$, which happens when v_{SW} rises above V_{RECT} by 29 mV – this offset keeps the comparator from tripping prematurely when remnant energy resonates between L_S and the parasitic capacitance at v_{SW}. Increasing v_{COMP} not only lowers comparator output v_O to engage M_P^+ or M_P^- but also engages switch M_H, which sinks offset current i_{HYST} at 18/32 of i_{P2} from

M_{P2}. As such, M_{P1}'s i_{P1} must fall below $2i_{P2}$ by $2i_{HYST}$ for v_{COMP} to fall and v_O to rise, which means i_{HYST} establishes a hysteretic offset of 3 mV when v_{SW} falls below V_{RECT}.

Since the circuit trips when M_{P1}'s v_{SG1} at $2i_{P2} - 2i_{HYST}$ and v_{SW} balance M_{P2}'s v_{SG2} at i_{P2} and V_{RECT}, v_{COMP} transitions when v_{SW} crosses the comparator's lower trip point V_{TRIP}:

$$V_{TRIP} = V_{RECT} - v_{SG2} + v_{SG1} = V_{RECT} - \left(\sqrt{i_{P2}} - \sqrt{2i_{P2} - 2i_{HYST}}\right)\sqrt{\frac{1}{K_P'\left(W/L\right)_{P2}}}, \tag{12}$$

M_{P1} and M_{P2}'s width–length aspect ratios W/L match and V_{TP}'s match and therefore cancel. Here, V_{TRIP} shifts with $1/\sqrt{K_P'}$, so V_{TRIP}'s offset from V_{RECT} rises with temperature because K_P' falls at -2.77×10^3 ppm/°C at 27 °C. To offset this drift, i_{P2} and i_{HYST} derive its bias from a reference current that falls with temperature: from complementary-to-absolute-temperature current I_{CTAT}. Although I_{CTAT}'s drift of -3.59×10^3 ppm/°C at 27 °C does not match that of K_P', I_{CTAT}'s compensation in V_{TRIP} is sufficient for the system to work as prescribed.

Ultimately, the key features of this design stem from gate-coupled p-type input pair M_{P1}–M_{P2}. For one, they can compare larger-than-supply voltages, which is necessary because v_{SW}^+ and v_{SW}^- both rise above V_{RECT}. Secondly, M_{P1} can conduct considerably more current than M_{P2} when v_{SW} surpasses V_{RECT}, so v_{COMP} rises and v_O falls quickly in 3 ns to engage M_P^+ or M_P^- before body diodes steer and dissipate more of L_S's energy. Because biasing transistor M_{PB} limits M_{P2}'s i_{P2}, M_{N1} pulls v_{COMP} in the opposite direction with no more than $2i_{P2}$, which is why v_O requires more time to rise at 62 ns than to fall.

Since 38.4 μA bias the comparator, disabling it across energizing periods τ_{EN}^+ and τ_{EN}^- saves considerable energy. For this purpose, M_{DIS1} shuts the circuit's current supply and M_{EN2} shuts input pair M_{P1}–M_{P2}. This way, CP_D^+ and CP_D^- dissipate P_{CP} across oscillating period T_O:

$$P_{CP} = I_{CP}V_{RECT}\left(\frac{\tau_{DE}^+ + \tau_{DE}^-}{T_O}\right) = \frac{2I_{CP}V_{RECT}}{T_O}\left(\frac{\Delta i_L L_S}{V_{RECT}}\right) = \frac{2I_{CP}v_{EMF.S(PK)}}{\pi}, \tag{13}$$

where I_{CP} is the bias current of each comparator. Notice P_{CP} increases with Δi_L because inductors with higher currents have more energy and therefore require more time to de-energize. In other words, since $v_{EMF.S}$ energizes L_S, higher $v_{EMF.S(PK)}$ and $P_{EMF.S}$ levels ultimately demand more power from CP_D^+ and CP_D^-.

Unfortunately, the benefits of a fast response to a rising v_{SW} dissipate when enabling the comparators requires considerable time. To mitigate this adverse effect, once M_{EN1} connects the source of diode-connected NMOS transistor M_{LB} to ground, M_B and M_{HYST} bias from a fast, low-impedance node: v_{BIASN}. For this, the negative feedback loop that M_{SF} and M_{FB} implements shunt-samples v_{BIASN}, so that when M_{LB}'s source terminal first connects to ground, the loop via M_{SF} quickly supplies whatever current is necessary to charge M_{LB}'s gate–source capacitance C_{GS} to v_{BIASN}. The purpose of M_{SB} is to activate the loop by ensuring M_{SF} conducts some current before v_{EN} enables the comparator, when M_{LB} is still off. The loop also counters the effects of noise injection from M_B's C_{GD} on v_{BIASN}, which is otherwise problematic during startup, when M_{DIS1} first switches. M_{SB} only sinks half of M_{FB}'s 150-nA current to conserve energy and, in addition to M_{SB}'s, conducts M_{LB}'s current once engaged to accelerate the loop's response.

The benefit of a diode-switch comparator over a p–n diode and a diode-connected MOSFET is low power because, while the latter two drop 200 – 600 mV, the former drops less than 50 mV. Charging to 1.2 V with a 400-mV drop, for example, when assuming no other component in the system dissipates power reduces efficiency to 75%. The prototyped system, on the other hand, achieves 82% after including all quiescent, switching, and conduction losses.

D. CTAT Current Generator

The two-stage amplifier that M_{IN}^-, M_{IN}^+, M_M^-, M_M^+, M_{TAIL}, and M_R realize in Fig. 8 impresses Q_{CTAT}'s emitter–base voltage V_{EB} across R_{CTAT} to ensure R_{CTAT} and M_R conduct V_{EB}/R_{CTAT}.

Because V_{EB} falls with temperature at -3.59×10^3 ppm/°C at 27 °C and R_{CTAT} drifts little with temperature, M_R and its mirroring outputs source CTAT currents. To ensure the amplifier's feedback loop is stable, C_C establishes a dominant pole at M_R's gate and nulling resistor R_C shifts the out-of-phase, feed-forward zero that C_C introduces to the left-half plane near the pole at M_R's drain. This way, the open-loop gain reaches 0 dB at –20 dB/decade of frequency with roughly 65° of phase margin. As to startup, long-channel, diode-connected transistor M_{SU1}'s current opposes M_{SU2}'s I_{CTAT}-derived current to engage M_{SU3} and pull M_R's gate down only when the circuit is off, so M_{SU3}'s current can raise M_{IN}^-'s gate and latch I_{CTAT} to its stable non-zero state. For all this, the generator uses 156 nA at 27 °C, which together with CP_D^+ and CP_D^-'s 900-nA startup mirrors, means the system's total quiescent power is 1.27 µW for a V_{RECT} of 1.2 at 27 °C.

V. Experimental Validation

The 180-nm 700 × 700-µm^2 die in Fig. 10 incorporates the power receiver proposed in Fig. 5, except for the 400-µH Coilcraft 4513TC receiver coil L_S, the 100-nF SMD ceramic holding capacitor C_{RECT}, the $S_{EMF.S}$-signal generator, and bias resistor R_{CTAT}, the latter two of which were off chip to add flexibility when testing the system. The prototyped printed circuit board (PCB) shown incorporates the 28-pin thin-shrink small-outline package (TSSOP) that encapsulates the IC, all off-chip components mentioned above, and instrumentation amplifiers, current-sense resistors, and voltage buffers designed to monitor and test the system. Additionally, the IC houses test-only circuits and pins, such as digital-signal buffers, override multiplexers to bypass switch-control blocks, and test-mode logic. L_S exhibited an ESR of 9.66 Ω with a quality factor of 29 at 125 kHz, which was the system's operating frequency. The power transmitter illustrated in Fig. 10 consists of a 14.8-mH primary Coilcraft ZXC coil L_P with an ESR of 160 Ω, a 100-nF SMD ceramic resonant capacitor C_P, and the $S_{EMF.S}$-signal generator. The stand, the 443-4

Newport linear stage, and the 1-μm sensitive SM-50 Newport Vernier Micrometer shown offers a 50-mm travel range with which to vary coupling factor k_C, that is, to vary $P_{EMF.S}$ and $v_{EMF.S(PK)}$.

A. Charging Performance

The time-domain charging profiles in Fig. 11 demonstrate how the prototyped system charged C_{RECT}'s 100 nF at 125 kHz when driven with peak EMF voltages of 30, 127, 261, and 368 mV, which correspond to successively increasing coupling factors 0.0046, 0.0195, 0.0342, and 0.0665. Since the system outputs packets of energy every half-cycle, C_{RECT}'s v_{RECT} rises in staircase fashion every 4 μs, much like a pulse-charged system does [37]–[38]. Here, higher $v_{EMF.S(PK)}$ values raise v_{RECT}'s rising stair-step rate because EMF power $P_{EMF.S}$ increases quadratically with $v_{EMF.S(PK)}$, which is to say that C_{RECT} charges more quickly with more $P_{EMF.S}$.

The stair steps are not perfectly flat because the system consumes power. Plus, the step is smaller than $P_{EMF.S}$ predicts at low $v_{EMF.S(PK)}$ values because gate-drive and quiescent power losses through the system do not scale with $v_{EMF.S(PK)}$, which means losses dissipate an increasing fraction of $P_{EMF.S}$ when $P_{EMF.S}$ falls. In fact, $P_{EMF.S}$ at a $v_{EMF.S(PK)}$ of 30 mV in this system is just high enough to account for all losses. Therefore, when comparing this threshold voltage to that of resonant systems, the proposed system's threshold voltage is lower when its losses P_{LOSS} fall below the minimum EMF power $P_{EMF.S(MIN)'}$ that resonant systems set with $v_{EMF.S(MIN)'}$:

$$P_{LOSS} < P_{EMF.S(MIN)'} = \frac{{v_{EMF.S(MIN)'}}^2}{\pi^2 f_O L_S} = \frac{\left(2V_D + V_{RECT}\right)^2}{\pi^2 f_O L_S {Q_{LS}}^2}. \tag{14}$$

B. Sensitivity of Threshold Voltage $v_{EMF.S(MIN)}$ to Frequency

Varying $v_{EMF.S}$'s oscillating frequency f_O by ±20% across 50 kHz about the 125-kHz nominal point changed the minimum $v_{EMF.S(MIN)}$ threshold voltage 13.6 mV. For comparison, as Fig. 12 shows, equivalent resonant systems with quality factors of 29 and 100 from [22], [27], [29], [39], [40] exhibit similar $v_{EMF.S(MIN)}$ values at 125 kHz, where $v_{EMF.S(MIN)}$ at a quality factor of 100 is slightly lower. When the oscillating frequency deviates ±20% from the receivers' natural frequency of 125 kHz, however, the resonant receivers' threshold voltages increase drastically to 433 – 529 mV, whereas that of the proposed system remains near 30 mV. What is more, $v_{EMF.S(MIN)}$ values of increasingly mismatched frequencies in resonant systems converge to values that are independent of L_S's quality factor, negating the benefits of inductors with higher quality factors. Notice $v_{EMF.S(MIN)}$ of the proposed receiver rises slightly with f_O because gate-drive power increases with f_O, while input power $P_{EMF.S}$ decreases slightly with f_O.

C. Receiver's Power Efficiency

Because M_N^+ and M_N^- conduct L_S's current i_L across the energizing periods of both the positive and negative half cycles in addition to one de-energizing period and M_P^+ and M_P^- only conduct across one de-energizing period, M_N^+ and M_N^- consume more conduction power as P_N than M_P^+ and M_P^- as P_P, as Fig. 13 shows. At 9.7 Ω, R_S not only is higher than the resistances of M_N^+, M_N^-, M_P^+, and M_P^- but also conducts i_L across all periods, so R_S dissipates more power as P_{RS} than P_N and P_P. In the end, all these losses scale with input power $P_{EMF.S}$, which means they increase quadratically with $v_{EMF.S(PK)}$, if not faster [35]. Comparator losses P_{CP}^+ and P_{CP}^- also rise with $v_{EMF.S}$ because more energy in L_S means M_P^+ and M_P^- and their driving comparators require more time to drain L_S into C_{RECT}. Bias and gate-drive losses P_{BIAS} and P_{GD}, on the other hand, which are 1.5 µW and 0.7 µW on average, do not vary as much with $v_{EMF.S(PK)}$ and $P_{EMF.S}$.

When input power $P_{EMF.S}$ is low, conduction losses P_N, P_P, and P_{RS} fall to the point P_{BIAS}, P_{GD}, P_{CP}^+, and P_{CP}^- dominate with 9 µW of the 11.3 µW the entire system dissipates, which means P_{BIAS}, P_{GD}, P_{CP}^+, and P_{CP}^- set the minimum threshold power $P_{EMF.S(MIN)}$ below which the system cannot output power. Note that, since $P_{EMF.S(MIN)}$'s dependence on P_{RS} is weak, the quality factor of a receiving inductor does not impose limits on $P_{EMF.S(MIN)}$. As $P_{EMF.S}$ rises, however, conduction losses P_N, P_P, and P_{RS} rise to 7.3 μW, 6.5 μW, and 24.2 μW at a $v_{EMF.S(PK)}$ of 386 mV, respectively, and ultimately limit the extent to which output power P_{RECT} increases with $P_{EMF.S}$. In other words, the system's conversion efficiency η_S in Fig. 14, which refers to output–input power ratio $P_{RECT}/P_{EMF.S}$, depends largely on M_N^+, M_N^-, M_P^+, M_P^-, and R_S at higher power levels and, accordingly, peaks at 82%, when $v_{EMF.S(PK)}$ is 386 mV and output power P_{RECT} is 224 μW:

$$\eta_S \equiv \frac{P_{OUT}}{P_{IN}} = \frac{P_{RECT}}{P_{EMF.S}} = \frac{P_{EMF.S} - P_{LOSS}}{P_{EMF.S}} . \tag{15}$$

D. Context

Table II summarizes and compares the performance of the prototyped receiver and charger with the state of the art. One basic aim in this design was to eliminate the large capacitor C_S that resonant receivers require. Although integrating the 33 – 336 pF that C_S in [24], [25], [41]–[43] requires is not always prohibitive, the operating frequencies they establish surpass 6 MHz. For them to operate at 125 kHz, like the prototyped system, C_S would be in the nano-Farad range, as Fig. 12 demonstrates. The significance of operating at lower frequency is lower power losses, or higher output power. At 125 kHz, transistors switch less frequently, so they require less gate-drive power, and the diode-switch comparators need less quiescent power. Resonant receivers prefer higher frequencies because a higher Q_{LS} [44] reduces the minimum $v_{EMF.S}$ above which they can harness power.

VI. Conclusions

With average and peak power-conversion efficiencies of 76% and 82% across $v_{EMF(PK)}$ values of 90.5 – 386 mV at 125 kHz, the presented 180-nm CMOS power receiver generated power from EMF voltages down to about 30 mV across 100 – 150 kHz, peaking at 386 mV with 224 μW to charge 100 nF from 1.25 to 1.33 V in 37.9 μs. The fundamental benefits of removing the off-chip resonant capacitor and the diode bridge that conventional resonant systems normally include are low form factor and low threshold-voltage sensitivities to oscillating frequency f_O and the receiving coil's quality factor Q_{LS}. This way, while the minimum EMF voltage above which a resonant system generates power increases roughly by 10× with 10% deviations in f_O from the system's natural resonant frequency f_{LC}, the threshold voltage of the system proposed only varied 10%. Plus, Q_{LS} does not limit this threshold voltage, whereas it does in the case of the resonant counterpart. The importance of a lower, less sensitive threshold voltage is that the power receiver can derive more energy from loosely coupled coils, which means wireless microsensors and biomedical implants, to cite two examples, can draw power from an emanating source that is further away. The space savings that results from removing the resonant capacitor can also shrink the system, or similarly accommodate a larger onboard battery that can power the device between longer recharge events.

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Figures

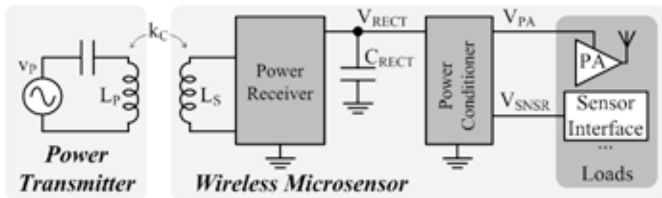

Fig. 1. Wirelessly powering a microsensor system from an inductively coupled source.

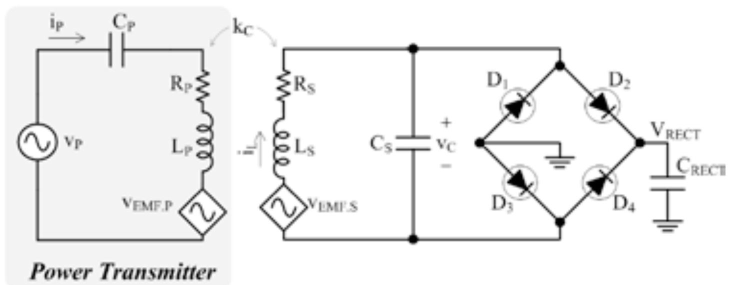

Fig. 2. Resonant power receiver and charger.

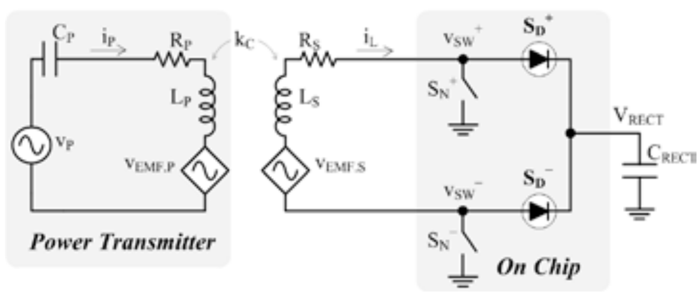

Fig. 3. Proposed switched-inductor power receiver and charger [35]–[36].

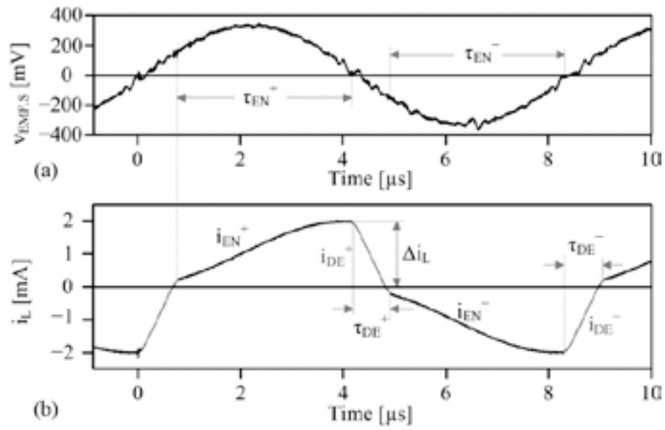

Fig. 4. Measured time-domain waveforms of the receiver coil's (a) EMF voltage and (b) current [35]–[36].

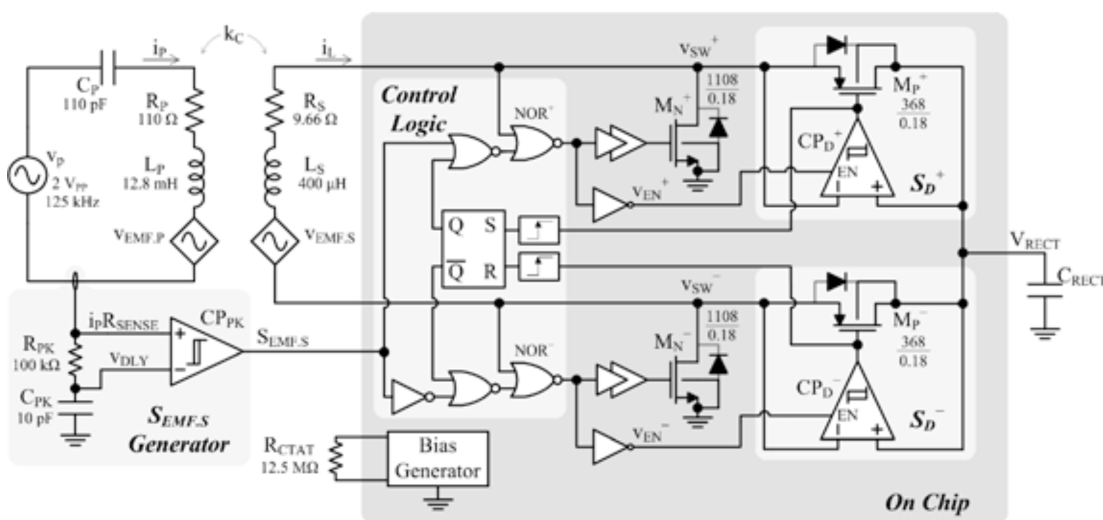

Fig. 5. Prototyped switched-inductor power receiver and charger, where transistor dimensions are in µm.

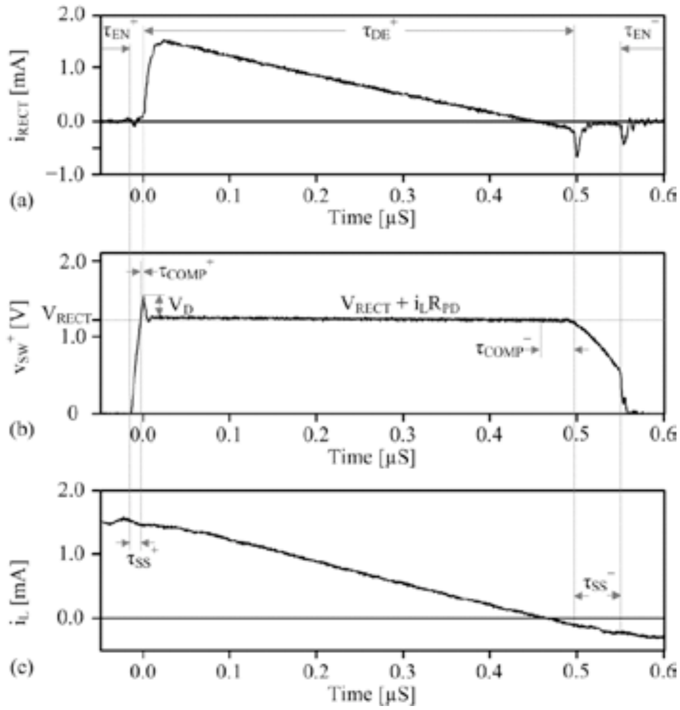

Fig. 6. Measured time-domain waveforms of (a) the rectified current, (b) the positive switching node voltage, and (c) the receiver coil current.

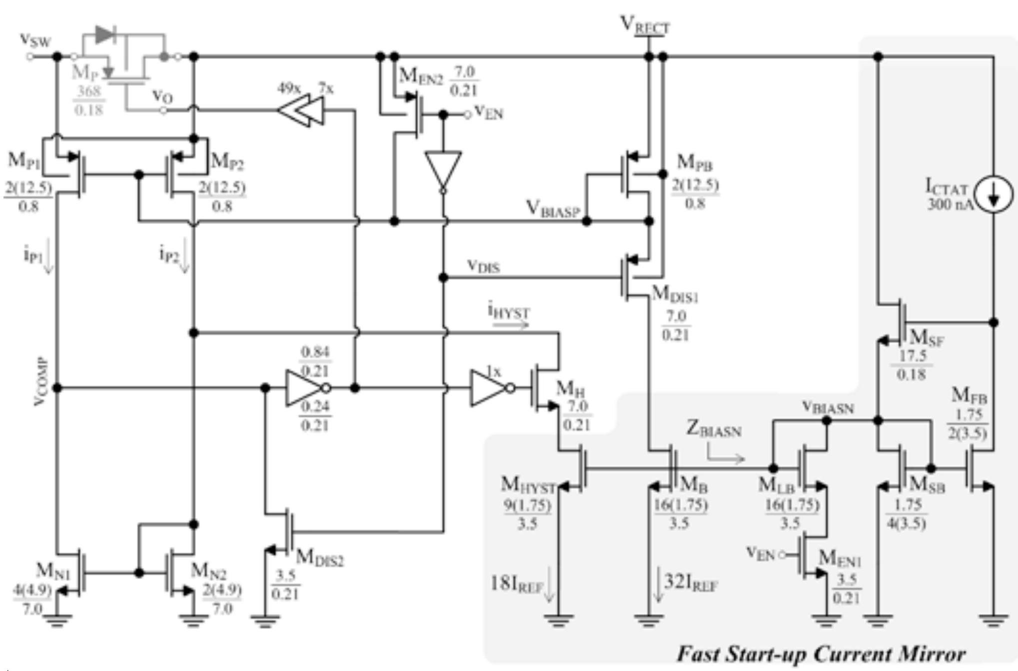

Fig. 7. M_P^+ and M_P^-'s synchronizing comparator, where n-type bulks are at ground and transistors dimensions are in μm.

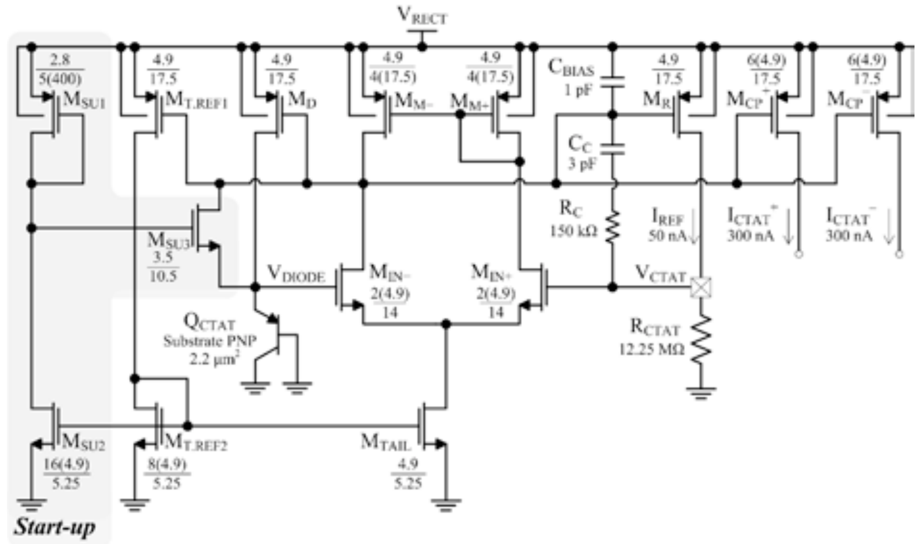

Fig. 8. CTAT current generator, where n-type bulks are at ground and transistors dimensions are in μm.

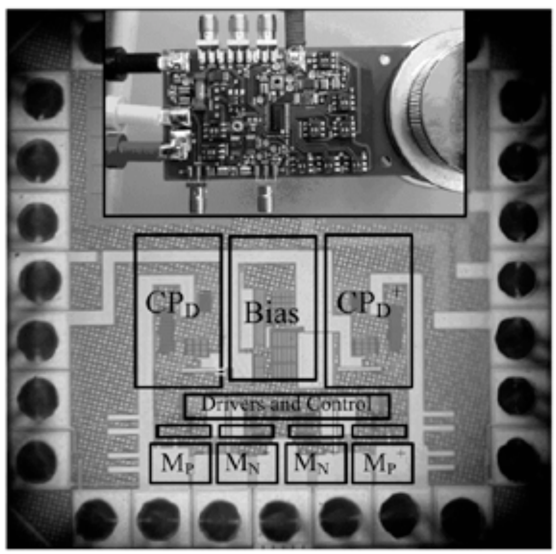

Fig. 9. Prototyped 180-nm CMOS IC and PCB.

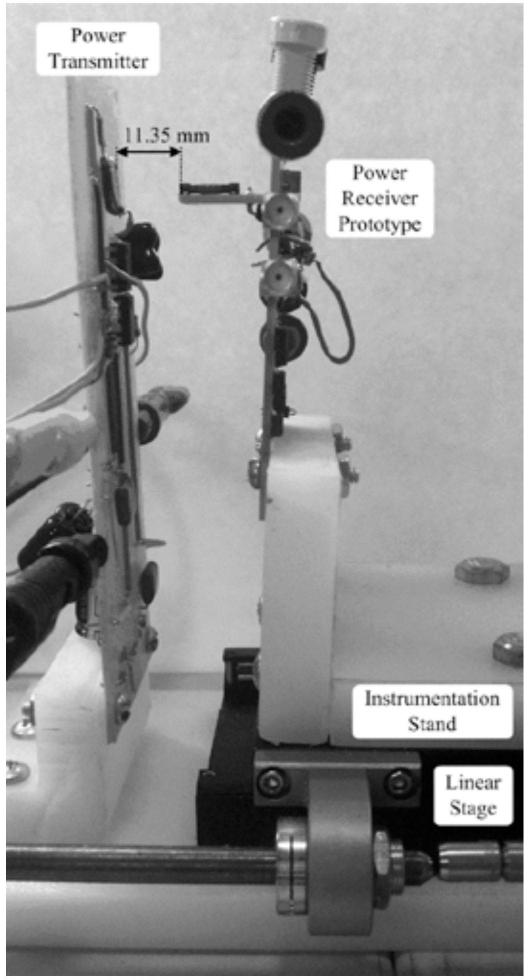

Fig. 10. Experimental setup.

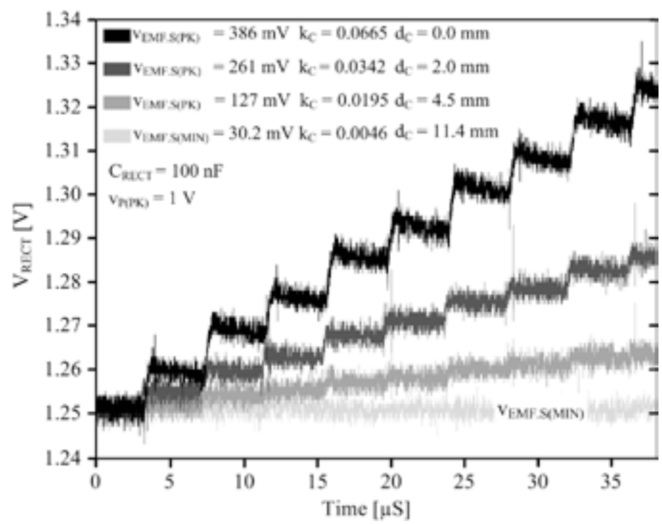

Fig. 11. Measured time-domain charging profiles for a 100-nF SMD ceramic capacitor at 125 kHz.

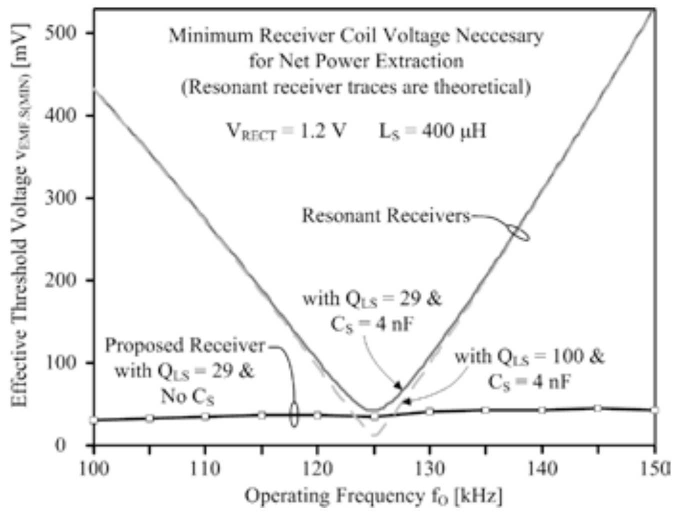

Fig. 12. Measured EMF threshold voltage of the proposed receiver and the theorized counterparts from resonant receivers across frequency.

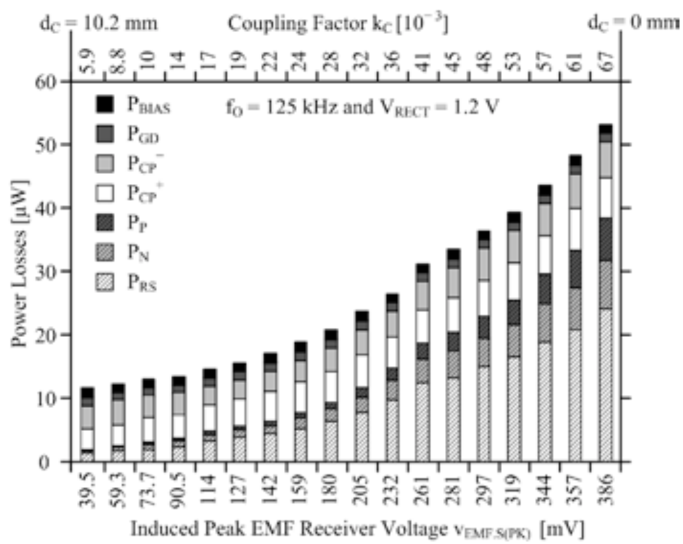

Fig. 13. Measured bias, gate-drive (GD), comparator (CP), p- and n-type switch, and ESR (RS) losses across EMF input power, or equivalently, across k_C, $v_{EMF.S(PK)}$, and distance d_C.

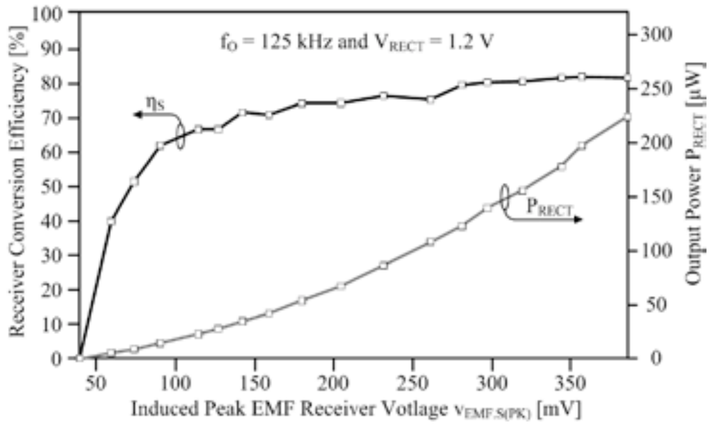

Fig. 14. Measured output power and receiver conversion efficiency across EMF input power, or equivalently, across k_C and $v_{EMF.S(PK)}$.

TABLE I: SWITCHING STATES AND TIMING SEQUENCE OF POWER SWITCHES.

State of $v_{EMF.S}$	Duration	$v_{SW}^+ - v_{SW}^-$	S_N^+	S_P^+	S_N^-	S_P^-
+	τ_{EN}^+	0	On	Off	On	Off
+/– Transition	τ_{DE}^+	V_{RECT}	Off	On	On	Off
–	τ_{EN}^-	0	On	Off	On	Off
–/+ Transition	τ_{DE}^-	$-V_{RECT}$	On	Off	Off	On

TABLE II: SUMMARY AND COMPARISON WITH THE STATE OF THE ART.

	ISSCC 2012 [41]	JSSC 2012 [25]	JSSC 2012 [42]	BIOCAS 2013 [43]	JSSC 2010 [24]	This Work
Technology	0.5 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
Resonant Capacitor C_S	336 pF#	220 pF	No Cs	33 pF#	141 pF#	No Cs
Minimum EMF Voltage Threshold $v_{EMF.S(MIN)}$	N/A	642 mV*	> 1.2 V†	34 mV*	78 mV*	30 mV
Receiver Quality Factor Q_{LS}	N/A	37	N/A	107	10	29
Receiver Efficiency η_S	Peak: 77%	N/A	93% (simulated)	70% – 87%	Peak: 55%	Avg: 76% Peak: 82%
Maximum Coil Separation $d_{C(MAX)}$	80 mm	1 mm	> 1 mm	20 mm	< 10 mm	11 mm
Output Voltage V_{RECT}	3.1 V	16.3 V	1.2 V	2.3 – 3 V	1.8 V	1 – 1.5 V
Operational Frequency f_O	13.56 MHz	6.78 MHz	13.56 MHz/ 6.78 MHz	13.56 MHz	13.56 MHz	100 – 150 kHz
Rectifier Type	Full-wave/ Doubling Resonant Receiver	Full-wave Resonant Receiver	Full-wave Rectifier	Full-wave Resonant Receiver	Multiplying Resonant Receiver	Inductor-based Current Rectifier

*$v_{EMF.S(MIN)}$ is calculated with $v_{C(MIN)}/Q_{LS}$, where $v_{C(MIN)}$ is the minimum resonant-tank voltage that allows power transfer (similar to Eq. (5))

#C_S is calculated using $2\pi f_O = 1/\sqrt{L_S C_S}$, where L_S and f_O are the reported values of receiver inductance and operational frequency

†Receiver is not resonant and requires $v_{EMF.S(MIN)}$ to be greater than V_{RECT}.