Achieving High Efficiency under Micro-Watt Loads with Switching Buck DC–DC Converters

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Abstract – The present-day and potential benefits of highly integrated miniaturized applications like wireless micro-sensors and biomedical implants in military, space, medical, and commercial markets fuel the demand for self-sustaining micro-electronic systems. Extending operational life to practical levels in such volume-constrained environments is difficult because space limits energy and power. Although switching dc-dc converters have been frequently used in power systems to supply and condition power efficiently, their quiescent and switching losses often render them inefficient at lighter loads, where micro-scale applications reside. Arbitrarily decreasing switching frequency with reductions in load, unfortunately, does not guarantee maximum efficiency because, for example, doing so in discontinuous-conduction mode also increases conduction losses. This paper therefore explores how power losses in switching dc-dc converters relate to load, switching frequency, and other design variables under extreme light loading conditions and ascertains how to manage them to achieve the highest possible efficiency across a micro-watt load. To that end, the paper discusses, analyzes, verifies, and graphically illustrates when and how each of the power-consuming mechanisms dominate efficiency performance. The results show that, after mode-hopping from continuous to discontinuous conduction when the load decreases below half the inductor ripple current, the switching frequency (and quiescent current) should decrease linearly with load at an optimal (derived) rate to balance the losses (and only use

just enough quiescent current to sustain the needed bandwidth) and yield maximum efficiency results (e.g., 85-95%) across the entire micro-power range. Simulations show that a constant peak-current control converter (as would a hysteretic converter) with the optimal frequency-load ratio achieves over 86% efficiency across a 50-500μA load range.

Keywords – Switching DC-DC Converter Supply, Micro-Watt Converter, Micro-Power Supply, Ultra Light Load Efficiency, Power Dominance, Wireless Micro-Sensor Power

1. Power Supplies in Micro-Power Applications

Micro-scale integration of sensors[1], batteries[2], fuel cells[3], microelectronics, and wireless telemetry[1] is inspiring a plethora of system-on-chip (SoC), system-in-package (SiP), and system-on-package (SoP) military, space, medical, and commercial applications that promise the ubiquity of the cellular phone, if not more. Wireless micro-sensors, for example, are not only unobtrusive and non-invasive but they can also retrofit existing difficult- and expensive-to-replace technologies such as power plants and power grids with state-of-the-art intelligence at a relatively minimal cost. Miniaturized platforms, however, constrain energy and power to critical thresholds, requiring re-charge or re-fuel cycles at a frequency that a network of difficult-to-reach sensors cannot typically tolerate. As a result, high-power efficiency, which ultimately determines the device's operational life, is of paramount importance, especially at low power levels, where micro-systems normally thrive[1].

The aim of on-chip power supplies is to deliver and condition power from a micro-scale energy source to the system efficiently. Linear regulators are relatively simple and introduce little-to-no noise but, because they conduct current with relatively high switch-on voltages, they suffer from higher power losses[4]. Although the switches in switched-capacitor supplies (charge pumps) do not sustain steady-state voltages while conducting current, they are nonetheless exposed to considerable voltages transiently, which means they still dissipate power[5]. Switches in magnetic- or inductor-based converters, on the other hand, sustain substantially lower voltages when they conduct current so their combined conduction losses are typically lower[6]. Needless to say, these fundamentally lower conduction losses offer appealing lifetime advantages to battery-powered micro-scale applications, which is the driving motivation behind this paper.

In practice, however, these dc-dc converters also suffer from quiescent and switching losses that do not scale with load current, as some conduction losses normally would. The result of

these losses when applied to micro-power applications can be severe. While optimizing static design variables such as inductance, capacitance, switch size, switching frequency, and output voltage may balance all relevant power losses at a particular load level, it does little to ensure tradeoffs remain favorable across a relatively wide micro-Watt load range, as a wireless micro-sensor, for instance, transitions from idling conditions to data-transmission mode. Dynamically adjusting some of these variables, however, offers the opportunity to maintain optimal design conditions across various operating states, which is why load-dependent mode-hopping schemes and variable frequency converters garner so much attention in commercial and research circles[7,8,9].

Arbitrarily decreasing the switching frequency of the supply with reductions in load power, however, does not guarantee power losses remain balanced because switching losses do not necessarily decrease at the same rate the resulting rise in inductor ripple current increases conduction losses. Different operating regions and modes exacerbate the difference in these rising and falling rates because their respective contributions vary[10,11]. While it is concluded that switching frequency should generally decrease with load current for high efficiency[12,13], this paper details, illustrates, identifies, and verifies how the various power-consuming mechanisms present in a magnetic-based converter shift and relate under the extreme micro-power conditions that micro-scale applications endure (e.g., less than 1mW), identifying in the process relevant design methodologies.

Although a synchronous step-down dc-dc converter, as shown in Fig. 1, by no means represents all plausible embodiments of inductive-based power supplies, it incurs all relevant power losses, from driver shoot-through losses to power-stage current-voltage overlap, Ohmic conduction, and gate-drive switching losses. Because this converter is relatively simple and it incorporates all the essential power components present in a magnetic-based switcher, such as an inductor, a capacitor, switches, drivers, a controller, etc., the foregoing

discussions use it to derive and draw general conclusions. Its asynchronous counterpart may be simpler architecturally and operationally but also incomplete, as it lacks the overlap losses normally present in applications that cannot tolerate the conduction loss associated with the asynchronous diode switch[14]. Section 2 revisits the origins of the power losses present in a synchronous buck converter with respect to load or output current I_O and switching frequency f_{SW} and Section 3 discusses when and how the various power loss groups identified dominate. Section 4 then examines and verifies how switching frequency should relate to load current under micro-power conditions to ensure optimal efficiency performance and Section 5 draws and extrapolates relevant conclusions.

2. Power Losses in Switching DC-DC Converters

Power losses generally fall into three major categories: (1) conduction, (2) switching, and (3) quiescent. Conduction losses refer to the Ohmic power dissipated in the parasitic series resistances and diodes present in the power-conducting switches (e.g., switch-on resistances and diodes in Fig. 1's M_P and M_N), inductors (e.g., $R_{L.ESR}$ in L), and capacitors (e.g., $R_{C.ESR}$ in C_O). Switching losses describe the energy needed to charge and discharge gate-drive capacitors (e.g., current i_C used to charge and discharge C_{GS} and C_{GD} in M_P and M_N), the energy lost due to the voltage-current overlaps across the switches (e.g., drain-source terminal voltages across M_P and M_N) and all other energy lost due to the switching actions of the converter. Finally, quiescent power refers to the steady-state current the controller in the feedback loop requires (e.g., I_Q) to function and operate at the prescribed switching frequency.

2.1. Conduction Losses

To start, it is worth noting high- and low-side switches M_P and M_N conduct almost all of inductor current i_L in alternate phases, which means their respective duty cycles d_{MP} and d_{MN} roughly complement one another; that is, d_{MN} is approximately $1\text{-}d_{MP}$. Collectively, as a

result, they present a single resistance R_{SW}, as shown in Fig. 1 (b), that is equivalent to the sum of their respective turn-on resistances R_{MP} and R_{MN} multiplied by their corresponding duty cycles:

$$R_{SW} \approx R_{MP} d_{MP} + R_{MN} d_{MN} \approx R_{MP} d_{MP} + R_{MN}\left(1 - d_{MP}\right) \quad (1)$$

Although not necessarily the case, R_{MP} is normally on the same order as R_{MN} so R_{SW}, R_{MP}, and R_{MN} are all about the same value (i.e., $R_{SW} \approx R_{MP} \approx R_{MN}$).

Decomposing inductor current i_L into its average and ac (or ripple) components $i_{L(avg)}$ and $i_{L(ac)}$ helps highlight the relative impact of the various Ohmic losses in the circuit. For instance, $i_{L(avg)}$ in the case of the buck converter shown in Fig. 1 (a) and modeled in Fig. 1 (b) does not flow continuously through C_O's $R_{C.ESR}$, but it does through L's $R_{L.ESR}$ and M_P and M_N's collective series resistance R_{SW}. As a result, $R_{L.ESR}$ and R_{SW} dissipate a dc conduction power $P_{C.DC}$ that is in direct proportion to $i_{L(avg)}^2$, in other words, to I_O^2:

$$P_{C.DC} = i_{L(avg)}^2\left(R_{SW} + R_{L.ESR}\right) = I_O^2\left(R_{SW} + R_{L.ESR}\right) \equiv I_O^2 R_{C.DC} \quad (2)$$

where $R_{C.DC}$ represents the converter's equivalent dc-conduction resistance.

Similarly, i_L's ripple $i_{L(ac)}$ also flows through R_{SW} and $R_{L.ESR}$, but instead of reaching the load, C_O and its parasitic $R_{C.ESR}$ steer $i_{L(ac)}$ to ground. Resistors R_{SW}, $R_{L.ESR}$, and $R_{C.ESR}$ therefore dissipate ac conduction power $P_{C.AC}$ that is in direct proportion to the square of $i_{L(ac)}$'s root-mean-square (RMS) value $i_{AC.RMS}^2$:

$$P_{C.AC} = i_{AC.RMS}^2\left(R_{L.ESR} + R_{C.ESR} + R_{SW}\right) \equiv i_{AC.RMS}^2 R_{C.AC} \quad (3)$$

where $R_{C.AC}$ is the converter's equivalent ac-conduction resistance. Note that in continuous-conduction mode (CCM), i_L is triangular in shape so $i_{AC.RMS(CCM)}$ depends on i_L's peak-peak value Δi_L, which means $i_{AC.RMS(CCM)}$ is directly proportional to the voltage across the inductor when M_P conducts (i.e., V_{IN}-V_O during d_{MP}) and inversely proportional to L's impedance Ls or Lf_{SW}, where f_{SW} is the switching frequency:

$$i_{AC.RMS(CCM)} = \frac{\Delta i_L}{\sqrt{12}} = \frac{(V_{IN} - V_O)d_{MP}}{Lf_{SW}\sqrt{12}} = \frac{V_{IN}(1 - d_{MP})d_{MP}}{Lf_{SW}\sqrt{12}} \qquad (4)$$

and ac conduction losses in CCM $P_{C.AC(CCM)}$ is

$$P_{C.AC(CCM)} = i_{AC.RMS(CCM)}{}^2 R_{C.AC} = \frac{[V_{IN}(1 - d_{MP})d_{MP}]^2}{12L^2 f_{SW}{}^2} R_{C.AC} \qquad (5)$$

When I_O drops below half ripple current Δi_L, i_L momentarily reverses direction (i.e., i_L becomes negative) and flows back to ground through R_{SW}. Allowing the converter to remain in CCM and sink this current constitutes an unnecessary power loss so, to avoid this loss, the controller normally shuts M_N off when i_L reaches zero[7], as shown in Fig. 2, allowing the converter to enter discontinuous conduction mode (DCM). Under these conditions, i_L is no longer triangular and the expression for $i_{AC.RMS}$ consequently changes. To extrapolate the mean-square fraction of ac current flowing into $R_{C.ESR}$ in DCM, the output current component is subtracted from the total mean-square inductor current $i_{L(RMS)}$, just as the load subtracts power from what is available in L:

$$i_{AC.RMS(DCM)}{}^2 = i_{L(RMS)}{}^2 - i_{L(avg)}{}^2 = \left(\frac{i_{L(peak)}{}^2}{3}\right)\left(\frac{t_\Delta}{T_{SW}}\right) - I_O{}^2 \qquad (6)$$

where $i_{L(peak)}$ is the peak inductor current and t_Δ is M_P and M_N's combined conduction period, which is now a fraction of switching period T_{SW} in DCM (Fig. 2). Since I_O is essentially the dc current i_L produces, that is, $i_{L(avg)}$ is I_O, $i_{L(peak)}$ increases with I_O and decreases with conduction period t_Δ:

$$i_{L(peak)} = 2i_{L(avg)}\left(\frac{T_{SW}}{t_\Delta}\right) = \frac{2I_O T_{SW}}{t_\Delta} \qquad (7)$$

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The fraction of time M_P conducts with respect to conduction period t_Δ in DCM is the same as the fraction of time M_P conducts with respect to switching period T_{SW} in CCM, which is

simply another way of referring to duty cycle d_{MP}, or equivalently, V_O/V_{IN}. This is true because L continues to be a dc short between switching node v_{SW} and v_O (i.e., $v_{SW(avg)}$ equals V_O) so M_P must therefore connect L to V_{IN} and ground at the same duty cycles it did in CCM. As a result, conduction duty-cycle d_{MP} is the ratio of conduction rise time $t_{L(rise)}$ to conduction period t_Δ:

$$t_\Delta = \frac{t_{L(rise)}}{d_{MP}} = \frac{i_{L(peak)}L}{d_{MP}(V_{IN} - V_{OUT})} = \frac{\left(\frac{2I_O T_{SW}}{t_\Delta}\right)L}{d_{MP}(V_{IN} - V_{OUT})} = \sqrt{\frac{2I_O T_{SW} L}{d_{MP}(1-d_{MP})V_{IN}}} \tag{8}$$

Substituting $i_{L(peak)}$ and t_Δ in $R_{C.ESR}$'s extrapolated RMS current $i_{AC.RMS(DCM)}$ for the above-derived equations yields:

$$i_{AC.RMS(DCM)}{}^2 = \left(\frac{i_{L(peak)}{}^2}{3}\right)\left(\frac{t_\Delta}{T_{SW}}\right) - I_O{}^2 = \frac{4}{3} I_O{}^{1.5}\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2Lf_{SW}}} - I_O{}^2 = \frac{4}{3} I_O{}^{1.5}\sqrt{I_{OB}} - I_O{}^2 \tag{9}$$

where I_{OB} represents I_O's value at the boundary of CCM and DCM operation (i.e., I_{OB} equals $0.5\Delta i_{L(CCM)}$) and ac conduction losses in CCM $P_{C.AC(CCM)}$ reduce to

$$P_{C.AC(DCM)} = i_{AC.RMS(DCM)}{}^2 R_{C.AC} = \left[\frac{4}{3} I_O{}^{1.5}\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2Lf_{SW}}} - I_O{}^2\right] R_{C.AC} \tag{10}$$

Under deep DCM conditions, when I_O is substantially below I_{OB}, the $I_O{}^2$ component in $i_{AC.RMS(DCM)}$ becomes negligibly smaller with respect to its counterpart, reducing $i_{AC.RMS(DCM)}$ and $P_{C.AC(DCM)}$'s dependence on I_O and f_{SW} to $I_O{}^{1.5}/f_{SW}{}^{0.5}$:

$$P_{C.AC(DCM)}\Big|_{I_O << I_{OB} \equiv 0.5\Delta i_L} = i_{AC.RMS(DEEP\ DCM)}{}^2 R_{AC} \cong \left(\frac{4}{3} I_O{}^{1.5}\sqrt{I_{OB}}\right) R_{AC} \propto \frac{I_O{}^{1.5}}{f_{SW}{}^{0.5}} \tag{11}$$

What is perhaps most important about this conclusion is that ac conduction losses in DCM depend on $I_O{}^{1.5}$ and $f_{SW}{}^{0.5}$, whereas in CCM, they depend on $f_{SW}{}^2$ alone.

2.2. Switching Losses

Switching power losses are all the losses attached to M_P and M_N's parasitic capacitors and diodes. The fact the converter incurs these losses every switching event, as capacitors charge and discharge and diodes temporarily conduct, is critical because their negative impact on efficiency increases with switching frequency f_{SW}. The eddy currents and core saturation in the inductor, as it turns out, also induce power losses every switching cycle, except they are negligibly small when compared against capacitor-derived losses. Similarly, skin effects, which are pronounced in conductors with multi-layer windings at high frequency under high currents[15], are normally insignificant at micro-Watt levels.

The fundamental loss in the gate capacitors is the energy required to charge them through a resistive switch: capacitor energy E_C is $C_{PAR}\Delta V_C^2$, where ΔV_C is the voltage variation in parasitic capacitor C_{PAR}. Gate-source capacitors C_{GSN} and C_{GSP} in M_N and M_P, for instance, require energy E_{GSN} and E_{GSP} to charge from zero to supply V_{IN} (i.e., $\Delta V_{GS} \approx V_{IN}$):

$$E_{GS} = E_{GSN} + E_{GSP} = C_{GSN}\Delta V_{GS}^2 + C_{GSP}\Delta V_{GS}^2 \approx (C_{GSN} + C_{GSP})V_{IN}^2 \tag{12}$$

Likewise, M_P's gate-drain capacitor C_{GDP} requires energy E_{GDP} to charge from $-V_{IN}$ (when M_N is off, M_P is on, and switching node v_{SW} is at V_{IN}) to $V_{IN}+V_{DN}$ (after M_P shuts off and M_N's diode pulls v_{SW} to a diode voltage below ground V_{DN} -during dead time-); in other words, ΔV_{GDP} is approximately $2V_{IN} + V_{DN}$. After dead time, M_N's gate-drain capacitor C_{GDN} charges from V_D (before M_N conducts) to V_{IN} (when M_N is fully engaged); that is, ΔV_{GDN} is roughly $V_{IN} - V_D$ and total gate-drain energy E_{GD} is

$$\begin{aligned} E_{GD} &= E_{GDP} + E_{GDN} = C_{GDP}\Delta V_{GDP}^2 + C_{GDN}\Delta V_{GDN}^2 \approx C_{GDP}(2V_{IN} + V_D)^2 + C_{GDN}(V_{IN} - V_D)^2 \\ &\approx (C_{GDN} + 4C_{GDP})V_{IN}^2 \end{aligned} \tag{13}$$

assuming V_D is considerably below V_{IN}. The average gate-drive power losses that result therefore reduce to

$$P_{SW.GD} = (E_{GS} + E_{GD})f_{SW} \approx \left[(C_{GSN} + C_{GSP})V_{IN}^2 + (C_{GDN} + 4C_{GDP})V_{IN}^2\right]f_{SW} = C_{GEQ}V_{IN}^2 f_{SW} \tag{14}$$

where C_{GEQ} is the equivalent switching capacitance present at the gates of M_N and M_P, the total value of which depends on the size of M_N and M_P.

As gate capacitors charge and discharge, while M_N or M_P conducts inductor current i_L, the conducting switch is temporarily exposed to a transitioning non-zero drain-source voltage v_{SW}, the current-voltage overlap of which induces an $i_L v_{SW}$ power loss across the conducting switch. In CCM, just before M_P turns on, for example, M_N's body diode conducts i_L's negative peak I_O-0.5Δi_L, switching node v_{SW} is below ground by a diode voltage V_{DN}, and M_P's source-drain voltage v_{SDP} is high, as illustrated at time equal zero in Fig. 3 (a), and as M_P engages, M_P's current i_P rises to i_L all the while v_{SDP} is high at V_{IN}+V_{DN} – the overlap area constitutes part of M_P's IV power loss $P_{IVP(CCM)}$. A similar event occurs when M_P disengages, as v_{SW} decreases and i_P decreases, which is why $P_{IVP(CCM)}$ reduces to

$$P_{IVP(CCM)} = (V_{IN} + V_{DN}) t_{OVER} I_O f_{SW} \qquad (15)$$

where t_{OVER} is the IV overlap time[15]. Although the model used[15] and Fig. 3 neglect the clamping effects parasitic bond-wire inductances induce, their influence is minimal when using multiple bond wires, as is typical in practice, with little to no performance trade-offs.

Power switch M_N also undergoes similar IV losses during CCM, except its drain-source voltage v_{DSN} is only exposed to diode voltage V_{DN} because dead time forces its body diode to conduct i_L and pull v_{SW} to -V_{DN} when M_N and M_P are both off, just before M_N is engaged and allowed to pull v_{SW} from -V_{DN} to zero:

$$P_{IVN(CCM)} \approx V_{DN} t_{OVER} I_O f_{SW} \qquad (16)$$

which means CCM IV losses combine to

$$P_{SW.IV(CCM)} = P_{IVP(CCM)} + P_{IVN(CCM)} \approx (V_{IN} + 2V_{DN}) t_{OVER} I_O f_{SW} \qquad (17)$$

In DCM, switching conditions are softer[12] because i_L is zero just after M_N disengages and

immediately before M_P engages, allowing M_N's v_{DSN} and M_P's v_{SDP} to transition with little-to-no current during M_N's turn-off and M_P's turn-on transitions, which means $P_{IVP(DCM)}$ and $P_{IVN(DCM)}$ reduce to

$$\begin{aligned} P_{IVP(DCM)} &= 0.5(V_{IN}+V_{DN})i_{L(peak)}t_{OVER}f_{SW} = 0.5(V_{IN}+V_{DN})\left(\frac{2I_O T_{SW}}{t_\Delta}\right)t_{OVER}f_{SW} \\ &= t_{OVER}(V_{IN}+V_{DN})\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2L}}\cdot\sqrt{I_O f_{SW}} \end{aligned} \tag{18}$$

$$P_{IVN(DCM)} = 0.5V_{DN}i_{L(peak)}t_{OVER}f_{SW} = t_{OVER}V_{DN}\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2L}}\cdot\sqrt{I_O f_{SW}}, \tag{19}$$

$$P_{SW.IV(DCM)} = P_{IVP(DCM)} + P_{IVN(DCM)} \approx t_{OVER}(V_{IN}+2V_{DN})\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2L}}\cdot\sqrt{I_O f_{SW}} \tag{20}$$

where $i_{L(peak)}$ is the peak inductor current in DCM.

During dead-time, when switches M_N and M_P are both off, because the inductor has energy and continues to demand current to flow to the output, M_N's parasitic diode forward biases and conducts i_L, pulling v_{SW} below ground by a diode voltage (V_{DN}). The diode therefore incurs a conduction loss during this time interval that is proportional to the product of V_{DN} and i_L. In CCM, for instance, i_L is at either its positive ($i_{L(+peak)}$ is I_O+0.5ΔI_L) or negative peak ($i_{L(-peak)}$ is I_O-0.5ΔI_L) during its transitions, giving an overall average value of I_O. The dead-time losses ($P_{SW.DT}$) in CCM are therefore proportional to V_{DN} and I_O, given $i_{L(+peak)}$ exceeds I_O by the same amount $i_{L(-peak)}$ falls below I_O:

$$P_{SW.DT(CCM)} = V_{DN}\left(i_{L(+peak)}+i_{L(-peak)}\right)\left(\frac{t_{DT}}{T_{SW}}\right) = 2V_{DN}t_{DT}I_O f_{SW}. \tag{21}$$

In DCM, however, dead-time conduction effectively occurs only when i_L is at its positive peak because its negative-peak counterpart is essentially zero, which means the negative peak experiences softer switching conditions. As a result, the expression for dead-time losses in DCM is similar in form to $P_{SW.DT(CCM)}$, but its dependence on I_O is less pronounced:

$$P_{SW.DT(DCM)} = V_{DN} i_{L(peak)} t_{DT} f_{SW} = V_{DN} t_{DT} \sqrt{\frac{2d_{MP}(1-d_{MP})V_{IN}}{L}} \sqrt{I_O f_{SW}} \qquad (22)$$

The drivers, because they do not normally incorporate dead-time features, incur shoot-through power losses when their respective supply and ground switches momentarily conduct shoot-through current i_{ST} (as shown in Fig. 3 (b)) at the same time. These Ohmic power losses are directly proportional to the square of V_{IN}, inversely proportional to combined switch-on resistances $R_{SW.DST}$, and the fraction of time they both conduct with respect to switching period T_{SW} or $1/f_{SW}$ (i.e., ratio of shoot-through time t_{DST} and switching period T_{SW}). Considering the size of each inverter in the driver chain is normally tapered, the inverter that drives the power switches, that is, the last inverter in the chain, incurs the most shoot-through losses:

$$P_{SW.DST} = \frac{2V_{IN}{}^2 t_{DST} f_{SW}}{R_{SW.DST}} \qquad (23)$$

2.3. Quiescent Losses

Feedback control, protection, and other vital functions require quiescent current to operate, and because input voltage V_{IN} normally supplies this current, the controller dissipates a quiescent power P_Q that is proportional to input supply V_{IN} and quiescent current I_Q:

$$P_Q = V_{IN} I_Q = E_Q f_{SW} + V_{IN} I_{Q0} \approx E_Q f_{SW} \qquad (24)$$

where E_Q refers to the quiescent energy required in each switching cycle and I_{Q0} to the frequency-independent quiescent current. As it turns out, quiescent power losses usually become strong functions of switching frequency because higher speeds demand more quiescent current. The fact is dominant and parasitic poles in the control loop shift to higher frequencies when I_Q increases because the effective resistance at each node in the circuit decreases with quiescent current (e.g., small-signal output resistance r_o or $1/\lambda I_Q$ in MOSFETs

and V_A/I_Q in BJTs). In other words, higher bandwidth f_{BW} demands higher switching frequency f_{SW} and lower parasitic resistance r_o, which means higher quiescent current I_Q and power P_Q:

$$P_Q \propto I_Q \propto \frac{1}{r_O} \propto f_{BW} \propto f_{SW}. \qquad (25)$$

2.4. Summary

TABLE I summarizes all the power losses present in a buck dc-dc switching regulator. Note that while dc conduction losses generally increase with the square of output current I_O, ac conduction losses are independent of I_O in CCM and increase with $I_O^{1.5}$ in DCM, during extreme light loading conditions. Similarly, while switching gate-drive and driver shoot-through losses increase with switching frequency f_{SW}, current-voltage overlap and dead-time losses increase with f_{SW} in CCM and $f_{SW}^{1.5}$ in DCM. Like gate-drive and shoot-through losses, quiescent current also increases with f_{SW}.

3. Dominancy of Power Losses and Efficiency

As shown in Section 2, output current I_O and switching frequency f_{SW} play pivotal roles in how much power a switching converter consumes. To understand their relative impact on efficiency across loads in micro-scale applications, it is helpful to cite a buck converter example confined to an off-chip 2mm x 2mm x 1mm 50μH power inductor with 5Ω of equivalent series resistance $R_{L.ESR}$, 0.6mm x 0.3mmx 0.3mm 100nF output capacitor with 1Ω of equivalent series resistance $R_{COUT.ESR}$, and a 50μA-10MHz CMOS controller[16] operated in sub-threshold, as tabulated in TABLE II. The relatively large series resistances associated with output filter L-C_{OUT} result because the devices are physically small, as constrained by the targeted micro-scale environment. Input and target-output voltages V_{IN} and V_{OUT} of 4V and 2V, respectively, were used, thereby producing a nominal high-side switch duty cycle d_{MP} of 50%. The physical dimensions of the power switches were 200μm/0.5μm for the

PMOSFET and 60μm/0.5μm for the NMOSFET (to balance conduction and switching losses) so their resulting turn-on resistance was approximately 48Ω and the equivalent gate-drive capacitance was 0.75pF, as prescribed by AMI's CMOS 0.5μm process technology. An equivalent driver shoot-through resistance of 5kΩ was calculated by assuming two-stage inverter chains with a tapering factor of three. In the end, the 50μH inductor produced a current ripple Δi_L of 2mA at the prescribed switching frequency of 10MHz.

Fig. 4 illustrates how these power losses change with load and how they ultimately affect efficiency η, which is the ratio of output load power P_{LOAD} and total input power P_{IN}:

$$\eta = \frac{P_{LOAD}}{P_{IN}} = \frac{P_{LOAD}}{P_{LOAD} + P_{LOSS}} \qquad (26)$$

where power losses P_{LOSS} is the summation of all the contributions described in Section 2 and summarized in TABLE II:

$$P_{LOSS} = P_{C.DC} + P_{C.AC} + P_{SW.IV} + P_{SW.GD} + P_{SW.DT} + P_{SW.DST} + P_Q \qquad (27)$$

Note the converter enters DCM (the shaded region in Fig. 4) when load current I_O falls below half inductor current ripple Δi_L, that is, when I_O is less than $0.5\Delta i_L$ (1mA in this case) because DCM operation is more suitable for extreme light loads (since power cannot be wasted in conducting negative inductor current). Although dc conduction losses $P_{C.DC}$ dominate at considerably high loads (as expected but not shown in Fig. 4) because $P_{C.DC}$ increases with the square of I_O, load-independent losses like quiescent and gate-drive switching losses P_Q and $P_{SW.GD}$ ultimately dominate at extreme light loading conditions, when I_O has negligible effects on power losses. Efficiency η, as a result, falls sharply at micro-power levels, which explains why magnetic-based switching converters are conventionally not used for this application space. Note, however, power losses and efficiency in this regime depend strongly on switching frequency f_{SW} because not only does $P_{SW.GD}$ increase with f_{SW} but so does quiescent current I_Q and therefore P_Q, which means changes in f_{SW} have a considerable

impact on η. (Notice the paper's focus is ultra low-power applications like wireless micro-sensors and not the entire gamut of mobile hand-held battery-operated devices, which is why this and ensuing graphs only depict ultra light loads ranging up to 2mA or 4mA, rather than the expanded range mobile products can demand. The fact is power dominance shifts almost linearly in the ultra light load region so sub-ranged linear scales tend to illustrate them best – a log scale would obscure shifts (cross points) in power dominance on the higher end of the range.)

While reducing f_{SW} in DCM (e.g., when P_{LOAD} is less than 1mW) decreases quiescent and switching losses, it also increases ac conduction losses $P_{C.AC}$ because inductor peak current $i_{L(+peak)}$ must necessarily increase to accommodate for a longer period. This means efficiency performance does not necessarily increase with decreasing switching frequencies. Note, however, η in the case shown in Fig. 4 would indeed increase with a reduction in f_{SW} but the point here is there will be an optimum point where further reductions in f_{SW} will again degrade η. In other words, there is an optimum relationship between f_{SW} and I_O that incurs the least losses and achieves the highest efficiency possible.

Power-Loss Contours across I_O and f_{SW}

Fig. 5 illustrate graphically how each of the losses described in Section 2 and tabulated in TABLE I change with load I_O and switching frequency f_{SW}. Fig. 5 (a), for example, shows dc conduction losses $P_{C.DC}$ decrease with the square of I_O and remains independent of f_{SW} across the entire load range. AC conduction losses $P_{C.AC}$, also shown in Fig. 5 (a), is dependent on f_{SW} across the entire load range and independent of I_O only in CCM. Note, however, $P_{C.AC}$'s dependence on f_{SW} changes in the two regions: inversely proportional to f_{SW}^2 in CCM and inversely proportional to $f_{SW}^{0.5}$ in DCM. Generally, ac conduction losses increase sharply at low switching frequencies.

While gate-drive and driver shoot-through switching losses $P_{SW.GD}$ and $P_{SW.DST}$ and quiescent power losses P_Q (Fig. 5(b), (c)) consistently decrease with f_{SW} and remain independent of I_O, current-voltage overlap and dead-time switching losses $P_{SW.IV}$ and $P_{SW.DT}$ do not. The fact is $P_{SW.IV}$ and $P_{SW.DT}$ increase with both I_O and f_{SW} in CCM and $I_O^{0.5}$ and $f_{SW}^{0.5}$ in DCM, as Fig. 5(b) demonstrates. (The axes are reversed in $P_{SW.IV}$ and $P_{SW.DT}$ to better illustrate how they change with I_O and f_{SW}.)

Ultimately, from a designer's perspective, what matters most is not that these losses depend on I_O and f_{SW} but how they compare against one another. The designer's objective is not necessarily to minimize all losses unilaterally but to increase efficiency with minimal cost and risk, which means focusing time, effort, silicon and printed-circuit board (PCB) real estate, and quiescent current on decreasing the dominant losses first, the ones that have a more pronounced effect on efficiency. To this end, it is helpful to combine all the loss contours illustrated in Fig. 5 in one graph, as shown in Fig. 5(d). (Note the 10MHz plane in Fig. 5(d) corresponds to the two-dimensional graph shown in Fig. 4.) Generally, as depicted from the graph, dc conduction losses $P_{C.DC}$ overwhelm most other losses at heavy loads, as expected, but only if f_{SW} is sufficiently high to keep ripple current Δi_L low and consequently induce lower ac conduction losses $P_{C.AC}$. At light loads, quiescent and switching gate-drive losses P_Q and $P_{SW.GD}$ dominate, as before, except decreasing f_{SW} considerably reduces them and their impact on efficiency.

4. Achieving Maximum Micro-Power Efficiency

4.1. Analysis

Quantifying the optimum operating point (e.g., f_{SW}) of the converter intuitively (from a designer's perspective) from the combined graph in Fig. 5 is not straightforward because not only are there too many variables to consider but their dependence on I_O and f_{SW} is also inconsistent. So, reducing the problem by grouping all power losses that show similar

dependence to I_O and f_{SW} is reasonable and appealing. Then, identifying the power groups that dominate the various load ranges further simplifies the problem. With this in mind, it is worthwhile to note power losses in the micro-power region fall into four distinct I_O- and f_{SW}-dependant groups: (1) $I_O^2 f_{SW}^0$ or $P_{I_O^2}$ (i.e., $P_{C.DC}$), (2) $I_O^0 f_{SW}^1$ or $P_{f_{SW}}$ (i.e., $P_{SW.GD}$, $P_{SW.DST}$, and P_Q), (3) $I_O f_{SW}$ or $P_{I_O f_{SW}}$ (i.e., $P_{SW.DT}$ and $P_{SW.IV}$), and (4) $I_O^{1.5} f_{SW}^{-0.5}$ or $P_{I_O^{1.5} f_{SW}^{-0.5}}$ (i.e., $P_{C.AC}$).

Combining these power groups into a single graph, as shown in Fig. 6(a), illustrates how reducing $P_{f_{SW}}$ and $P_{I_O^{1.5} f_{SW}^{-0.5}}$ decreases the dominant power losses present under extremely light loads; similarly, decreasing $P_{I_O^2}$ and $P_{I_O^{1.5} f_{SW}^{-0.5}}$ achieves the same objective at heavier loads. What this means is that efficiency (Fig. 6(b)) is highest when f_{SW} at light loads is just low enough to balance $P_{f_{SW}}$ and $P_{I_O^{1.5} f_{SW}^{-0.5}}$. The two-dimensional mapping at the base of Fig. 6(b) illustrates the I_O-f_{SW} regions of dominance, verifying the importance of $P_{I_O^{1.5} f_{SW}^{-0.5}}$ across the entire load range and how $P_{f_{SW}}$ supersedes $P_{I_O^2}$ in the low-power regime. The highest efficiencies occur near the boundaries, where power losses are balanced. Note that, because decreasing I_O and f_{SW} reduces $P_{I_O f_{SW}}$ and $P_{I_O f_{SW}}$ is low to begin with, $P_{I_O f_{SW}}$ does not normally dominate any region.

In more explicit terms, an optimum relationship exists between switching frequency f_{SW} and load I_O where power groups balance. Balancing losses, however, does not necessarily imply equating power groups, or arbitrarily decreasing f_{SW} with I_O, because linear reductions in f_{SW}, for instance, decrease $P_{f_{SW}}$ linearly but increase $P_{I_O^{1.5} f_{SW}^{-0.5}}$ nonlinearly. So, in review, light load efficiency η_{LT} is the ratio of load power P_{LOAD} to total input power P_{IN} or the sum of P_{LOAD} and all losses P_{LOSS}, the latter of which is mostly comprised of $P_{f_{SW}}$ and $P_{I_O^{1.5} f_{SW}^{-0.5}}$ at low power levels:

$$\eta_{LT} = \left.\frac{P_{LOAD}}{P_{LOAD} + P_{LOSS}}\right|_{\downarrow P_{LOAD}} \approx \frac{P_{LOAD}}{P_{LOAD} + P_{f_{SW}} + P_{I_O^{1.5} f_{SW}^{-0.5}}} = \frac{V_{OUT} I_O}{V_{OUT} I_O + E_{f_{SW}} f_{SW} + K_{C.AC} I_O^{1.5} f_{SW}^{-0.5}} \tag{28}$$

where $E_{f_{SW}}$ refers to the energy lost in each cycle as a result of $P_{f_{SW}}$ and $K_{C.AC}$ is the design constant associated with $P_{I_O^{1.5} f_{SW}^{-0.5}}$:

$$E_{f_{SW}} = E_{SW.GD} + E_{SW.DST} + E_Q = C_{G.EQ} V_{IN}^{\ 2} + \frac{2 V_{IN}^{\ 2} t_{ST}}{R_{SW.ST}} + E_Q \tag{29}$$

$$K_{C.AC} = \frac{4}{3} R_{C.AC} \sqrt{\frac{d_{MP}(1 - d_{MP}) V_{IN}}{2L}} \tag{30}$$

From here, one means of ascertaining a target switching frequency with respect to load I_O is to fix light-load efficiency η_{LT} to a prescribed target value and solve for f_{SW} in terms of I_O. When graphing the results on a two-dimensional graph of f_{SW} and I_O for various target efficiencies, as shown in Fig. 7, a family of equal-efficiency curves results. Super-imposing the power-dominance mapping shown in Fig. 6(b) onto Fig. 7 reveals two important conclusions: (1) the highest light-load efficiencies (when I_O is less than 1mA) occur near the $P_{f_{SW}} - P_{I_O^{1.5} f_{SW}^{-0.5}}$ boundary, but not exactly at the boundary, as demonstrated in Fig. 7, and (2) efficiencies above 90% are possible at load currents nearing 50μA (in the micro-power regime).

Strictly speaking, for the best possible performance, maximizing efficiency by tuning f_{SW} amounts to differentiating η_{LT} with respect to f_{SW}, equating to zero (for maximum efficiency), and solving for optimum switching frequency $f_{SW(opt)}$:

$$\left.\frac{\partial \eta_{LT}}{\partial f_{SW}}\right|_{f_{SW(opt)}} = -V_{OUT} I_O \left(E_{f_{SW}} - 0.5 K_{C.AC} I_O^{1.5} f_{SW(opt)}^{-1.5} \right) \equiv 0 \tag{31}$$

or

$$\frac{f_{SW(opt)}}{I_O} = \left(\frac{K_{C.AC}}{2E_{f_{SW}}}\right)^{\frac{2}{3}} \tag{32}$$

which means $P_{f_{SW(opt)}}$ should be half of $P_{I_O^{1.5} f_{SW(opt)}^{-0.5}}$, in other words, half of ac conduction losses $P_{C.AC}$:

$$P_{f_{SW(opt)}} = 0.5 P_{I_O^{1.5} f_{SW(opt)}^{-0.5}} = 0.5 P_{C.AC} \tag{33}$$

and

$$\begin{aligned}\eta_{LT(\max)} &\approx \frac{V_{OUT}}{V_{OUT} + E_{f_{SW}}\left(\frac{f_{SW(opt)}}{I_O}\right) + K_{C.AC}\left(\frac{I_O}{f_{SW(opt)}}\right)^{0.5}} = \frac{V_{OUT}}{V_{OUT} + E_{f_{SW}}\left(\frac{f_{SW(opt)}}{I_O}\right)(0.5+1)} \\ &= \frac{1}{1 + \frac{1.5\left(E_{f_{SW}}\right)^{\frac{1}{3}}\left(K_{C.AC}\right)^{\frac{2}{3}}}{(2)^{\frac{2}{3}} V_{OUT}}}\end{aligned} \tag{34}$$

4.2. Maximizing Efficiency in a Buck Converter

Note ratio $f_{SW(opt)}/I_O$ is a constant, which means the product of optimum switching period $T_{SW(opt)}$ and I_O is also fixed. In other words, maximum efficiency occurs when inductor L delivers (in every switching cycle) the optimum amount of charge $Q_{L(opt)}$ ($T_{SW(opt)}I_O$) to the load. In applying this condition to a practical switching buck converter, it is best to adopt a control scheme that automatically modulates f_{SW} to keep the charge-per-cycle delivered to the load constant, such as constant peak-current, constant on-time, and constant ripple voltage (output hysteresis) control[13]. For example, when considering a peak-current control scheme and using the constant derived for I_O/f_{SW} in this section to achieve maximum light-load efficiency (in DCM), peak current $i_{L(peak)}$ should be

$$i_{L(peak)} = \left(\frac{2I_O}{f_{SW}}\right)\left(\frac{1}{t_\Delta}\right) = \left(\frac{2I_O}{f_{SW}}\right)\sqrt{\left(\frac{f_{SW}}{I_O}\right)\left(\frac{d_{MP}(1-d_{MP})V_{IN}}{2L}\right)} \tag{35}$$

$$= \left(\frac{2E_{f_{SW}}}{K_{C.AC}} \right)^{\frac{1}{3}} \sqrt{\frac{2d_{MP}(1-d_{MP})V_{IN}}{L}},$$

where t_Δ is the conduction period.

Applying this result to the buck-converter example cited earlier in the paper and assuming frequency-independent quiescent current I_{Q0} is 1.25μA (i.e., P_{Q0} is 5μW) means $f_{SW(opt)}$ is $2.33 \times 10^9 I_O$ and $i_{L(peak)}$ should therefore be kept at 4.2mA, producing a theoretical efficiency slightly above 90% (dashed line in Fig. 7). To validate this conclusion, a peak-current controlled buck-converter circuit (whose simplified schematic is shown in Fig. 8(a)) was simulated and its efficiency performance plotted in Fig. 8(b). Although peak efficiency was slightly below 90% and the best performance occurred at a peak current (4mA) that is slightly below its theoretical prediction (4.2mA), the difference in performance was less than 1%. The reason for this discrepancy is that theory (at light loads) neglected minor terms in P_{LOSS} such as dc conduction losses $P_{C.DC}$, current-voltage overlap losses $P_{SW.IV}$, etc. Nevertheless, increasing and decreasing $i_{L(peak)}$ from the optimum value produced degraded results, which means 4.0-4.2mA is indeed the optimum setting. Notice the conclusions drawn expand to converters fabricated in other process technologies (other than 0.5μm CMOS), albeit at slightly different values (given differences in oxide thicknesses and carrier mobilities), because the basic power-inducing mechanisms present in switching converters remain unchanged across technology nodes. Also note there is a portion of quiescent current that depends on the bandwidth of the system, which means that portion should also decrease with I_O, as $f_{SW(opt)}$ decreases and its resulting bandwidth requirement relaxes.

5. Conclusions

This paper demonstrates that switching buck dc-dc converters under micro-Amp loads (50-500μA) suffer mostly from switching losses (which include bandwidth-dependent quiescent losses) and ac conduction losses, and operating a converter in discontinuous-conduction

mode (DCM) and decreasing its switching frequency (f_{SW}) with reductions in output load current (I_O) balances and minimizes these power losses. The paper further shows that relating f_{SW} (and quiescent current) to I_O at the derived optimum (which is a constant) can yield efficiencies of 85-95%, even when only loaded with micro-Watts. In other words, maximum efficiency occurs when the amount of charge transferred to the load is at an optimum constant, which also means (as shown in the paper) constant peak-current controlled and hysteretic (i.e., sliding-mode) buck dc-dc converters can be configured to yield maximum light load efficiencies. The high-efficiency features of magnetic-based switching supplies therefore extend to micro-power applications, where charge pumps and linear regulators were thought to dominate. This is particularly important because (i) micro-scale devices may only draw a few micro-Watts at a time (at considerably low duty cycles) and idle for the remainder of the period and (ii) the miniaturized batteries they embed severely restrain how much total energy is available. These conclusions intimate that low-power wireless micro-sensors, to cite an example, self-powered from embedded thin-film lithium-ion batteries and/or onboard energy harvesters can now enjoy the lifetime performance that results from using 85-95% efficient conditioning supplies.

ACKNOWLEDGMENTS

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FIGURES AND TABLES

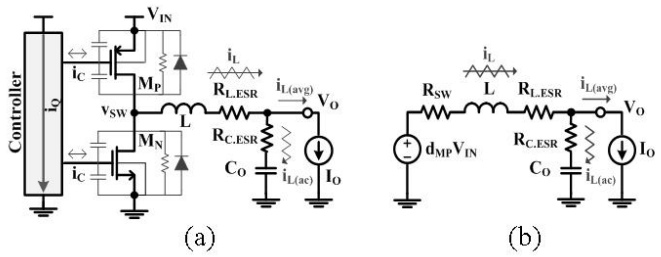


Figure 1. (a) A synchronous buck dc-dc converter and parasitic devices, and (b) an equivalent conduction-loss Model

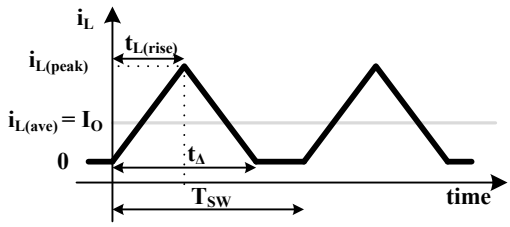


Figure 2. Inductor current in DCM

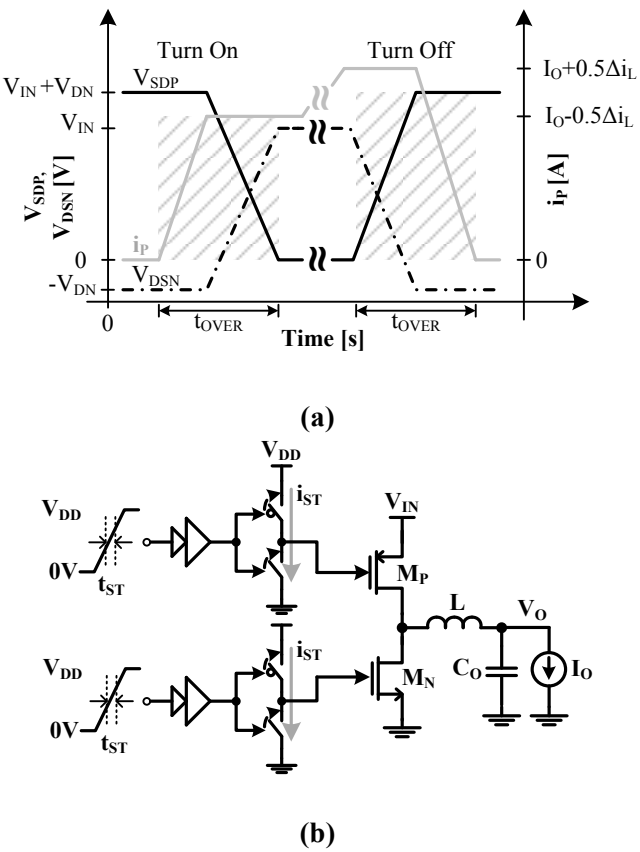


Figure 3. (a) IV overlap power losses in M_P and M_N (b) Shoot-through losses in M_P and M_N's driver chains.

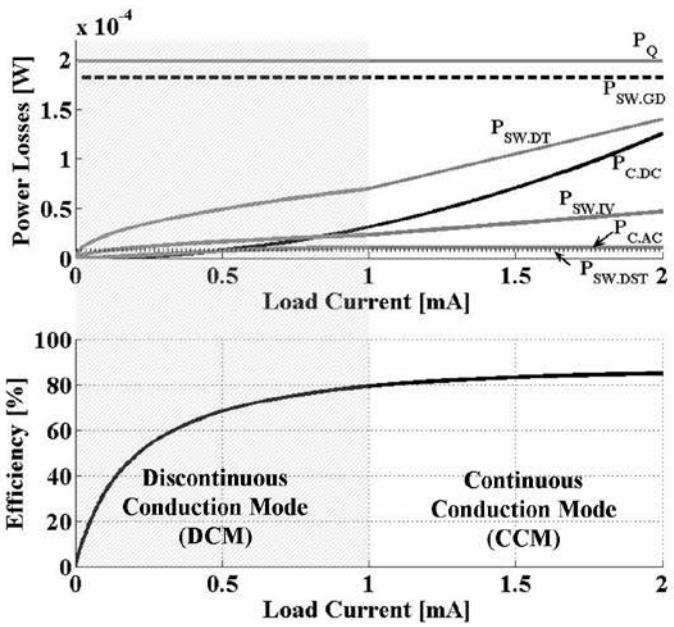
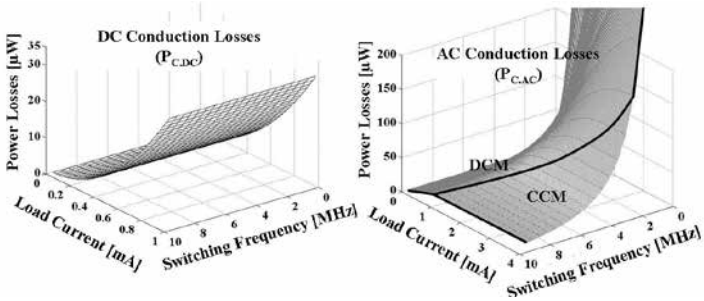
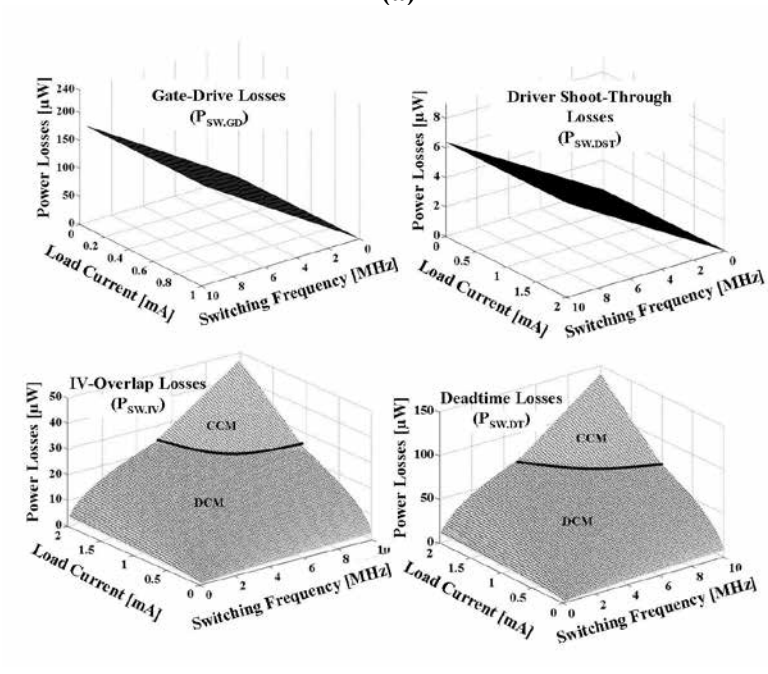


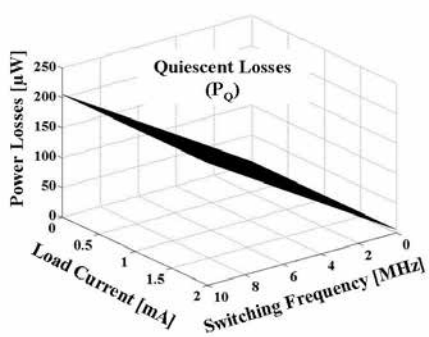
Figure 4. Power losses and efficiency of the buck converter across a 0-2mA load.



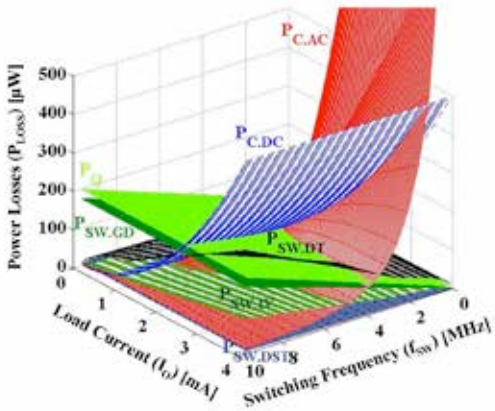
(a)



(b)

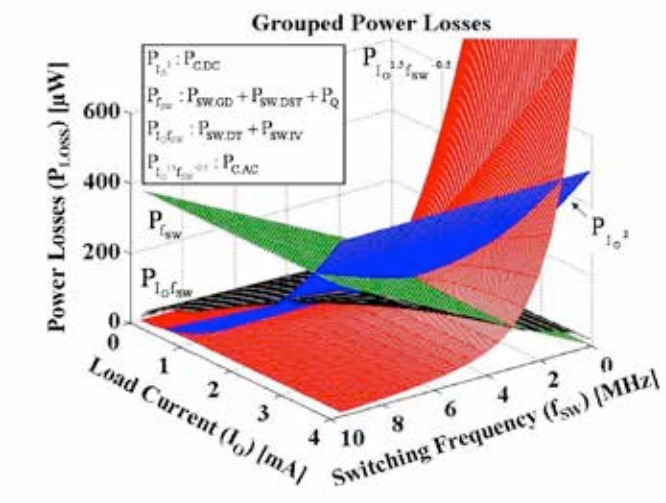


(c)

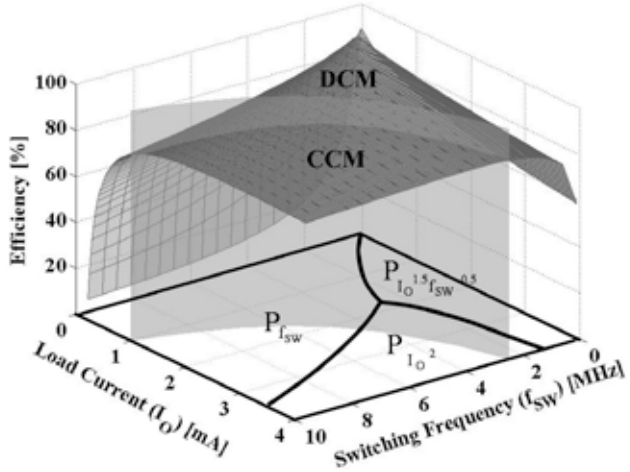


(d)

Figure 5. (a) Conduction losses, (b) Switching losses, (c) Quiescent losses in CCM and DCM, and (d) all relevant power losses combined in one graph



(a)



(b)

Figure 6. (a) Combined power losses and (b) resulting efficiency and dominance mapping of a switching buck converter across load and switching frequency.

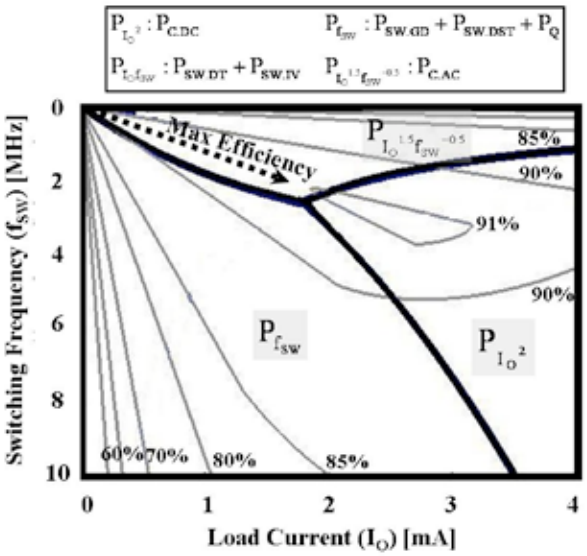
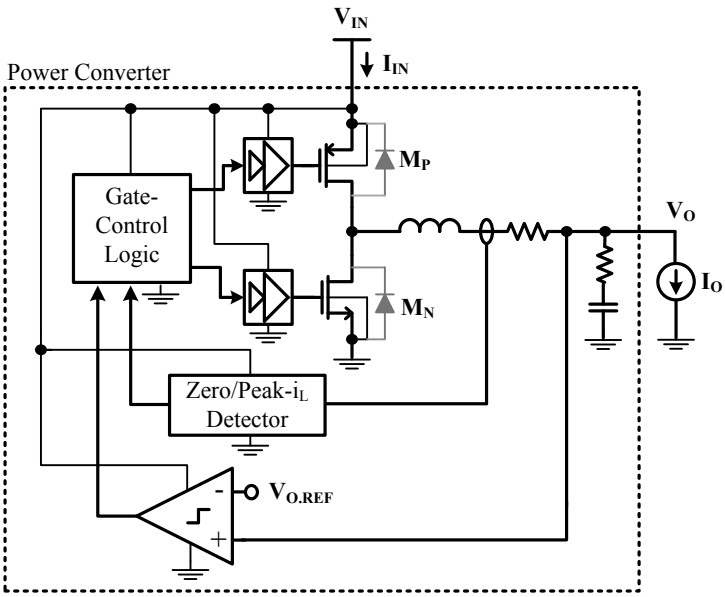
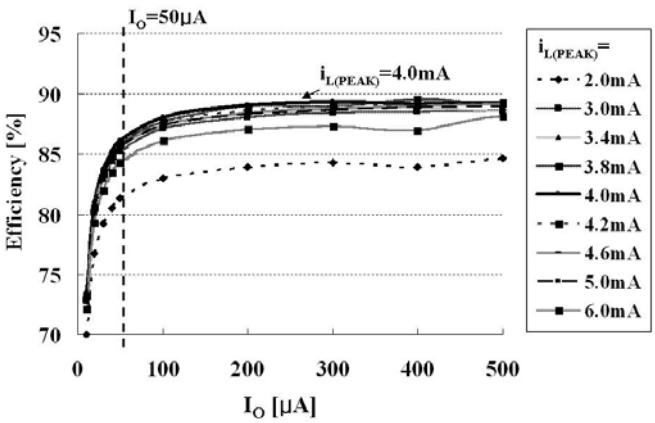


Figure 7. Family of equal-efficiency curves superimposed with the power-dominance mapping from Figure 6(b)



(a)



(b)

Figure 8. (a) Peak-current controlled buck-converter circuit and (b) its simulated efficiency at various peak-current settings.

TABLE I
SUMMARY OF POWER LOSS EXPRESSIONS

Category	Power Losses	CCM	DCM
Conduction Losses	$P_{C.DC}$	$I_O^2(R_{SW}+R_{L.ESR})$	
	$P_{C.AC}$	$\frac{[d_{MP}(1-d_{MP})V_{IN}]^2}{12L^2f_{SW}^2}(R_{SW}+R_{L.ESR}+R_{C.ESR})$	$\left[\frac{4}{3}I_O^{1.5}\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2Lf_{SW}}}-I_O^2\right](R_{SW}+R_{L.ESR}+R_{C.ESR})$
Switching Losses	$P_{SW.GD}$	$C_{G.EQ}V_{IN}^2f_{SW}$	
	$P_{SW.IV}$	$(V_{IN}+2V_{DN})t_{OVER}I_Of_{SW}$	$t_{OVER}(V_{IN}+2V_{DN})\sqrt{\frac{d_{MP}(1-d_{MP})V_{IN}}{2L}}\sqrt{I_Of_{SW}}$
	$P_{SW.DT}$	$2v_{DN}t_{DT}I_Of_{SW}$	$V_{DN}t_{DT}\sqrt{\frac{2d_{MP}(1-d_{MP})V_{IN}}{L}}\sqrt{I_Of_{SW}}$
	$P_{SW.DST}$	$\frac{2V_{IN}^2t_{DST}f_{SW}}{R_{SW.DST}}$	
Quiescent Losses	P_Q	$V_{IN}I_Q \approx E_Qf_{SW}$	

TABLE II
PARAMETERS OF A BUCK CONVERTER

Input Voltage	V_{IN}	4V
Output Voltage	V_{OUT}	2V
Load Current	I_O	< 10mA
Quiescent Current @ 10MHz	I_Q	50µA
Switching Frequency	f_{SW}	10MHz
Inductance	L	50µH
Inductor's ESR	$R_{L.ESR}$	5Ω
Output Capacitor	C_{OUT}	100nF
Output Capacitor's ESR	$R_{COUT.ESR}$	1Ω
Switch-On Resistance	R_{SW}	48Ω
Equivalent Gate Capacitance	$C_{G.EQ}$	0.75pF
Dead Time	t_{DT}	5ns
IV-Overlap Time	t_{OVER}	0.5ns
Driver Shoot-Through Time	t_{DST}	0.1ns
Driver Shoot-Through Resistance	$R_{SW.DST}$	5kΩ

BIOGRAPHIES

Suhwan Kim received the B.S. degree in electrical engineering from Seoul National University in 2002, and the M.S. degree in electrical and computer engineering from Georgia Institute of Technology. He joined Georgia Tech Analog & Power IC laboratory to pursue the Ph. D. in October 2006, under the guidance of Dr. Gabriel A. Rincón-Mora. His research area is power management circuit design for micro-scale systems. Most recently, he is working on the Self Powered Chip project supported by the NUWC (Naval Undersea Warfare Center), designing a power management IC for hybrid energy sources.

Gabriel A. Rincón-Mora (B.S., M.S., and Ph.D.) worked for Texas Instruments in 1994-2003, was appointed Adjunct Professor for Georgia Tech in 1999-2001, and became a full-time faculty member at Georgia Tech in 2001. His scholarly products include 7 books (as sole author), 1 book chapter, over 123 scientific publications, 26 patents, and over 26 commercial power management chip designs. He received the "National Hispanic in Technology Award" from the Society of Professional Hispanic Engineers, the "Charles E. Perry Visionary Award" from Florida International University, a “Commendation Certificate” from the Lieutenant Governor of California, an IEEE Service Award from IEEE CASS MWSCAS, and “Orgullo Hispano” and “Hispanic Heritage” awards from Robins Air Force Base. He was inducted into the "Council of Outstanding Young Engineering Alumni" by Georgia Tech, elected Distinguished Lecturer by IEEE’s CASS for 2009-2010, and featured on the cover of Hispanic Business Magazine as one of “The 100 Most Influential Hispanics,” La Fuente (Dallas publication), and three times on Nuevo Impacto (Atlanta magazine).

Dr. Rincón-Mora is (was/has been) an Associate Editor for IEEE's Transactions on Circuits

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