

Low-Power CMOS Ramp Generator Circuit for DC–DC Converters

H. Pooya Forghani-zadeh* and Gabriel A. Rincón-Mora

Analog and Power IC Lab, School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332
forghani@ece.gatech.edu, rincon-mora@ieee.org

Abstract — Ramp-signal generators are particularly critical in controlling the frequency and duty-cycle of pulse-width modulated (PWM) switching supplies. They are normally implemented with a timed charging current source into a capacitor and a reset switch controlled by two comparators whose reference signals set the lower and upper limits of the ramp. A fast comparator is required to ensure the reset operation is short and therefore mitigate its adverse effects on switching supply frequency. Unfortunately, the resulting delay requirements of the comparator are often stringent and difficult to meet under low power conditions. To alleviate the comparator’s bandwidth requirement, a scheme is proposed by which the circuit generates a non-ideal ramp with its reset time to be 10% of period utilizing the fact that the ramp signal is needed in DC-DC converter’s controller feedback loop only until the duty-cycle is set. Therefore, the condition on comparator delay and its respective power is relaxed. The proposed scheme was experimentally verified with a 770 kHz ramp generator prototype embedded in a current-mode controller buck DC-DC converter built in a 0.5- μm CMOS process, which achieved 28 mV amplitude accuracy with current consumption of 256 μA .

Keywords — Signal generator, ramp generator, DC-DC converter, switching regulator, low power, power efficient.

1 INTRODUCTION

Among others, ramp- and pulse-signal generators are critical building blocks in built-in self-test (BIST), phase-locked loop (PLL), neural network, and pulse-width modulated (PWM) switching power supply applications [1-4]. In controllers of DC-DC converters, the pulse, as the name implies, is a digital signal whose width is normally much smaller than its period (e.g., 50 ns pulse within a 1 μ s cycle). The ramp, on the other hand, is an analog signal with non-zero upper (V_H) and lower (V_L) voltage limits whose absolute amplitude is governed by the stability criteria of the system's negative feedback loop [5] and whose values are determined by the input common-mode range requirements of the loading amplifiers and comparators they drive. The signal frequency ranges from a few kHz to the several MHz that state-of-the-art switching supplies demand [6].

Conventionally to generate ramp signal, after an initial reset event, a capacitor is slowly charged with charge-current I_{Chg} until the capacitor voltage (ramp) reaches upper limit V_H (Figure 1), at which point the comparator trips and quickly resets the ramp to ground with low resistance switch S_{Dchg} , marking the beginning of another cycle [2-8]. However, quickly discharging C to ground via a finite-delay comparator causes the lower limit of the ramp to reset below lower threshold V_L , introducing an error equal to

$$V_{Error} = \frac{dV_{Fall}}{dt} t_{Dly}, \quad (1)$$

where dV_{Fall}/dt is the capacitor's discharge rate and t_{Dly} is comparator CMP2's delay. Even a few nano-seconds of delay causes an error of hundreds of milli-Volts because dV_{Fall}/dt is high. The resulting period is therefore the time required to charge C from the less than predictable low voltage peak to V_H ,

$$T_{\text{Conv}} = \frac{C[V_H - (V_L - V_{\text{Error}})]}{I_{\text{Chg}}}. \quad (2)$$

If a 100 mV peak-to-peak ramp is designed with a 10 V/ μ s discharge rate, for example, a 2 ns delay comparator is required to limit V_{Error} and the extended period to within 20 mV and 20%, respectively.

To decrease the comparator's delay, its quiescent current and consequently power consumption must increase [9]. The exact nature of the delay-power trade-off depends on overdrive and topology and manifests itself as a combination of bandwidth- and slew-rate-limited events, both of which require more current for faster response. Mitigating the adverse effects of this trade-off is intrinsic in portable applications where battery life is many times defined by light load efficiency performance (e.g., idle mode), a good portion of which depends on the ramp generator circuit power consumption [10].

2 SWITCHING REGULATORS

Switching regulators are quickly becoming vital building blocks for an increasing number of electronic applications, including the normally low power, portable sector devices such as cell phones and digital cameras, because of their innate ability to pre-condition widely variable supplies with minimum power losses. Most voltage- and current-mode switching DC-DC converters derive their outputs from averaging pulse-width modulated (PWM) signals with low pass LC filters. The resulting averaged (filtered) PWM signals are the analog outputs of the regulators, whose values are set by duty-cycle. Figure 2(a) illustrates a representative block-level diagram of a typical voltage-mode PWM DC-DC converter, where V_{Out} is the output of the negative shunt-feedback loop and its value is sensed, amplified, and converted into PWM signal V_{ph} before finally being filtered back into a voltage. The peak-to-peak voltage (V_{in}) and duty-cycle D of V_{ph} determine the value of V_{Out} , which

is an averaged version of switching signal V_{ph} . Error amplifier EA modulates D via ramp generator and hysteretic comparator circuits to regulate V_{Out} against reference V_{ref} [5].

The ramp signal sets the duty-cycle by defining the on-time duration of power switch M_H with comparator PWM CMP. The ramp and on-time start at the onset of the constant frequency pulse (Figure 2(b)). The ramp is then compared against the slow-moving output of EA (EA_{out}), and when the ramp surpasses EA_{out} , PWM comparator trips, resets the SR latch, and connects V_{ph} to ground through switch M_L , marking the end of the on-time sequence. Practically, a driver is placed between the output of SR latch and gates of M_H and M_L to prevent the switches from simultaneously conducting current by introducing “dead-time,” without which a short-circuit condition would prevail.

The SR latch ensures only one pair of set-reset events occurs per period. As a result, after a reset, the regulator cannot change state until the onset of the following pulse. The ramp must therefore be linear for the longest worst-case on-time condition, which occurs when duty-cycle D is at its maximum value. Duty-cycle D, however, is normally constrained to less than 90% to protect power switch M_H from overheating and exceeding its power-rating limits. Without this protection, duty-cycle D could viably increase to such an extent that M_H is mostly on and conducting exceedingly large current densities [5]. Consequently, the on-time should never exceed 90% of the period, so slightly less than 10% of the period can be dedicated to reset the ramp (Figure 2(b)), which is the idea behind the proposed scheme. In other words, intrinsic characteristics of the PWM controllers are used to relax the specification of the comparators required in ramp generator circuit, significantly reducing their power consumption and increasing system efficiency at light loads.

3 PROPOSED RAMP

The proposed scheme, shown in Figure 3, charges a capacitor with constant charge current I_{Chg} for 90% of the period, until an upper voltage limit is reached, and discharges it with discharge current I_{Dchg} ($I_{\text{Dchg}} = 9I_{\text{Chg}}$) for the remaining 10%, until the lower limit is surpassed and a new cycle begins. As before, the ramp limits are set with two comparators and the resulting period is

$$T_{\text{Prop}} = C[V_{\text{H}} - (V_{\text{L}} - V_{\text{Error}})] \left(\frac{1}{I_{\text{Chg}}} + \frac{1}{I_{\text{Dchg}}} \right), \quad (3)$$

since the negative ramp is now slew-rate limited, the comparator's delay has a lower impact on V_{Error} .

For example, if a 100 mV peak-to-peak ramp with a 1 V/ μ s discharge rate is designed, a 20 ns-delay comparator is required to limit V_{Error} and the period from varying less than 20 mV and 20%. In other words, a 20 ns-comparator in the proposed circuit (Figure 3) produces the same results that a 2 ns-comparator does with the conventional approach. Replacing the constant discharge current or switch S_{Dchg} with a high-resistance switch performs a similar function, but the uncorrelated process- and temperature-dependence of the resistor introduces uncertainty in the discharge cycle and consequently frequency and the 10% duty-cycle region.

4 CIRCUIT DESIGN

The charge-discharge circuit and a comparator are the building blocks of the proposed ramp generator and their circuit realization are shown in Figure 4. In the proposed charge-discharge circuit of Figure 4(a), bias current I_{b} and mirrors N0,1,2 and P1,2 set the charge- and discharge-current ratios. Switches N4 and P4 reduce transient on-off mirror glitches by preventing transistors N2 and P2 from turning off when they are disconnected from C.

The comparator should toggle when the ramp barely exceeds the upper and lower voltage

limits V_H and V_L , in other words, when input overdrive is at a minimum level. As a result, the design approach of the comparator is to gradually amplify a small overdrive with high bandwidth, low gain amplifiers until enough voltage drive exists to drive CMOS inverters, as shown in Figure 4(b) [11]. The first two stages are low gain, resistor-loaded differential amplifiers, which amplify the overdrive signal enough to drive a higher gain, mirror-loaded differential amplifier. Resistor loads are used instead of PMOS devices because they introduce lower parasitic capacitors to their respective ac nodes, thereby not slowing down the circuit. The higher gain, double to single-ended conversion amplifier then drives a class-A inverter, which, in turn, drives a digital CMOS inverter chain [11].

5 EXPERIMENTAL RESULTS

The proposed ramp generator was designed and fabricated with a 0.5- μm CMOS process (chip photograph shown in Figure 5). An 8-bit counter was added to derive a low frequency clock from the output of the SR latch (S_{Dchg}). The 256 μA ramp generator (charger/discharger and two 32 ns-delay comparators) operates with supply voltages as low as 1.8 V. The high and low ramp limits are 1.4 V and 1.3 V (Figure 6(a)). The circuit was tested and embedded within a current-mode PWM DC-DC converter chip whose results are in Figure 6(b). The ramp in Figure 6(a) was only 320 kHz because the probe capacitance slowed it down. Without the probe, the ramp had a switching frequency of 769 kHz, as proved by the PWM waveforms of Figure 6(b). The 12 mV negative peak error of the probed 320 kHz signal extrapolates to a 28 mV peak error for the 769 kHz ramp, which closely agrees with simulations.

The proposed and conventional ramp generator circuits for switching regulators are compared in Table I. For the same rising ramp-rate and frequency, as required by a PWM DC-DC regulator, the proposed ramp generator requires much slower comparators than conventional schemes (20 ns vs. 2 ns). The cost is limited duty-cycle range ($D \leq 90\%$), but regulators are usually prevented from reaching these limits anyway, to protect the switches from overheating and exceeding power-rating

limits. More importantly, the resulting power savings from relaxing the performance of the comparator is crucial in portable electronics where light-loading power losses limit battery life.

6 CONCLUSIONS

In switching DC-DC regulators, linear ramp signals are only necessary through the duration of the maximum on-time of their respective systems and that is normally limited to within a maximum duty-cycle of 90% to protect the converter from the adverse effects of short-circuit events. Consequently, roughly 10% of the period can be dedicated to controllably discharge the ramp, which is what is proposed in this paper to achieve low-power highly accurate ramp generators for DC-DC converters. In all, the proposed technique relaxes the comparators' propagation delay requirements and therefore decreases their respective power needs, which is critical for switching regulator's circuits used in portable applications since light load efficiency has a significant impact on battery life.

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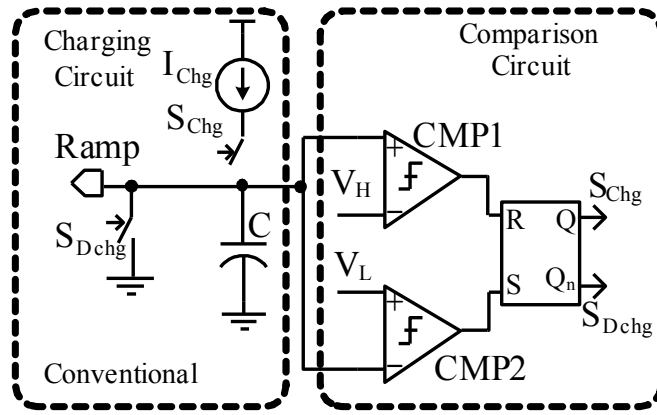


Figure 1. Conventional ramp-generator circuit

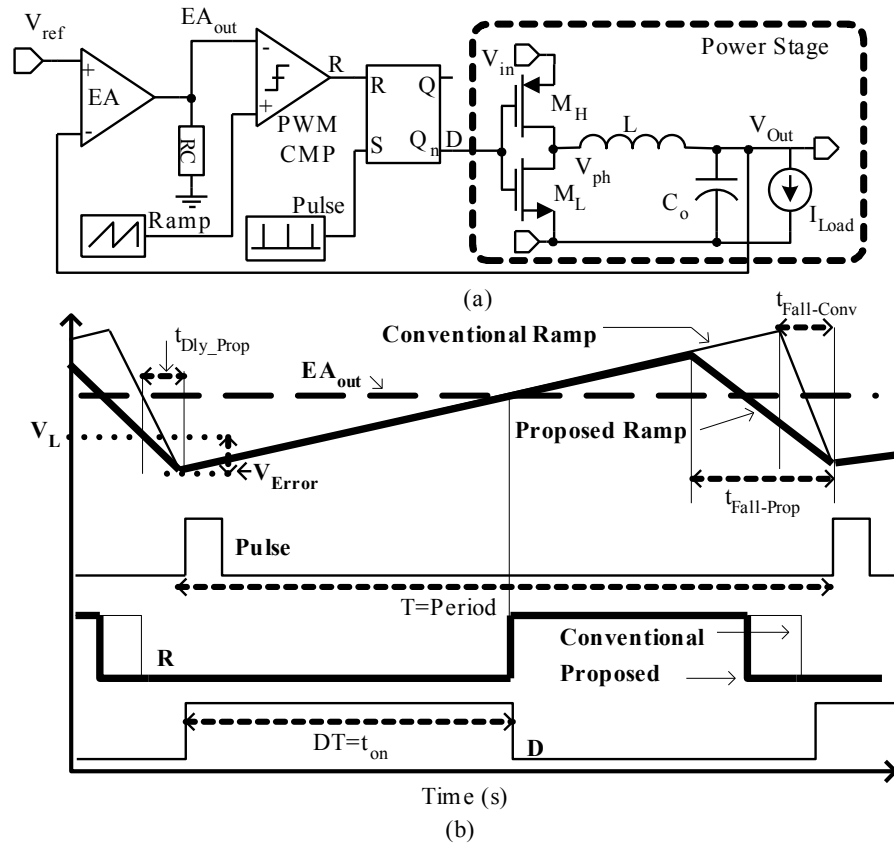


Figure 2. (a) Voltage-mode PWM buck converter and (b) respective signals

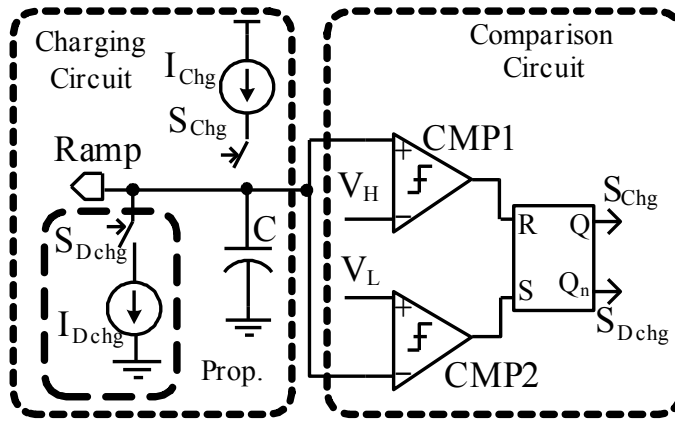


Figure 3. Proposed ramp-generator circuit

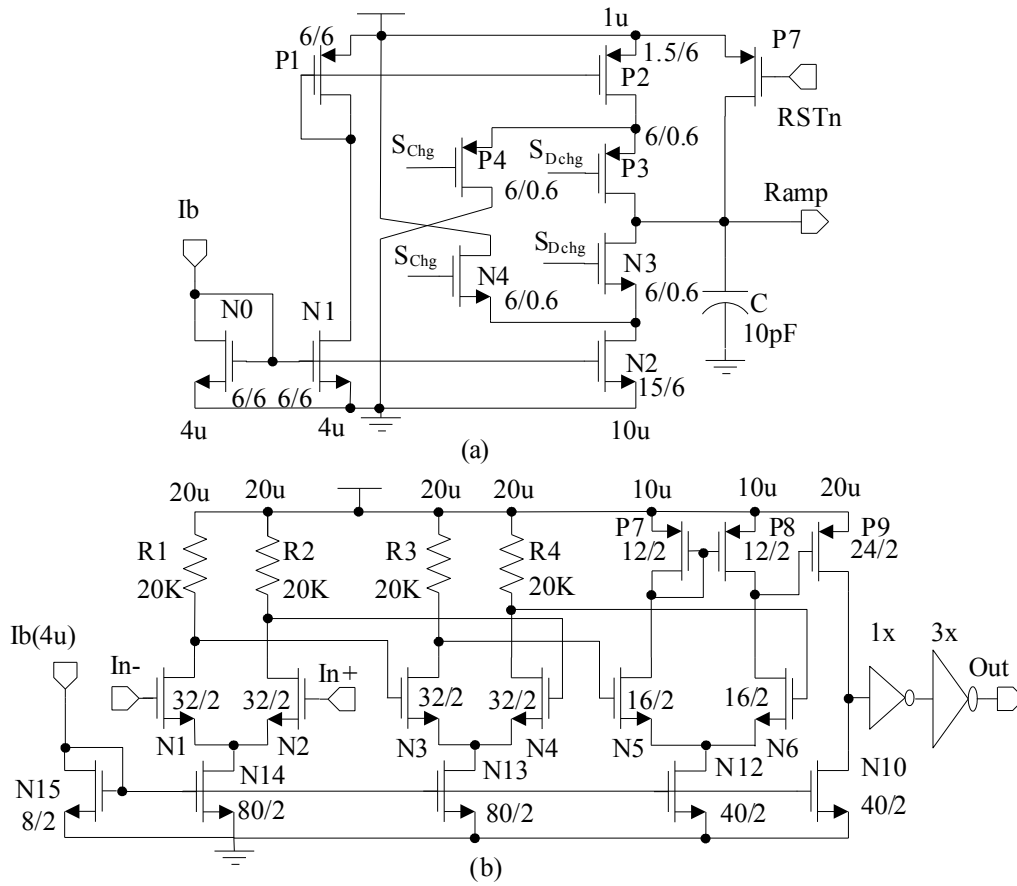


Figure 4. Proposed 0.5-μm CMOS (a) charger/discharger and (b) comparator circuit

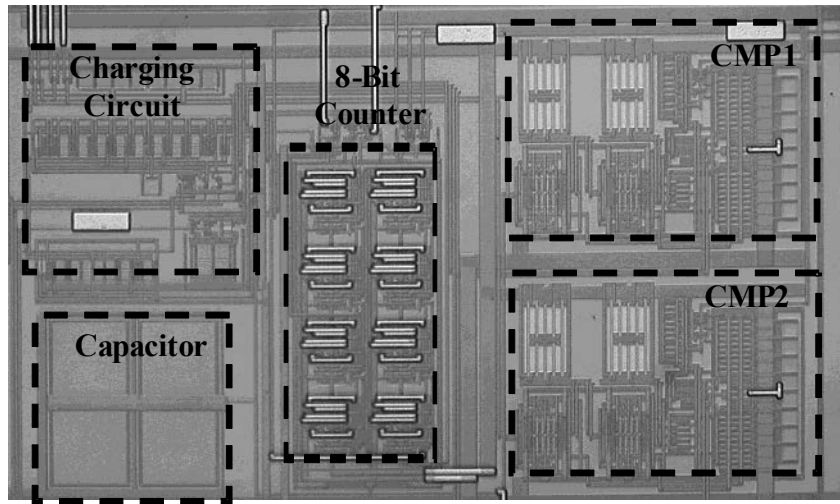
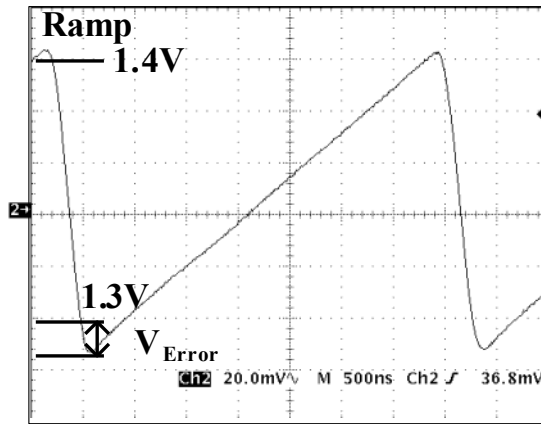
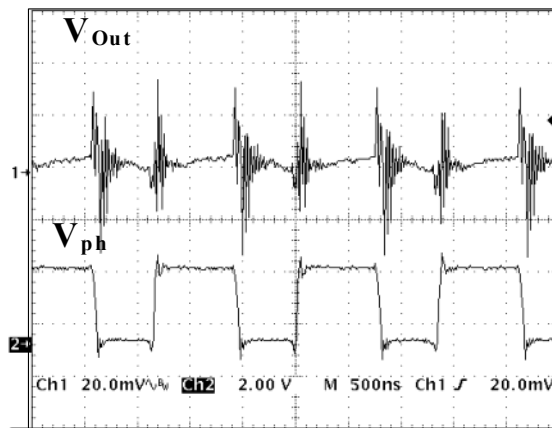


Figure 5. Proposed circuit chip photograph



(a)



(b)

Figure 6. (a) Probed ramp and (b) current-mode DC-DC converter outputs

TABLE I
COMPARISON OF THE PROPOSED AND CONVENTIONAL SCHEMES

Topology Specification	Conventional	Proposed
$\frac{dV_{Rise}}{dt}$	0.1 V/ μ s	0.1V/ μ s
$\frac{dV_{Fall}}{dt}$	10 V/ μ s (Supply dependent)	1 V/ μ s (Supply independent)
Ramp Fall Time t_{Fall}	0.01 μ s	0.1 μ s
Ramp Rise Time t_{Rise}	1 μ s	0.9 μ s
Period T	1.01 μ s	1 μ s
Maximum Converter Duty Cycle	99%	90%
Ramp Amplitude	100 mV	90 mV
Amplitude Accuracy	20 mV	20 mV
Comparator Delay	2 ns	20 ns

BIOGRAPHIES

H. Pooya Forghani-zadeh received his B.S. degree in Electrical Engineering from Sharif University of Technology, Tehran, Iran in 2000 and his M.S. and Ph.D. degrees from Georgia Institute of Technology, Atlanta, Georgia in 2003 and 2006, respectively. He has joined Custom Mixed Signal group of Texas Instruments Incorporated, Dallas, Texas as analog circuit designer since November 2005.

Gabriel A. Rincón-Mora received his B.S.E.E. from Florida International University (High Honors) in 1992 and M.S.E.E. and Ph.D. from Georgia Tech (Outstanding Ph.D. Graduate) in 1994 and 1996, respectively. He worked for Texas instruments defining and designing integrated power management circuit solutions for cellular phones, pagers, laptop and desktop computers, and others from 1994 to 2003 as Senior Integrated Circuits Designer, Design Team Leader, and member of Group Technical Staff and from 2003 to 2005 as Senior Analog Consultant. In 1999, he was appointed Adjunct Professor for Georgia Tech and in 2001 he became a full-time faculty member of its School of Electrical and Computer Engineering. From 2002 to 2004, he was the Director of the Georgia Tech Analog Consortium.

Dr. Rincón-Mora's research is on designing and developing power efficient, high performance, totally integrated, system-on-chip (SoC) and system-in-package (SiP) power management solutions for mobile applications (e.g., energy harvesting, micro-scale fuel cells, thin-film lithium-ion batteries, inductor multipliers, etc.). He received the "National Hispanic in Technology Award" from the Society of Professional Hispanic Engineers, the "Charles E. Perry Visionary Award" from Florida International University, a "Commendation Certificate" from the Lieutenant Governor of California, and "Orgullo Hispano" and "Hispanic Heritage" awards from Robins Air Force Base. He was inducted into the "Council of Outstanding Young Engineering Alumni" by Georgia Tech and featured on the cover of Hispanic Business Magazine as one of "The 100 Most Influential Hispanics," La

Fuente (Dallas Morning News publication), and three times on Nuevo Impacto (Atlanta-based magazine). Dr. Rincón-Mora is a life member of the Society of Hispanic Professional Engineers (SHPE) and a member of IEE.