Limits of Predictive Current-Ripple Suppression in Switching Power-Supply ICs

Lucas A. Milner and Gabriel A. Rincón-Mora, *Member, IET*

lamilner@ece.gatech.edu, rincon-mora@ece.gatech.edu

Georgia Tech Analog, Power, and Energy IC Research

School of Electrical and Computer Engineering

Georgia Institute of Technology

777 Atlantic Drive

Atlanta, GA 30332-0250

Abstract—Large inductance requirements (for accuracy) in switching power supplies for portable applications impede system-on-chip (SoC) integration and therefore form-factor reduction because on-chip inductances are invariably low and off-chip inductors intolerably obtrusive. Canceling the current ripple of innately small on-chip inductors, however, keeps the effective output current ripple and its resulting output voltage variation (i.e., accuracy) within acceptable window limits (e.g., 50-200mA and 20-50mV), effectively multiplying the on-chip inductance and circumventing the need for bulky off-chip inductors. To this end, while gyrators and other voltage-mode inductor multiplier circuitry simulate relatively high inductances, they cannot supply the 250-750mW loads typically attached to battery-powered switching regulators, which the predictive current-mode multipliers discussed in this paper can. The basic objective is to cancel the ac inductor current ripple with an inverting ac replica and allow the on-chip inductor to source the full dc load. AC mismatches in the form of amplitude, delay, and nonlinearity, however, limit the extent to which the original ac ripple is cancelled, constraining the inductor multiplication factor to finite values. The foregoing paper describes, illustrates, and derives the effects of these mismatches on the multiplication factor and shows how realistic non-idealities (e.g., up to 10% gain error and less than 10ns of delay) can yield inductance multiplication factors of 125H/H at 100kHz and 11.5H/H at 10MHz in a practical switching dc-dc power-supply integrated circuit (IC).

1. Inductor Multiplication

Switching dc-dc supplies are bulky, yet essential fixtures in portable and stationary microelectronic applications. The fact is state-of-the-art dc-dc converters used to drive processors, backlights, power amplifiers (PAs), and the like, require

discrete off-chip power inductors. The magnetic-based buck converter shown in Figure 1, for example, converts a 2.7-4.2V Li-Ion voltage (i.e., V_{IN}) into a steady 1.2V supply (i.e., v_O) by modulating how often transistor MP connects switching node v_{SW} to V_{IN}; in other words, because inductor L is a short circuit at dc, the average value of v_{SW} equates to the average value of v_O:

$$v_{O(avg)} \equiv V_O = v_{SW(avg)} = V_{IN} d_{MP} \quad \textbf{(1)}$$

where V_O is the average value of v_O and d_{MP} the duty cycle of MP. The switching action of v_{SW}, however, causes the voltage across the inductor to alternate between V_{IN}-v_O and -v_O and its current i_L to rise and fall as a result. The rippling current (ac component) ultimately flows into output capacitor C_O and produces an ac voltage at the output. This ac ripple voltage, which constitutes accuracy degradation, is inversely proportional to inductance L_O, which is why large off-chip inductors are typically used. Although on-chip inductors with plated ferromagnetic layers are promising [1]-[4], state-of-the-art on-chip inductances are prohibitively low, on the order of 20-100nH, and increasing the number of turns increases the Ohmic losses across its increased equivalent series resistance (ESR) while using cores with higher permeability decreases the onset of saturation conditions. Note MN conducts whenever M_P does not, which means M_N's duty cycle complements d_{MP} and is equal to 1-d_{MP}, or by convention, d_{MP}'.

The "linear-assisted converters" in [5]-[6], "gyrators" in [7]-[8], "active filters" in [9]-[11], and "inductor multipliers" in [12]-[13] attenuate the ac ripple current driven into C_O by subtracting a circuit-derived complementary ripple replica current i_R from on-chip inductor current i_L (Figure 1), the difference of which constitutes a smaller effective ripple current (i.e., $i_{L(eff)}$) that produces less voltage variations in v_O (i.e., across C_O). If i_R were an exact inverting replica of the ac component of i_L, $i_{L(eff)}$ would carry no ac component to drive into C_O and v_O would consequently be free of ripple. Because a larger inductor induces lower ripple currents, the circuit generating i_R is said to be an inductor multiplier, and since an infinitely large inductor produces no ripple, an exact inverting copy yields infinite inductor gain (i.e., infinitely high inductor multiplication factor). Note increasing switching frequency also reduces the ripple current, but additional passives and burst-mode operation are required to implement the resonant topologies that mitigate the increased switching losses, and so reductions in the physical area and voltage ripple are never fully realized. The fact is increasing the switching frequency enough for on-chip inductors to be viable can be impractical in some applications (e.g. when restricted to low-voltage process technology) and might negate the efficiency advantage switching regulators have over their linear counterparts [14]-[15], which are considerably easier and less costly to integrate. Inductor multipliers present their own challenges and also heavily impact

converter efficiency, but an integrated prototype has been developed that demonstrates current-ripple suppression of more than an order of magnitude and also compares favorably with other strategies in terms of efficiency [16].

Given the systematic nature of inductor current i_L—it rises and falls on cue and in proportion to V_{IN} and V_O—both [10] and [13] predict (rather than sense) and reproduce the ac component of i_L via inverting replica i_R. The basic idea is that integrating the voltage across L_O with a capacitor produces an ac triangular voltage that is analogous to i_L so converting this ripple voltage into a current with an inverting transconductor yields i_R. Unfortunately, neither the transconductance nor the capacitance track L_O so i_R is not entirely accurate, plus i_R lags i_L (in time) and finite resistances across the integrating capacitor distort the otherwise triangular voltage. Irrespective of the scheme, however, errors in amplitude, delay, and linearity such as theses change the ultimate amplitude and shape of the current driven into C_O (i.e., $i_{L(eff)}$), limiting the efficacy of the multiplying circuit in switching regulator applications (i.e., the amount by which the effective inductance appears larger). For example, the amplitude of $i_{L(eff)}$ is still almost half of i_L in one experiment with the integrated prototype inductor multiplier [16] shown in Figure 2(a), and as shown in Figure 2(b), its waveform is not triangular. (Although the copper wires added to capture these waveforms with a current probe introduced several nanohenries to the circuit, L_O was 4.7μH so the parasitic effects of the wires were negligible, and considering the wires were only included for the sake of the measurement, their effects do not apply to practical applications, even when using small on-chip inductors.) The ripple suppression in this example is limited because i_R (which is not shown) is only 260mA_{PP} and delayed by 35ns relative to i_L. While literature of multiphase converters, such as [17] and [18], analyze the cancellation effect of complementary current ripples with respect to amplitude errors, delay and nonlinearity effects due to finite time constants, either of which can dominate the cancellation factor and both of which are inherent in any active-circuit technique, remain largely unexplored. This paper describes, illustrates, and derives the individual (Section 2) and combined (Section 3) effects of non-idealities such as these on a switching power supply circuit (Section 4), drawing and discussing relevant conclusions (Section 5).

Note 1: Since analyzing these errors by comparing the ac portions of i_R to i_L only (and ignoring their dc components) is easier, to help delineate one from the other, the following sections use all lowercase variables (e.g., i_r and i_l) for ac signals only, all uppercase variables (e.g., I_R and I_L) for dc, and lowercase-uppercase combinations (e.g., i_R and i_L) for both ac and dc. Notice, nevertheless, that removing the dc component does not affect the peak-to-peak magnitude of a signal, which means, for example, $\Delta i_{l(eff)}$ equals (by definition) $\Delta i_{L(eff)}$, even if $i_{l(eff)}$ differs from $i_{L(eff)}$ by a dc value.

Note 2: A ripple in v_O constitutes a ripple voltage across L_O, which causes variations in i_L. The extent to which the ripple in v_O affects i_L's large-signal response depends on its percent variation, which in the case of state-of-the-art dc-dc converters is

on the order of 5-10mV/V, in other words, at most 1% of V_{OUT}. In deriving i_L, as a result, assuming v_O reduces to its dc value of V_O produces errors well below 1%. Neglecting this error in the foregoing analysis is therefore reasonable (and practical) because other errors, as results will show, swamp its effects, ultimately yielding sufficiently accurate and insightful expressions from which to draw meaningful design-oriented conclusions. Incidentally, lower ripples, which result from higher multiplication factors, reduce the impact of this error. Nevertheless, for validation and accuracy, all simulation results in this paper include this error (i.e., the effects of a ripple in v_O) so the graphs and tables shown are accurate, proving the validity of this assumption.

2. Individual Errors

A. Linear (Amplitude) Error

The first error to consider is a variation in amplitude, when the peak-to-peak value of inverting replica current i_R differs from that of the ac component in inductor current i_L (i.e., i_l), as depicted in Figure 3. This error has been acknowledged before in the context of multiphase converters [17], in which the ripple currents through two or more inductors are meant to cancel each other. With a linear error of this sort, the effective ripple current driven into C_O (i.e., $i_{l(eff)}$), which is the sum of i_l and i_R, retains a triangular shape but with smaller amplitude:

$$\Delta i_{L(eff)} = \Delta i_L + \Delta i_R = \Delta i_L - \Delta i_L\left(1 - K_A\right) = K_A \Delta i_L, \tag{2}$$

where K_A is the fractional amplitude-error coefficient, which can be positive or negative. Because the ultimate metric in a switching power supply is its peak-to-peak output ripple voltage, the inductor multiplication factor amounts to the peak-to-peak ratio of Δi_L to $\Delta i_{L(eff)}$, which in this case is the reciprocal of K_A:

$$M_{LA} \equiv \frac{L_{Eff}}{L_O} \equiv \frac{\Delta i_L}{\Delta i_{L(eff)}} = \frac{1}{K_A}, \tag{3}$$

or equivalently, by definition, the ratio of equivalent inductance L_{Eff} that would have produced $i_{L(eff)}$ and on-chip inductance L_O, where M_{LA} is the multiplication factor when only an error in amplitude exists.

B. Delay (Timing) Error

A delay error in inverting replica current i_R with respect to i_L is more problematic because its effect on effective output current $\Delta i_{L(eff)}$ is to substantially increase its ac ripple, especially under high di_L/dt conditions, when the voltage across the inductor is relatively large, and with increasing switching frequencies, as delay t_d becomes a larger fraction of switching period T_{SW}. Figure 4 illustrates a replica current i_R that, other than being delayed by t_d, is perfectly matched to the ac portion of i_L. The effect of the delay on $i_{L(eff)}$ when i_L and $-i_R$ both rise (or fall) is a constant difference $\Delta i_{L(eff).R}$ (or $\Delta i_{L(eff).F}$). During the

times i_L rises and $-i_R$ falls, and *vice versa*, $i_{L(eff)}$ rises and falls linearly to and from peak values $\Delta i_{L(eff).R}$ and $-\Delta i_{L(eff).F}$, the net result of which is a trapezoidal ac current into output capacitor C_O, as shown in Figure 4. The trapezoidal shape is an unfortunate result in so far as it complicates control of a switching regulator. Since this shape is a result of delay, which cannot be completely eliminated in any active filter, it will always be a feature of $i_{L(eff)}$ that may in some cases dominate other errors, so it must be characterized.

Rising difference $\Delta i_{L(eff).R}$ is the product of rising rate di_L^+/dt and delay t_d, which is inversely proportional to L_O and directly proportional to the voltage across L_O when switch M_P conducts, that is, V_{IN} - v_O, or equivalently, $V_{IN}(1 - d_{MP})$ or $V_{IN}d_{MP}'$:

$$\Delta i_{L(eff).R} = \left(\frac{di_L^+}{dt}\right)t_d = \left(\frac{V_{IN} - v_O}{L_O}\right)t_d = \left[\frac{V_{IN}\left(1\text{-}d_{MP}\right)}{L_O}\right]t_d = \left(\frac{V_{IN}d_{MP}'}{L_O}\right)t_d. \quad \textbf{(4)}$$

Similarly, falling difference $\Delta i_{L(eff).F}$ is the product of di_L^-/dt and t_d and inversely proportional to L_O and directly proportional to v_O, or $V_{IN}d_{MP}$:

$$\Delta i_{L(eff).F} = \left(\frac{di_L^-}{dt}\right)t_d = \left(\frac{v_O}{L_O}\right)t_d = \left(\frac{V_{IN}d_{MP}}{L_O}\right)t_d. \quad \textbf{(5)}$$

The total ac peak-to-peak current in $i_{L(eff)}$ is the sum of the aforementioned rising and falling difference currents (i.e., $\Delta i_{L(eff)} = \Delta i_{L(eff).R} + \Delta i_{L(eff).F}$) whereas the peak-to-peak current in i_L (i.e., Δi_L) is the product of rising rate di_L^+/dt and M_P's on time, the latter of which is the product of switching period T_{SW} and d_{MP} (i.e., t_{on}/T_{SW}):

$$\Delta i_L = \left(\frac{di_L^+}{dt}\right)d_{MP}T_{SW} = \left(\frac{V_{IN}\text{-}v_O}{L_O}\right)\frac{d_{MP}}{f_{SW}} = \left[\frac{V_{IN}\left(1\text{-}d_{MP}\right)}{L_O}\right]\frac{d_{MP}}{f_{SW}} = \frac{V_{IN}d_{MP}'d_{MP}}{L_O f_{SW}}, \quad \textbf{(6)}$$

where f_{SW} is switching frequency $1/T_{SW}$. As before, within the context of switching power supplies, the effective inductor multiplication factor is the ratio of $\Delta i_{L(eff)}$ and Δi_L, which in the presence of a delay yields a factor that is directly proportional to $d_{MP}d_{MP}'$ and inversely proportional to t_d and f_{SW}, or inversely proportional to the percentage of time t_d is with respect to T_{SW}:

$$M_{I.D} \equiv \frac{L_{Eff}}{L_O} \equiv \frac{\Delta i_L}{\Delta i_{L(eff)}} = \frac{\Delta i_L}{\Delta i_{L(eff).R} + \Delta i_{L(eff).F}} = \frac{d_{MP}d_{MP}'}{t_d f_{SW}} = d_{MP}d_{MP}'\left(\frac{T_{SW}}{t_d}\right), \quad \textbf{(7)}$$

where $M_{I.D}$ is the effective inductor multiplication factor in the presence of a delay. Note that, unlike an amplitude mismatch, a delay error changes the shape of $\Delta i_{L(eff)}$ to trapezoidal and its impact is worse under higher switching frequencies.

C. Nonlinear Error

Nonlinearities in replica current i_R constitute another error source (as amplitude and delay errors are linear effects). These nonlinear errors result from non-idealities in the circuit, such as the exponential response of RC poles in the signal path. For instance, driving and sinking a constant square current into and from a capacitor produces a triangular voltage, which when multiplied by a transconductor, generates the triangular current desired in i_R. However, considering current levels are low to decrease quiescent power losses and therefore extend battery life, the presence of a parasitic resistance across the aforementioned filter capacitor, as shown in Figure 5(a), distorts the otherwise linear response with higher order components (i.e., the exponential RC time-constant response produces nonlinearities in i_R). Note the equivalent series resistance ($R_{ESR.L}$) of L_O in the power stage of a switching supply (Figure 5(b)) also produces similar effects in i_L, except L_O and $R_{ESR.L}$ are typically large and small enough, respectively, to produce unobservable nonlinear effects in i_L.

A second-order polynomial with respect to time approximates the effects of the exponential relationship in i_R and i_L reasonably well while simultaneously simplifying the math. The fact is the coefficient of the second-order term of an exponential is considerably larger than those of higher order components, as seen from its Taylor-series expansion:

$$\mathrm{e}^{At} = \mathrm{e}^{At}\Big|_{t=0} + \left(\frac{1}{1!}\right)\frac{d^1\left(\mathrm{e}^{At}\right)}{dt^1}\Bigg|_{t=0} t + \ldots + \left(\frac{1}{n!}\right)\frac{d^n\left(\mathrm{e}^{At}\right)}{dt^n}\Bigg|_{t=0} t^N = 1 + At + \left(\frac{A^2}{2}\right)t^2 + \left(\frac{A^3}{6}\right)t^3 + \ldots + \left(\frac{A^n}{n!}\right)t^n, \quad \textbf{(8)}$$

where second-order coefficient $A^2/2$ is greater than the third and all others. (Amplitude and delay errors already account for errors in linear term At.) Figure 6 shows how this simplifying assumption preserves the general characteristics of the nonlinearity shown in Figure 5. Adding the second-order term, however, also affects the amplitude of the signal, which was already addressed in the analysis of fractional amplitude-error coefficient K_A. As a result, scaling factor K is used to normalize the otherwise amplitude-affected replica current i_R' (shown as its inverse $-i_R'$ in Figure 6 to appreciate how it relates to i_L) into $-i_R$ to decouple nonlinear effects from amplitude and delay errors.

To understand the impact of nonlinearity on $i_{l(eff)}$, it is helpful to first recall that the rising and falling inductor current is a function of the rising and falling rates of i_L when subjecting L_O to on- and off-time voltages of $V_{IN} - v_O$ and $-v_O$, respectively, as M_P switches on and off:

$$i_{l.R} = \left(\frac{di_L^+}{dt}\right)t = \left(\frac{V_{IN} - v_O}{L_O}\right)t = \left(\frac{V_{IN}\, d_{MP}'}{L_O}\right)t \equiv m_R t \quad \textbf{(9)}$$

and

$$i_{l.F} = \left(\frac{di_L^-}{dt}\right)t = \left(\frac{-v_O}{L_O}\right)t = \left(\frac{-V_{IN}\, d_{MP}}{L_O}\right)t = \left(\frac{-m_R\, d_{MP}}{d_{MP}'}\right)t \equiv -m_F t, \quad \textbf{(10)}$$

where the effects of parasitic resistor $R_{ESR.L}$ are negligible and m_R and m_F are the linear rising and falling coefficients of i_l. Inverting replica current $-i_R$ must therefore include scaling factor K and the aforementioned linear rising and falling coefficients to retain the amplitude and first-order term of i_L while succumbing to the effects of rising and falling nonlinear terms α_R and α_F:

$$-i_{R.R} = K\left(m_R t - \alpha_R t^2\right) \tag{11}$$

and

$$-i_{R.F} = K\left(-m_F t + \alpha_F t^2\right), \tag{12}$$

where K, by definition, is the constant that equates the amplitudes of i_l and $-i_R$ (i.e., $i_{l.R}$ and $-i_{R.R}$ at time t_{on} and $i_{l.F}$ and $-i_{R.F}$ at t_{off}):

$$i_{l.R}\big|_{t_{on}} = m_R t_{on} \equiv -i_{R.R}\big|_{t_{on}} = K\left(m_R t_{on} - \alpha_R t_{on}{}^2\right) \tag{13}$$

or

$$K = \frac{m_R}{m_R - \alpha_R t_{on}}, \tag{14}$$

which, for the purpose of this discussion, is a constant. The sign of nonlinear terms α_R and α_F is consistent with exponential distortion in i_R (Figure 6).

As before, the effective inductor multiplication factor, as it relates to switching converters, is the ratio of the peak-to-peak values of i_L and $i_{L(eff)}$. Effective output ripple ac current $i_{l(eff)}$ is the sum of i_l and i_R (or the difference between i_l and $-i_R$) so rising and falling $i_{l(eff)}$ with a nonlinear error amount to

$$i_{l(eff).R} = i_{l.R} + i_{R.R} = m_R t - K\left(m_R t - \alpha_R t^2\right) = m_R\left(1-K\right)t + K\alpha_R t^2 \tag{15}$$

and

$$i_{l(eff).F} = i_{l.F} + i_{R.F} = -m_F t - K\left(-m_F t + \alpha_F t^2\right) = -m_F\left(1-K\right)t - K\alpha_F t^2. \tag{16}$$

The polarity of the second-order (i.e., squared) term indicates $i_{l(eff)}$ is concave and larger than $i_{l.R}$ during M_P's on time (i.e., rising portion of i_L) and convex and smaller than $i_{l.F}$ during M_P's off time (i.e., falling part of i_L), as seen in Figure 6. Unlike the amplitude and delay errors, however, the maximum error (i.e., $\Delta i_{L(eff)}$) does not occur at transitional points t_{on} or t_{off}. Differentiating $i_{l(eff).R}$ and $i_{l(eff).F}$ and equating to zero reveals the maximum error occurs half way through t_{on} and t_{off}:

$$\left.\frac{di_{l(eff).R}}{dt}\right|_{t=0.5t_{on}} = 0 \tag{17}$$

and

$$\left.\frac{di_{l(eff).F}}{dt}\right|_{t=0.5t_{off}} = 0, \tag{18}$$

which means the amplitude of $i_{l(eff)}$ is

$$\Delta i_{L(eff)} \equiv \Delta i_{L(eff).R} + \Delta i_{L(eff).F} = -i_{l(eff).R}\Big|_{0.5t_{on}} + i_{l(eff).F}\Big|_{0.5t_{off}}$$

$$= -m_R\left(1-K\right)\left(\frac{t_{on}}{2}\right) - K\alpha_R\left(\frac{t_{on}}{2}\right)^2 - m_F\left(1-K\right)\left(\frac{t_{off}}{2}\right) - K\alpha_F\left(\frac{t_{off}}{2}\right)^2. \quad \textbf{(19)}$$

Similar to how d_{MP}/d_{MP}' relates m_R and m_F (i.e., m_F is $m_R d_{MP}/d_{MP}'$), t_{on} and t_{off} correlate (with respect to switching period T_{SW}):

$$t_{on} = d_{MP}T_{SW} = d_{MP}T_{SW}\left(\frac{d_{MP}'}{d_{MP}'}\right) = d_{MP}'T_{SW}\left(\frac{d_{MP}}{d_{MP}'}\right) = t_{off}\left(\frac{d_{MP}}{d_{MP}'}\right). \quad \textbf{(20)}$$

Additionally, for equilibrium and steady-state conditions, the ripple must rise as much as it falls every period, which means $i_{R.R}$ at t_{on} must equate to $-i_{R.F}$ at t_{off} and second-order coefficients α_R and α_F consequently also relate through the ratio of d_{MP}' and d_{MP}:

$$i_{R.R}\Big|_{t_{on}} = K\left(m_R t_{on} - \alpha_R t_{on}^2\right) \equiv -i_{R.F}\Big|_{t_{off}} = -K\left(-m_F t_{off} + \alpha_F t_{off}^2\right) = K\left(m_R\left(\frac{d_{MP}}{d_{MP}'}\right)t_{on}\left(\frac{d_{MP}'}{d_{MP}}\right) - \alpha_F t_{on}^2\left(\frac{d_{MP}'}{d_{MP}}\right)^2\right) \quad \textbf{(21)}$$

or

$$\alpha_R = \alpha_F\left(\frac{d_{MP}'}{d_{MP}}\right)^2, \quad \textbf{(22)}$$

where $m_R d_{MP}/d_{MP}'$ and $t_{on}d_{MP}'/d_{MP}$ replace m_F and t_{off}, respectively. Using these simplifying relations reduces $\Delta i_{L(eff)}$ to

$$\Delta i_{L(eff)} = -2K\alpha_R\left(\frac{t_{on}}{2}\right)^2 - 2m_R\left(1-K\right)\left(\frac{t_{on}}{2}\right) = 2\left|i_{l(eff).R}\Big|_{0.5t_{on}}\right| = 2\left|i_{l(eff).F}\Big|_{0.5t_{off}}\right|, \quad \textbf{(23)}$$

which means the worst-case variation during a rising i_l event equals that of its falling counterpart. Recalling Δi_L is the product of rising rate m_R and t_{on} and the current-based inductor multiplication factor is the ratio of Δi_L and $\Delta i_{L(eff)}$:

$$M_{I.N} \equiv \frac{L_{Eff}}{L_O} \equiv \frac{\Delta i_L}{\Delta i_{L(eff)}} = \frac{m_R t_{on}}{-2K\alpha_R\left(\frac{t_{on}}{2}\right)^2 - 2m_R\left(1-K\right)\left(\frac{t_{on}}{2}\right)} = \frac{m_R}{-K\left(0.5\alpha_R t_{on} - m_R\right) - m_R} = 2\left(\frac{m_R}{\alpha_R t_{on}} - 1\right), \quad \textbf{(24)}$$

where $M_{I.N}$ is the multiplication factor in the presence of nonlinear error α, reveals that the decreasing effect of a nonlinearity in i_R on $M_{I.N}$ is more pronounced with slower rise and fall times because the mid on- and off-time (i.e., worst-case) differences between a linear and an exponential (or second-order) response is worse (i.e., greater) as more time elapses (i.e., slower di_L/dt rates). Given the true nature of nonlinearity effects in RC circuits, it is useful to consider the time constant that produced α in the first place with respect to switching period T_{SW}, in other words, $R_T C_T$ or $L_O/R_{ESR.L}$ time-constant τ_α. In this sense, α is inversely proportional to τ_α (i.e., a small α value corresponds to a large τ_α), which means an infinitely large τ_α

produces no discernable nonlinear effects in i_R within finite switching period T_{SW} (i.e., the multiplier circuit integrates its square input current perfectly and therefore produces a nearly flawless triangular current) and yields a substantially high inductor multiplication factor.

3. Combined Effects

Although replica current i_R contains amplitude, delay, and nonlinearity errors, one of these often dominates and determines the nature of the resulting response. The inductor multiplier, by design, should balance and trade-off the dominant error for another to minimize the total variation in effective output inductor current $i_{L(eff)}$, producing in the process a combined effect. In the case where amplitude (i.e., K_A) and delay (i.e., t_d) errors overwhelm nonlinearity (i.e., τ_α), the ac component of $i_{L(eff)}$ mostly conforms to the triangular and trapezoidal shapes K_A and t_d induce on $i_{l(eff)}$, as illustrated in Figure 7(a), yielding a worst-case peak-to-peak ripple at M_P's switching transitions t_{on} and t_{off}. On the other hand, as shown in Figure 7(b), in the event τ_α effects dominate over those of K_A and t_d, the peak ripple occurs closer to half way through M_P's on and off conduction times (i.e., at $0.5t_{on}$ and $0.5t_{off}$).

In the first case, when amplitude and delay errors dominate (Figure 7 (a)), the total peak-peak error can be divided into two parts: the portion impacted by all K_A, t_d, and τ_α and the one only due to K_A. The sums of the two parts at the end of the on time and at the end of the off time are, respectively:

$$\Delta i_{L(eff).R} = \Delta i_{K_A} + \Delta i_{K_A,t_d,\tau_\alpha} = \left(\frac{K_A}{2}\right)\Delta i_L + K(1-K_A)\left(m_R t - \alpha_R t^2\right)\Big|_{t_{on}-t_d}^{t_{on}}$$

$$= \frac{K_A}{2}\left(\Delta i_L\right) + K(1-K_A)\left(m_R t_d + \alpha_R t_{on}^2 - 2\alpha_R t_{on} t_d\right). \quad \textbf{(25)}$$

and

$$\Delta i_{L(eff).F} = \Delta i_{K_A} + \Delta i_{K_A,t_d,\tau_\alpha} = \left(\frac{K_A}{2}\right)\Delta i_L + K(1-K_A)\left(m_F t - \alpha_F t^2\right)\Big|_{t_{off}-t_d}^{t_{off}}$$

$$= \left(\frac{K_A}{2}\right)\Delta i_L + K(1-K_A)\left(m_F t_d + \alpha_F t_{off}^2 - 2\alpha_F t_{off} t_d\right)$$

$$= \left(\frac{K_A}{2}\right)\Delta i_L + K(1-K_A)\left(m_R\left(\frac{d_{MP}}{d_{MP}'}\right)t_d + \alpha_R t_{on}^2 - 2\alpha_R t_{on}\left(\frac{d_{MP}}{d_{MP}'}\right)t_d\right). \quad \textbf{(26)}$$

Therefore, the combination of K_A, t_d, and τ_α, when dominated by K_A and t_d, yields effective ripple current $\Delta i_{L(eff)}$

$$\Delta i_{L(eff)} = \Delta i_{L(eff).R} + \Delta i_{L(eff).F} = K_A\left(\Delta i_L\right) + K(1-K_A)\left(\frac{m_R t_d}{d_{MP}'} + 2\alpha_R t_{on}^2 - \frac{\alpha_R t_{on} t_d}{d_{MP}'}\right). \quad \textbf{(27)}$$

The multiplication factor, again defined in terms of current, is a ratio with Δi_L in the numerator and the above expression in the denominator. In the case where α is substantially small (or τ_α practically infinite and scaling factor K nearly one), the multiplication factor simplifies to

$$M_{I.A.D.N}\big|_{\alpha\to 0, K\to 1} \equiv \frac{\Delta i_L}{\Delta i_{L(eff)}} = \frac{d_{MP} d_{MP}' T_{SW}}{t_d(1-K_A) + d_{MP} d_{MP}' T_{SW} K_A}. \quad \textbf{(28)}$$

The likelihood τ_α effects dominate over those of K_A and t_d (Figure 7 (b)), however, is low because the degree of non-linearity required to overwhelm amplitude error and delay errors (given practical K_A and t_d values of 5-10% and 50-100ns) is unrealistically high (e.g., τ_α must be below 5-20% of T_{SW}). Even if nonlinearity is introduced intentionally, there is no reason to make it dominant.

From a design perspective, it helps to reduce the combined effects of all errors (i.e., $M_{I.A.D.N}$) into a compact, easy-to-discern format. Intuitively, and as shown, a dominant error prevails over the others (i.e., $M_{I.A.D.N}$ is approximately the worse of $M_{I.A}$, $M_{I.D}$, and $M_{I.N}$), and the impact of non-dominant errors is to reduce $M_{I.A.D.N}$ slightly. Interestingly, resistors in parallel behave in a similar fashion, that is, higher resistances (e.g., R_{HI}) pull the combined resistance (e.g., R_{TOT}) below the lowest resistance in the network (e.g., R_{LOW}), where the combined resistance is closest to the lowest (e.g., $R_{TOT} \approx R_{LOW}$) when the lowest is substantially lower than the rest (e.g., $R_{LOW} < 0.1R_{HI}$). As such, $M_{I.A.D.N}$ may be empirically expressed as the (resistive) parallel combination of its constituent factors, where the lowest individual factor dominates $M_{I.A.D.N}$ and other factors have a tendency to decrease $M_{I.A.D.N}$ below the lowest factor:

$$M_{I.A.D.N} \approx M_{I.A} \| M_{I.D} \| M_{I.N} = \frac{M_{I.A} M_{I.D} M_{I.N}}{M_{I.A} M_{I.D} + M_{I.D} M_{I.N} + M_{I.N} M_{I.A}}. \quad \textbf{(29)}$$

Note, for example, that when nonlinearity is negligible (i.e., $M_{I.N}$ is infinitely high), Eqn. (29) reduces to

$$M_{I.A.D.N}\big|_{M_{I.N}\to\infty} \approx \frac{M_{I.D} M_{I.A}}{M_{I.A} + M_{I.A}} = \frac{d_{MP} d_{MP}' T_{SW}}{t_d + d_{MP} d_{MP}' T_{SW} K_A}, \quad \textbf{(30)}$$

which is almost identical to Eqn. (28). To further qualify the foregoing approximation, consider the practical case where delay and amplitude errors dominate, such as when t_d is 20ns, K_A is 0.05, α_R is 0.001A/μs^2, d_{MP} is 0.3, T_{SW} is 500ns, V_{IN} is 3V, and L_O is 0.5μH. $M_{I.A.D.N}$ in this scenario is 10.21 (from simulation results) and the simplified expression of Eqn. 29 predicts 10.17, which represents a 0.4% error. If on the other hand, error dominance is less prevalent (i.e., all three errors have similar impact), such as in the case where t_d is 10ns, K_A is 0.1, α_R is 0.01A/μs^2, d_{MP} is 0.5, T_{SW} is 1μs, V_{IN} is 4V, and L_O is 1μH, $M_{I.A.D.N}$ is 4.58 and Eqn. 29 predicts 5.19, a value that is 13% off its target. Simulation results of several cases, in fact, show the error is usually within 10% and less often up to 20%. The accuracy ultimately improves when one factor is considerably

larger (i.e., its corresponding error is negligible) or smaller (i.e., its corresponding error is dominant) than the others, which is more likely to occur in a practical application.

4. Realistic Inductor Multipliers in Switching Regulators

Thus far, inductor multiplication factor M_I has been defined as the ratio of inductor ripple current Δi_L to effective ripple current $\Delta i_{L(eff)}$. However, because the overriding objective of a switching regulator (Figure 1) is to suppress variations in output voltage v_O, and increasing (or multiplying) L_O is only a means to reducing steady-state voltage ripple Δv_O, a current-based definition is not always as meaningful as a voltage-based one. The fact is output capacitor C_O integrates $\Delta i_{L(eff)}$ and the shape and frequency content of $\Delta i_{L(eff)}$ (not just the amplitude) determine Δv_O. For example, while the same $\Delta i_{L(eff)}$ ripple could result from gain error (as shown with triangular $\Delta i_{L(eff)}$ in Figure 8(a)) or delay (as with trapezoidal $\Delta i_{L(eff)}$ in Figure 8(b)) alone or a combination of both, the same peak-to-peak output ripple voltage (i.e., Δv_O) does not necessarily result. Therefore, the efficacy of the multiplier (i.e., the amount by which the effective inductance appears larger) should also be characterized by the ratio of Δv_O with and without the benefit of i_R (as denoted by M_V), If the voltage across $R_{ESR.C}$ (i.e., Δv_{ESR}) overwhelms that of C_O (i.e., Δv_C), however, output ripple voltage Δv_O is only a linear translation of $i_{l(eff)}$ (i.e., $\Delta v_O = \Delta v_C + \Delta v_{ESR} \approx \Delta v_{ESR} = R_{ESR.C} i_{l(eff)}$), which means current-based multiplication factor M_I, when applied to high-ESR capacitors, is equivalent to its voltage-based counterpart, that is, M_I equals M_V. In general, M_I does not account for the shape of $i_{L(eff)}$, and M_V accounts for it in the manner most relevant to switching regulators: output ripple voltage accuracy.

Voltage-based inductor multiplication factor M_V for low-ESR output capacitors is the ratio of Δi_L to $\Delta i_{L(eff)}$, but integrated by C_O. Deriving the output voltage ripple effects of i_L alone without the multiplier amounts to integrating half the ac inductor current ripple into C_O from time t_a to t_b (i.e., half period T_{SW}) in Figure 8(a), which is the area under the specified triangle:

$$\Delta v_{O.L} = \frac{\Delta Q}{C_O} = \frac{1}{C_O}\left(\int_{t_a}^{t_b} i_l\,dt\right) = \frac{(0.5\Delta I_L)(0.5T_{SW})}{2C_O} = \frac{V_{IN}\,d_{MP}\,d_{MP}'\,T_{SW}^2}{8L_O C_O}, \tag{31}$$

where $\Delta v_{O.L}$ is the output ripple without the multiplier and t_a and t_b mark the points when ac current i_l crosses zero, which coincide with the points when ac current $i_{l(eff)}$ crosses zero, but only if amplitude is the dominant error (Figure 8(a)). In general, the boundaries for the integral of $i_{l(eff)}$ are not straightforward because the different combinations of errors affect the shape of the waveform drastically. However, in a simple case, such as when delay is the only error, integrating $i_{l(eff)}$ into C_O from t_c to t_d in Figure 8(b) yields multiplied output ripple $\Delta v_{O.L(eff)}$, which is proportional to the area of the highlighted trapezoid (i.e. the average of the parallel sides times the distance between them):

$$\Delta v_{O.L(eff)} = \frac{1}{C_O}\left(\int_{t_c}^{t_d} i_{L(eff)}\,dt\right) = \frac{1}{C_O}\left[\frac{(A+B)}{2}C\right] = \frac{1}{C_O}(A-\Delta t)C$$

$$= \frac{1}{C_O}\left[A - \frac{C}{\left(\frac{di_{L(eff)}}{dt}\right)}\right]C = \left(\frac{d_{MP}'d_{MP}T_{SW} - d_{MP}t_d}{C_O}\right)\left(\frac{d_{MP}V_{IN}t_d}{L_O}\right), \quad \textbf{(32)}$$

where A, B, C, and Δt are the current levels and time intervals labeled in Figure 8(b). Voltage-based inductor multiplication factor M_V for the simplified case of t_d therefore becomes

$$M_{V.D} \equiv \frac{\Delta v_{O.L}}{\Delta v_{O.L(eff)}} = \frac{1}{8}\left[\frac{d_{MP}'}{d_{MP}'\left(\frac{t_d}{T_{SW}}\right) - d_{MP}\left(\frac{t_d}{T_{SW}}\right)^2}\right] \approx \frac{1}{8}\left(\frac{T_{SW}}{t_d}\right), \quad \textbf{(33)}$$

which means $M_{V.D}$ is less sensitive to d_{MP} (and d_{MP}') than $M_{I.D}$ in the presence of delay errors only. In fact, for a gain of 10H/H in terms of $M_{V.D}$, t_d can be no more than 1.25% of T_{SW} (e.g., less than 12.5ns for a 1MHz converter and less than 1.25ns for a 10MHz converter), unless duty cycles are at their extremes (e.g., 1% or 99%). In feedback schemes, where i_L is sensed and then replicated, sensing and applying i_R to v_O in less than 1.25-12.5ns is considerably difficult under low-quiescent current conditions. Although feed-forward techniques [13] partially decrease this delay by deriving Δi_L information from further back in the ac path, matching and tracking delays down to 1.25-12.5ns remains a substantial challenge.

Simplifying the case to only delay errors, however, does not account for the possible canceling effects of gain error and nonlinearity. Nonlinearity errors, in fact, accelerate the rising rate of $-i_R$ (Figure 6) and therefore offset the effects of delay errors. Figure 9 illustrates an optimal case where time constant τ_α is sufficiently small to offset t_d and allow $-i_R$ to lead i_L for part of the period, even when t_d is 10% of T_{SW}. Even though the impact on $\Delta i_{L(eff)}$ is not as significant, $\Delta i_{L(eff)}$ now crosses zero more often, as i_R shifts from leading to lagging i_l, which means Δv_O rises and falls more frequently and charges and discharges C_O less (i.e., Δv_O is smaller). (Figure 9 also shows how v_O, without the benefit of i_R, exceeds its counterpart substantially because the unabated inductor current ripple Δi_L now charges and discharges C_O.) For comparison, M_V is 1.25H/H when t_d is 10% of T_{SW} and other errors are negligibly small and 11.5H/H when t_d is 10%, K_A is 10%, and τ_α is 22% of T_{SW}, and for the simulation below T_{SW} is 10MHz.

In practice, delay t_d and gain K_A errors are unavoidable, and offsetting their effects with nonlinearity τ_α is better but not perfect. With respect to t_d, the effects on inductor multiplication factor M_V are worse at high frequencies, when a small delay

of 10ns constitutes 10% of a 100ns period T_{SW}, which barring K_A and τ_α errors, constrains M_V to less than 2H/H, as shown by the black trace in Figure 10(a). The same delay would only be 0.1% of a 10μs period, and so at 100kHz, M_V could be as high as 125H/H. Similarly, neglecting other errors, a time constant less than 200% of T_{SW} or a gain error more than 10% would limit M_V to 10H/H (as shown with the black traces in Figure 10(b)-(c), respectively). Furthermore, without nonlinearity (i.e., τ_α is infinite) a 10% delay and 10% gain error would limit M_V to less than 2H/H (as denoted by the light gray trace in Figure 10(b)), negating almost entirely the cancellation purpose of i_R. However, intentionally reducing time constant τ_α to 20% of T_{SW} in the presence of these errors increases M_V to 10H/H. A similar adjustment of τ_α is just as effective when t_d is 2.5% and K_A is 5% (Figure 10(b)). Note Figure 10 includes the combined effects of amplitude, delay, and nonlinearity errors and illustrates how various relative combinations of these errors alter the resulting multiplication factor of the circuit. Also note that even though the expressions derived earlier neglected the effects of a ripple in v_O, the simulation results shown do not, for they include the effects of C_O and $R_{ESR.C}$ both of which produce this ripple. Nevertheless, the derived expressions for the most part predict the results well because the ripple in the output of a switching supply, by design, is small.

Two of the examples discussed above were simulated, and the results are summarized in Table 1. In the first, just as in the experimental results shown inFigure 2, K_A is 30%, t_d is 3.5%, and τ_α is practically infinite. The simulated multiplication factors in this case are modest, but they agree with the experimental result and are predicted by Eqn. (28), which is applicable because of the negligible nonlinearity. In the second case, K_A is 10%, t_d is 10%, and τ_α is 22%, which are the conditions chosen to demonstrate an optimal combination of delay and nonlinearity, as depicted in Figure 9; by itself, t_d would prohibit a worthwhile multiplication factor. Note that even though t_d is only 10ns (and it would be difficult to achieve a lower t_d), t_d remains a considerable fraction of T_{SW}, which is only 100ns. Nevertheless, due to the cancellation effect of nonlinearity, M_V is 11.5 so the multiplier circuit suppresses the output voltage ripple by more than an order of magnitude.

Generally, in increasing inductor multiplication factor M_V, partially canceling the effects of one dominant error requires making one or two of the remaining errors equally significant. Additionally, the sensitivity of M_V to K_A in light of moderate-to-large delay and nonlinearity is lower (i.e., dark and light gray traces are relatively flat in Figure 10(c)) when compared to t_d and τ_α under similar conditions (as shown with the dark and light gray traces in Figure 10(a)-(b)), which means the effects of t_d overwhelm those of K_A, and τ_α is more effective in compensating for t_d. Given delays in the signal path of i_L and i_R and that output inductance L_O can vary by as much as 40% or more with process corners and temperature, a post-processing tuning or trimming scheme with at least first-order temperature-tracking features is necessary, and performing this calibration cycle *in situ* and periodically is ideal, but maybe not essential.

5. Conclusions

Current-mode inductor multipliers for switching power-supply applications suffer from sensitivity to delay (i.e., t_d), gain error (i.e., K_A), and nonlinearity (i.e., time constant τ_a) in the replica current (i.e., i_R) supposed to cancel the ac component of inductor current i_L. While a gain error in i_R retains the triangular shape desired in switching power supplies, delay and nonlinearity induce trapezoidal and sinusoidal current signals. Ultimately, however, their effects on regulator accuracy (i.e., output ripple voltage Δv_O) depend on output capacitor C_O and its equivalent series resistance $R_{ESR.C}$, given low $R_{ESR.C}$ values integrate effective output current $i_{L(eff)}$ and large $R_{ESR.C}$ values only linearly translate $i_{L(eff)}$, which is why inductor multiplication factor M_V is best based on voltage ripple Δv_O and not on current ripple $\Delta i_{L(eff)}$. Ultimately, given typical circuit delays of 50-100ns and practical state-of-the-art switching frequencies of 5-10MHz, M_V is particularly sensitive to delay, but tuning or trimming nonlinearity can offset those effects and yield an M_V on the order of 10H/H. Nonlinearity aside, in maximizing M_V, sensing i_L to generate i_R, as presented in [5], [6], [9], and [11], is more challenging than predicting i_R with feed-forward techniques, as in [10] and [13], because the latter offsets delay by tapping further back in the ac-signal chain. Matching and tracking the feed-forward delay in i_R to the delay in i_L remains a practical challenge, but in this way, the total delay between i_R and i_L might realistically stay within 5-10ns so that a factor of roughly 10H/H may be achieved at 5-10MHz, where 50-100nH on-chip inductors start becoming viable. The possibility of fully integrating the switching power supply on chip (i.e., system-on-chip -SoC- solution) while producing state-of-the-art performance appeals to the portable electronics market, especially the promising wireless micro-sensors space.

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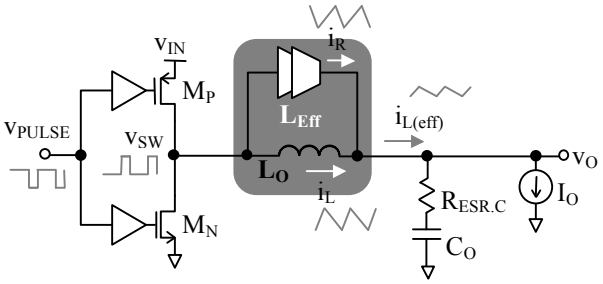
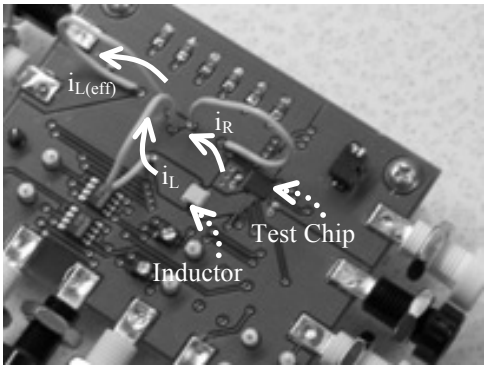
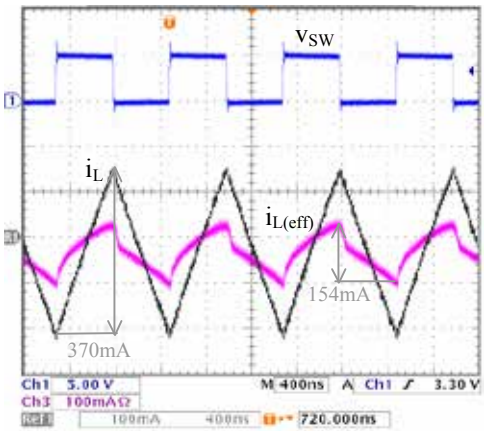


Figure 1. Current-mode inductor multiplication in a buck switching dc-dc supply circuit.



(a)



(b)

Figure 2. Prototyped inductor multiplier IC in the printed-circuit board (PCB) used to test it (a) and the experimental waveforms measured (b).

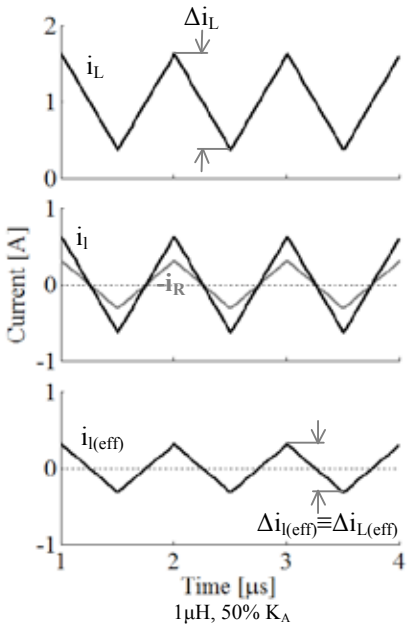


Figure 3. Spice simulation results showing the effect of amplitude error K_A in replica current i_R on output ripple current $i_{l(eff)}$.

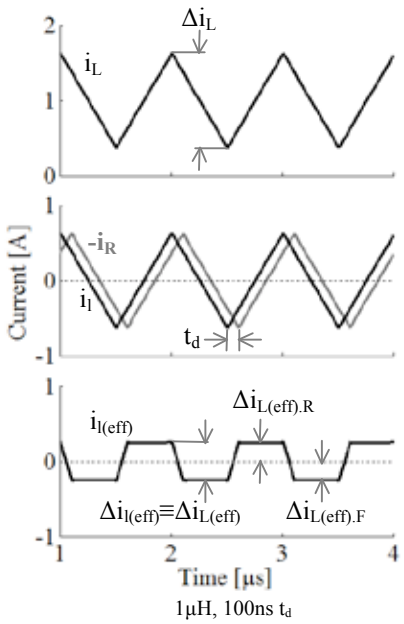


Figure 4. Spice simulation results showing the effect of delay error t_d in replica current i_R on output ripple current $i_{l(eff)}$.

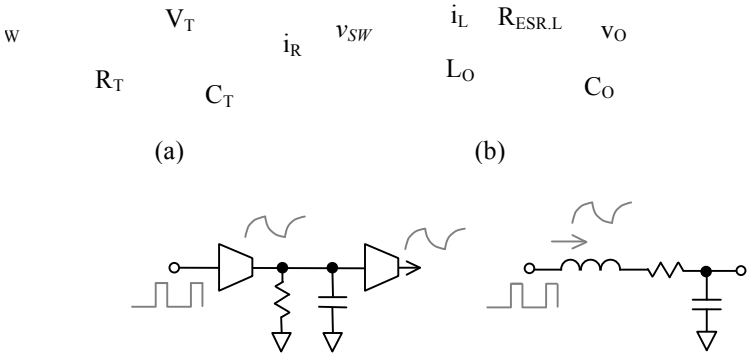


Figure 5. The nonlinear effects of the (a) parasitic filter resistor in the replica-current circuit on replica current i_R and (b) inductor's equivalent series resistance $R_{ESR.L}$ in the power stage of a switching buck regulator on inductor current i_L.

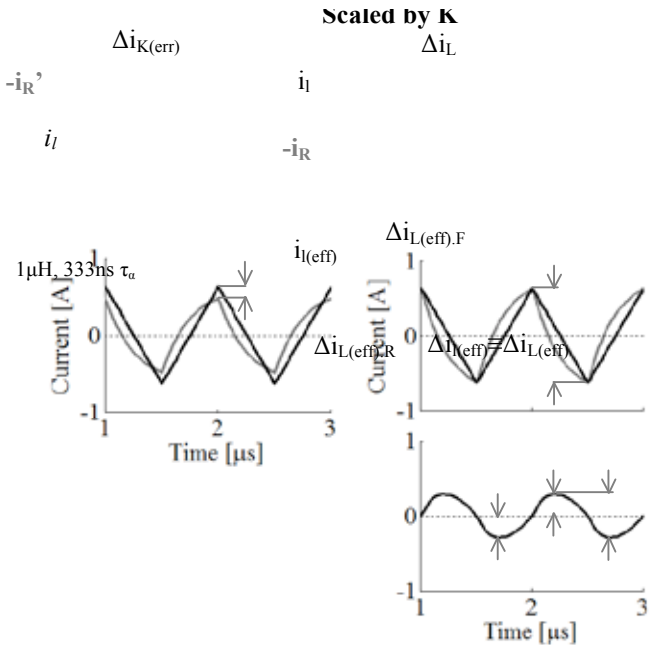


Figure 6. Spice simulations showing the effect of nonlinearity in replica current i_R on output ripple current $i_{L(eff)}$.

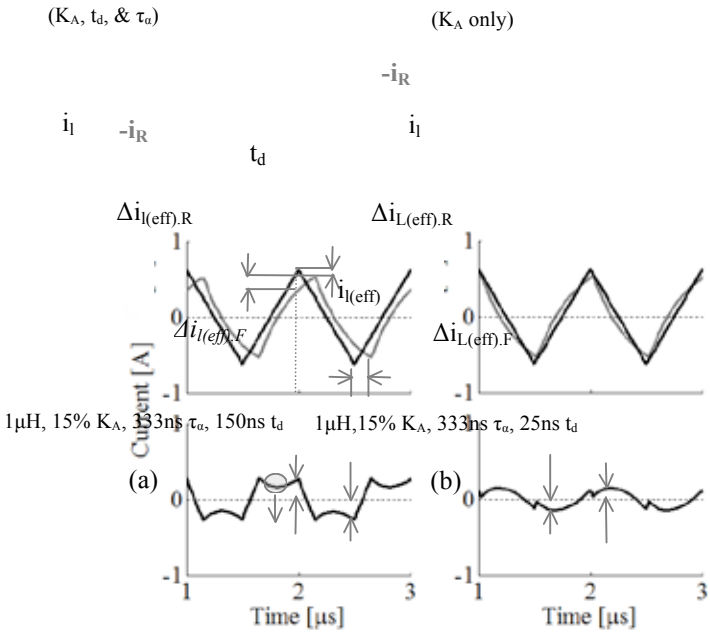


Figure 7. Spice simulation results showing the effect of nonlinearity time-constant error τ_α in the presence of amplitude and delay errors K_A and t_d in replica current i_R on output ripple current $i_{l(eff)}$ when K_A and t_d (a) are and (b) are not dominant.

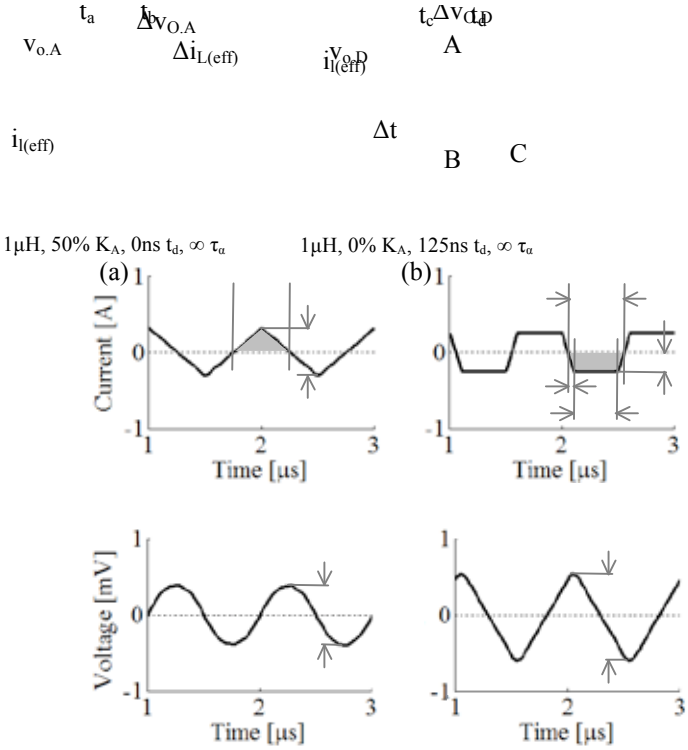


Figure 8. Spice simulation results showing the effects of (a) gain K_A and (b) delay t_d errors on output voltage ripple Δv_O.

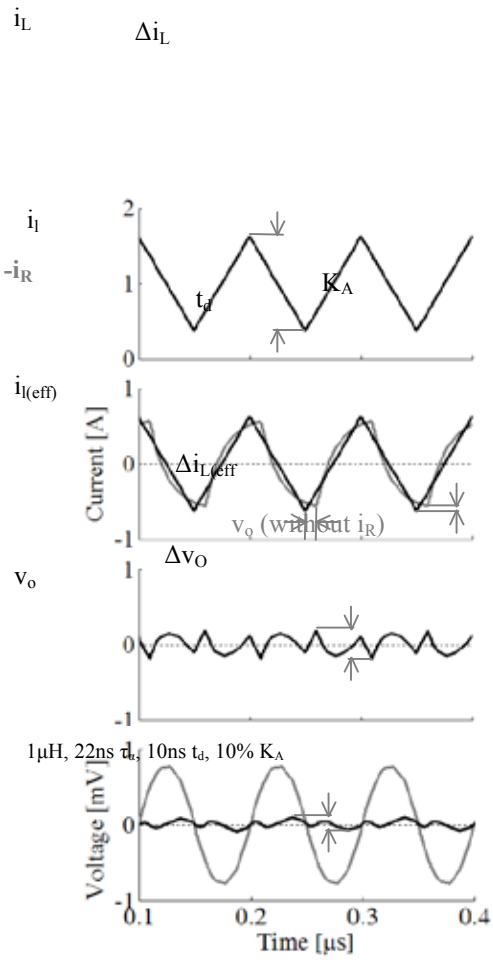


Figure 9. Spice simulation results showing how using the nonlinearity (τ_a) in replica current i_R to compensate for delay error t_d generates a ripple current $\Delta i_{L(eff)}$ that crosses zero more often and produces a smaller supply output ripple voltage Δv_O.

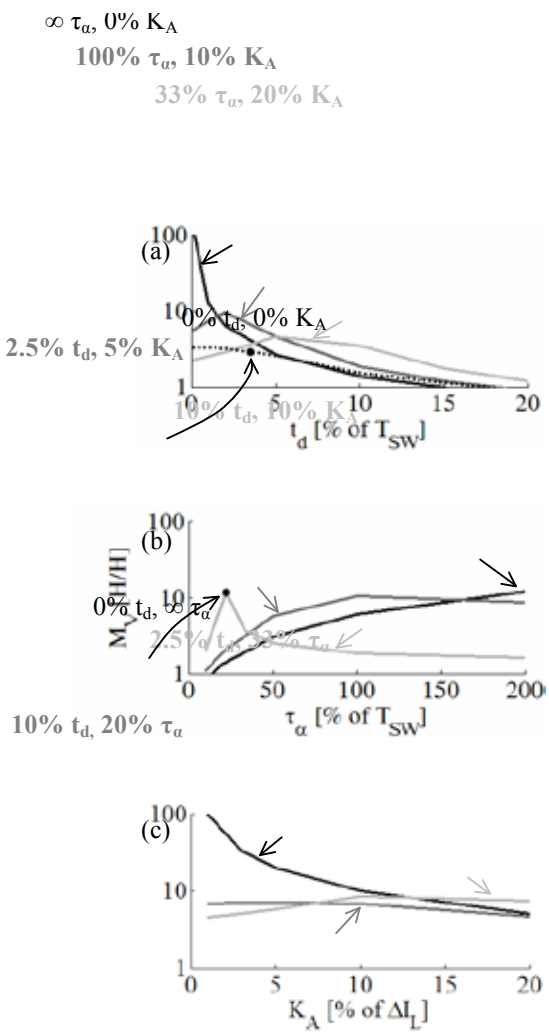


Figure 10. Spice simulation results showing the combined effects of delay t_d, nonlinearity τ_α, and gain error K_A on inductor multiplication factor M_V with respect to (a) t_d, (b) τ_α, and (c) K_A.

TABLE 1. SIMULATION RESULTS FOR COMPARISON WITH EXPERIMENTAL EXAMPLE

	Example 1 (Figure 2)	Example 2 (Figure 9)
Δi_L (mA_{PP})	378*	1250
Δi_R (mA_{PP})	265	1125
K_A (%)	30	10
T_{SW} (μs)	1	0.1
t_d (ns)	35	10
t_d (% of T_{SW})	3.5	10
L (μH)	3.3	1
R_{ESR} (Ω)	0.335	45
τ_α (% of T_{SW})	980 (~ ∞)	22
$\Delta i_{L(eff)}$ (mA_{PP})	151*	375
M_I	2.5*	3.3
M_V	2.9	**11.5**

* Compare to Experiment in Figure 2.