

Maximizing Power-Transfer Efficiency in Low-Power DC–DC Converters

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Wireless microsensors can add energy- and life-saving intelligence to remote and inaccessible places like factories, hospitals, etc. For this, they normally house sensors, data converters, digital processors, memory, transmitters, and power supplies. Although some of these functions can demand milliwatts at a time, the events monitored are typically so sporadic and sparse in time that average consumption is in microwatts. Still, tiny batteries cannot supply power for long, so power supplies cannot afford to burn much power. This is why reducing the power that switched-inductor supplies lose when delivering microwatts is critical. For these power levels, this paper shows that balancing switches to deliver fixed energy packets in discontinuous-conduction mode (DCM) and adjusting their frequency to modify power level is the most efficient means of managing a dc–dc converter. In other words, fixing the inductor's peak current and adjusting frequency is more efficient than fixing frequency and adjusting peak current. In fact, experimental measurements show that fixing peak current to 6 mA and adjusting frequency to supply up to 250 μ W is 2%–10% more efficient than fixing frequency at 40, 80, and 120 kHz and 1.4%–7% more efficient than fixing current at 5 and 10 mA.

Average power consumption for autonomous microsystems that collect, process, and transmit information across factories, hospitals, and farms is often 10–250 μ W [1]. Since tiny on-board batteries deplete easily, power-supply circuits for these applications cannot dissipate much power. In this respect, switched inductors are better than their competing alternatives because switched capacitors normally require many more switches and switches in linear regulators drop much higher voltages [2].

Switched-Inductor Converters: Switched inductors transfer energy by energizing and draining an inductor L_X in alternating phases of a switching cycle from an input source v_{IN} into a receiving output v_O . In Fig. 1, for example, switches S_{IN} and S_E close first to energize L_X from v_{IN} . S_{IN} and S_E then open and S_D and S_O close to drain L_X into v_O . Since L_X 's voltage v_L is positive and constant across energizing time t_E , L_X 's current i_L in Fig. 2 rises linearly across t_E . Similarly, because v_L is negative and nearly constant across drain time t_D , i_L falls linearly across t_D . The net result is that i_L ripples Δi_L about an average $i_{L(AVG)}$.

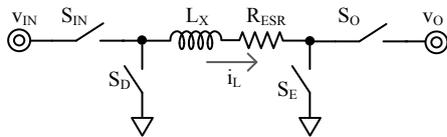


Fig. 1 Non-inverting buck–boost switched-inductor converter.

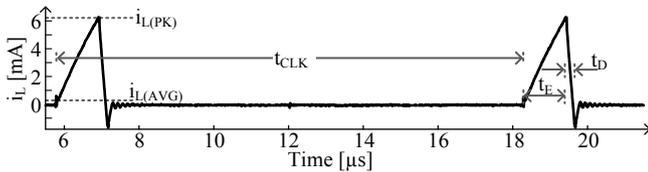


Fig. 2 Measured inductor current in discontinuous conduction (DCM).

When v_O is less than v_{IN} , L_X can energize from v_{IN} into v_O directly because $v_{IN} - v_O$ is still positive this way. This is why S_E and S_O are absent and L_X connects to v_O in typical buck converters. Similarly, when v_{IN} is less than v_O , L_X can drain from v_{IN} to v_O because $v_{IN} - v_O$ is still negative. This is the reason boost converters exclude S_{IN} and S_D and connect v_{IN} to L_X directly. In other words, buck and boost converters are special cases of the non-inverting buck–boost case in Fig. 1.

Low-Power Operation: In continuous-conduction mode (CCM), i_L ripples about an average $i_{L(AVG)}$ that is high enough to keep i_L from ever reaching zero. When delivering microwatts, though, $i_{L(AVG)}$ is so low

that the only way to keep L_X in CCM is to keep the ripple Δi_L in the microwatt range. For this, the converter must switch states at tens of megahertz, for which switching power losses are excessive. Luckily, inserting rest periods between successive energy packets like Fig. 2 shows alleviates this sacrifice. This way, in discontinuous-conduction mode (DCM), L_X transfers a large energy packet that, across a long clock period t_{CLK} , delivers microwatts. Since $i_{L(PK)}$ is higher for larger packets, t_E and t_D can be longer and sufficiently infrequent to keep switching losses low [3].

Power-Conversion Efficiency: The size and frequency of the energy packets that L_X delivers sets how much power v_{IN} sources with P_{IN} :

$$P_{IN} = \frac{E_{IN}}{t_{CLK}} = E_{IN} f_{CLK}, \quad (1)$$

where E_{IN} is input energy per cycle and t_{CLK} and f_{CLK} the clock period and corresponding frequency. Unfortunately, the controller, the switches, and L_X 's equivalent series resistance R_{ESR} consume energy E_C , E_{SW} , and E_{ESR} that together add to E_{LOSS} . This means, v_O receives with E_O a fraction of E_{IN} that power-conversion efficiency η_C describes with

$$\eta_C = \frac{E_O}{E_{IN}} = \frac{E_{IN} - E_{LOSS}}{E_{IN}} = 1 - \frac{E_{LOSS}}{E_{IN}} < 100\%. \quad (2)$$

Increasing η_C therefore amounts to reducing fractional losses E_{LOSS}/E_{IN} .

Energy per Cycle: Since i_L reflects how much energy L_X stores, E_{IN} in the case of Fig. 1 is the energy in L_X at the end of the energizing period t_E , when i_L peaks at $i_{L(PK)}$:

$$E_{IN} = 0.5 L_X i_{L(PK)}^2. \quad (3)$$

For this, S_{IN} and S_E impress v_{IN} across L_X long enough across t_E to raise i_L to $i_{L(PK)}$:

$$t_E = \frac{L_X i_{L(PK)}}{v_{IN}} \propto i_{L(PK)}, \quad (4)$$

which means t_E rises with $i_{L(PK)}$. S_D and S_O similarly impress $-v_O$ across L_X long enough across t_D to reduce i_L from $i_{L(PK)}$ to zero:

$$t_D = \frac{L_X i_{L(PK)}}{v_O} \propto i_{L(PK)}, \quad (5)$$

so t_D also scales with $i_{L(PK)}$. In fact, since L_X 's equivalent series resistance R_{ESR} conducts i_L only across t_E and t_D , S_{IN} and S_E only across t_E , and S_D and S_O only across t_D , all conduction times t_{ON} similarly rise with $i_{L(PK)}$:

$$t_{ON} = \begin{cases} t_E + t_D & R_{ESR} \\ t_E & S_{IN} \text{ and } S_E \\ t_D & S_D \text{ and } S_O \end{cases} \propto i_{L(PK)}. \quad (6)$$

Minimum Switch Losses: Switches in the network dissipate ohmic energy E_R when they conduct i_L . Since i_L is nearly a triangle across every instance of t_{ON} , $i_{L(RMS)}$ across t_{ON} is $i_{L(PK)}/\sqrt{3}$ [4]. So the power P_R consumed by the resistance of a switch R_{SW} is $i_{L(RMS)}^2 R_{SW}$ across the t_{ON} fraction of t_{CLK} that R_{SW} conducts i_L . So E_R , which is P_R across t_{CLK} , is

$$E_R = \left[i_{L(RMS)}^2 R_{SW} \left(\frac{t_{ON}}{t_{CLK}} \right) \right] t_{CLK} = \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 R_{SW} t_{ON} \\ = \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 \left(\frac{\rho_{SW} L_{SW}}{W_{SW}} \right) t_{ON}. \quad (7)$$

In the case of MOS switches, R_{SW} , and as a result, E_R fall with decreasing channel resistivity ρ_{SW} and channel length L_{SW} and increasing channel width W_{SW} .

Unfortunately, MOS switches also require gate-drive energy E_G to control them. E_G , to be more specific, is the energy that the gate capacitance C_G requires to charge across its gate-drive voltage Δv_G :

$$E_G = C_G \Delta v_G^2 = (C_{OX}'' W_{SW} L_{SW}) \Delta v_G^2. \quad (8)$$

Here, of course, C_G , and as a result, E_G rise with oxide capacitance per unit area C_{OX}'' , W_{SW} , and L_{SW} .

Since both E_R and E_G fall with shorter lengths, L_{SW} should be the minimum length L_{MIN} possible. But because E_R falls and E_G rises with increasing W_{SW} , W_{SW} should neither be short nor wide. Instead,

designers should raise W_{SW} until the rise in E_G cancels the fall in E_R . In other words, E_R and E_G are at their lowest combined point when W_{SW} is optimal width W_{SW}' :

$$\left(\frac{\partial E_R}{\partial W_{SW}} + \frac{\partial E_G}{\partial W_{SW}} \right) \bigg|_{W_{SW}' = \sqrt{\frac{i_{L(PK)}^2 t_{ON} P_{SW}}{3 C_{OX} A_{VG}}} = 0. \quad (9)$$

With L_{MIN} and W_{SW}' , E_R' equals E_G' , and together, they yield $E_{SW(MIN)}$:

$$E_{SW(MIN)} = E_{R(OPT)} + E_{G(OPT)} = 2E_{G(OPT)} \propto \sqrt{i_{L(PK)}^2 t_{ON}} \propto i_{L(PK)}^{1.5}. \quad (10)$$

And since t_{ON} scales with $i_{L(PK)}$, $E_{SW(MIN)}$ rises with $i_{L(PK)}^{1.5}$.

ESR Losses: Like switches, L_X 's R_{ESR} dissipates ohmic energy E_{ESR} when R_{ESR} conducts i_L across a t_{ON} fraction of t_{CLK} :

$$E_{ESR} = \left[i_{L(RMS)}^2 R_{ESR} \left(\frac{t_{ON}}{t_{CLK}} \right) \right] t_{CLK} = \left(\frac{i_{L(PK)}}{\sqrt{3}} \right)^2 R_{ESR} t_{ON} \propto i_{L(PK)}^3. \quad (11)$$

And since t_{ON} rises with $i_{L(PK)}$, E_{ESR} is proportional to $i_{L(PK)}^3$. In other words, E_{ESR} rises more quickly with $i_{L(PK)}$ than $E_{SW(MIN)}$ does.

Controller Losses: Portions of the controller operate continuously across t_{CLK} , so energy $E_{C(DC)}$ changes with t_{CLK} :

$$E_{C(DC)} = P_{C(DC)} t_{CLK}. \quad (12)$$

Others need only engage when L_X conducts, so they may consume power a t_{ON} fraction of t_{CLK} . Energy $E_{C(DUTY)}$ for these duty-cycled blocks therefore changes with t_{ON} , and as a result, $i_{L(PK)}$, but not t_{CLK} :

$$E_{C(DUTY)} = P_{C(Q)} \left(\frac{t_{ON}}{t_{CLK}} \right) t_{CLK} = P_{C(Q)} t_{ON} \propto i_{L(PK)}. \quad (13)$$

Still others need only engage momentarily, when transitioning between switching states. These transient blocks consume power across a constant period t_{TRAN} , so energy $E_{C(TRAN)}$ is independent of both t_{CLK} and t_{ON} , and as a result, also of $i_{L(PK)}$:

$$E_{C(TRAN)} = P_{C(Q)} \left(\frac{t_{TRAN}}{t_{CLK}} \right) t_{CLK} = P_{C(Q)} t_{TRAN} \neq f(i_{L(PK)}). \quad (14)$$

Maximum Efficiency: Switched inductors in discontinuous conduction can either fix peak current $i_{L(PK)}$ and adjust frequency f_{CLK} [5] or fix f_{CLK} and adjust $i_{L(PK)}$ [6] to adjust power level. Of the two schemes, the one with the lowest fractional losses E_{LOSS}/E_{IN} , as concluded earlier, produces the highest power-conversion efficiency η_C . To determine this, first note E_{ESR}/E_{IN} rises with $i_{L(PK)}$ and $E_{SW(MIN)}/E_{IN}$ falls with $1/i_{L(PK)}^{0.5}$ and $E_{C(DUTY)}/E_{IN}$ and $E_{C(TRAN)}/E_{IN}$ fall faster with $1/i_{L(PK)}$ and $1/i_{L(PK)}^2$, as Fig. 3 shows. So like in the case of W_{SW} , designers should raise $i_{L(PK)}$ until the rise in E_{ESR}/E_{IN} cancels the drops in $E_{SW(MIN)}/E_{IN}$, $E_{C(DUTY)}/E_{IN}$, and $E_{C(TRAN)}/E_{IN}$. Note that $E_{C(DC)}/E_{IN}$ reduces to $P_{C(DC)}/P_{IN}$ and is therefore independent of $i_{L(PK)}$. In other words, fixing $i_{L(PK)}$ to its optimal setting $i_{L(PK)'}$ and adjusting f_{CLK} is the scheme that produces the highest efficiency, irrespective of E_{IN} . And since W_{SW} depends on $i_{L(PK)}$, W_{SW}' for $i_{L(PK)'}$ is optimal for all values of E_{IN} .

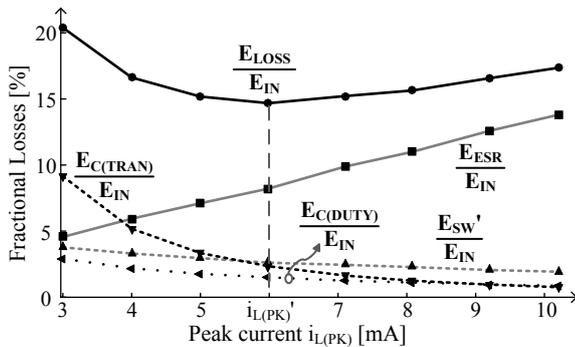


Fig. 3 Simulated fractional losses.

Validation: Figure 4 illustrates the power-conversion efficiencies η_C of a 0.3-to-1.8-V boost 0.18- μ m CMOS converter with a 47- μ H-5.6- Ω inductor in discontinuous conduction. With frequency fixed at 40, 80, and 120 kHz, η_C peaks at 57, 114, and 165 μ W, at the power levels that

correspond to the optimal $i_{L(PK)}$ and W_{SW} settings $i_{L(PK)'}$ and W_{SW}' . In other words, $i_{L(PK)}$ and W_{SW} are optimal only at particular power levels.

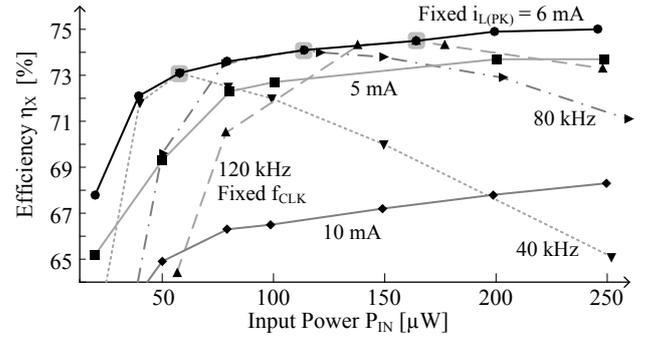


Fig. 4 Measured efficiency for fixed-peak and fixed-frequency schemes.

With $i_{L(PK)}$ fixed at 5, 6, and 10 mA, η_C is nearly flat above 50 μ W. This results because E_{ESR} , $E_{SW(MIN)}$, and $E_{C(DUTY)}$ both scale with E_{IN} and overwhelm $E_{C(DC)}$ and $E_{C(TRAN)}$, so fractional losses are nearly constant across P_{IN} . η_C falls below 50 μ W because $E_{C(DC)}$ and $E_{C(TRAN)}$ do not scale with frequency and dominate over E_{ESR} , $E_{SW(MIN)}$, and $E_{C(DUTY)}$. With losses fixed, fractional losses rise with decreasing P_{IN} below 50 μ W. Nevertheless, η_C at 6 mA is 1.4% and 7% more efficient than at 5 and 10 mA and 2%–10% more efficient than fixed f_{CLK} settings. In other words, 6 mA is the optimal $i_{L(PK)}$ setting $i_{L(PK)'}$ for all power levels.

Conclusions: This paper shows that fixing peak inductor to 6 mA and adjusting frequency to draw up to 250 μ W is 1.4%–7% more efficient than at 5 and 10 mA and 2%–10% more efficient than fixing frequency at 40, 80, and 120 kHz and adjusting peak current. And with a constant peak current, switch dimensions are optimal for all power levels. This way, microwatt power supplies can sustain more functions and tiny energy-harvesting microsystems can output more power.

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References

- Vullers, R.J.M., Van Schaijk, R., Doms, I., Van Hoof, C., Mertens, R.: ‘Micropower energy harvesting’, *Solid-State Electronics*, 2009, **53**, (7), pp. 684–693, doi: 10.1016/j.sse.2008.12.011
- Prabha, R.D., Rincon-Mora, G.A., Kim, S.: ‘Harvesting circuits for miniaturized photovoltaic cells’, *IEEE Int. Symp. Circuits Syst.*, Brazil, May 2011, pp. 309–312, doi: 10.1109/ISCAS.2011.5937563
- Kim, S., Rincon-Mora, G.A.: ‘Achieving High Efficiency under Micro-Watt Loads with Switching Buck DC-DC Converters’, *Journal of Low-Power Electronics*, **5**, (2), doi: 10.1166/jolpe.2009.1023
- Prabha, R.D., Rincon-Mora, G.A.: ‘Battery-assisted and photovoltaic-sourced switched-inductor CMOS harvesting charger-supply’, *IEEE Int. Symp. Circuits Syst.*, China, May 2013, pp. 253–256, doi: 10.1109/ISCAS.2013.6571830
- Yifeng Qiu, Van Liempd, C., Op het Veld, B., Blanken, P.G., Van Hoof, C.: ‘5 μ W-to-10mW input power range inductive boost converter for indoor photovoltaic energy harvesting with integrated maximum power point tracking algorithm’, *IEEE Int. Solid-State Circuits Conf.*, USA, Feb. 2011, pp.118–120, doi: 10.1109/ISSCC.2011.5746245
- Bandyopadhyay, S., Chandrakasan, A.P.: ‘Platform Architecture for Solar, Thermal, and Vibration Energy Combining With MPPT and Single Inductor’, *IEEE J. Solid-State Circuits*, **47**, (9), pp. 2199–2215, doi: 10.1109/JSSC.2012.