Low Output Impedance 0.6μm-CMOS Sub-Bandgap Reference

V. Gupta and G.A. Rincón-Mora

Abstract: A 0.6μm-CMOS sub-bandgap reference circuit whose output voltage is, unlike reported literature, *concurrently* low voltage and low output impedance is presented. Experimental measurements verify that the proposed circuit, which produces a first-order temperature compensated reference voltage of 890mV, sources up to 5mA of load current and rejects noise by a factor of 30.8-8.1dB at 500kHz-4MHz, neither feature of which is achieved by state-of-the-art sub-bandgap circuits.

Introduction: A low output impedance reference is desirable for noise-sensitive applications to shunt and steer noise away from sensitive nodes and source dc and ac load currents [1-2], which is why most of the references used in industry are variations of the regulated references presented in [3]. Reported regulated references, however, only produce the conventional 1.2V bandgap voltage, or a higher voltage [1-5], which is unsuitable for a growing number of high-end applications that use modern CMOS processes with low breakdown voltages. Alternatively, as shown in Fig. 1, a series linear regulator can buffer the output of a low-voltage, high output impedance reference [6-7]. The buffer, however, introduces additional random and systematic offset components to the reference, significantly degrading the overall accuracy performance of the system; these offsets, for instance, caused an additional ±4mV error in [2]. This additional error, which monopolizes 0.4% of a 1V reference, leaves little error budget for the reference itself, which is particularly troubling in CMOS technologies because MOS offsets have a

non-linear dependence to temperature and cannot be compensated with trim. Moreover, a buffer does little to attenuate the noise already present in the high impedance reference, since it simply propagates the disturbance to the output unabated. Generating a sub-bandgap reference voltage with low output impedance characteristics, for which no prior art solution was found to exist, is the objective of this paper.

Proposed Topology: For shunt feedback, which is necessary for low output impedance, the reference must be the sum of temperature-dependent voltages (not currents), as shown in the proposed circuit of Fig. 2(a), where a proportional-to-absolute temperature (PTAT) voltage is sampled and regulated via amplifier OA_1 and power PMOS MP_O. The forward-biased voltage of diode D decreases, for the most part, linearly with temperature and hence has a complementary-to-absolute-temperature (CTAT) behavior. This CTAT voltage is attenuated by the potential divider comprised of resistors R_{11} and R_{12} to produce CTAT voltage component $V_{X\text{-}CTAT}$ at node V_X.

The amplifier has a pre-set PTAT offset voltage and the loop regulates and impresses this voltage across R_{13}. The temperature-compensated output, shown in Fig. 2(b), is the sum of this PTAT voltage ($V_{R\text{-}PTAT}$), the CTAT diode-derived voltage across R_{12} ($V_{X\text{-}CTAT}$), and the additional PTAT voltage component across R_{12} ($V_{X\text{-}PTAT}$), that results from running R_{13}'s PTAT current through R_{12} ($V_{X\text{-}PTAT}$) and is given by

$$V_{REF} = V_{R-PTAT} + \left(V_{X-PTAT} + V_{X-CTAT}\right) = V_{PTAT} + V_{CTAT}. \quad (1)$$

Amplifier OA_1 and pass device MP_O constitute the high loop-gain, shunt-feedback path ($A_{ol}\beta$)) around V_{REF}. This negative feedback loop regulates the output against variations in input supply and load. Since MP_O is a large PMOS device, the regulated reference can

sustain low supply voltages under relatively high load currents, in other words, yield low dropout voltages.

Complete Schematic: The complete circuit shown in Fig. 3 is comprised of a biasing block and the output stage and amplifier presented in Fig. 2. The bias current is defined by a conventional PTAT generator block. The dominant low-frequency pole of the loop is established at the gate of MP_O through Miller-compensating capacitor C_M.

Key to this circuit is OA_1's PTAT offset voltage, which is intrinsically defined by input pair $QP_{21\text{-}22}$, whose emitter areas are 8x and x, respectively, and current mirror $MP_{21\text{-}22}$, which ensures equal currents flow through $QP_{21\text{-}22}$. The result is a PTAT difference across their base-emitter voltages (i.e., $\Delta V_{BE} = V_T \ln(8)$). The offset voltage across the bases of $QP_{21\text{-}22}$ is the voltage divided version of the voltage across R_{13} ($V_{R\text{-}PTAT}$); or equivalently, $V_{R\text{-}PTAT}$ is an amplified version of the PTAT voltage present at the bases of $QP_{21\text{-}22}$,

$$V_{R-PTAT} = \left(\frac{R_{14} + R_{15}}{R_{15}} \right) \Delta V_{BE} . \tag{2}$$

This voltage defines R_{13}'s PTAT current, which ultimately flows into node V_X. Resistors R_{14} and R_{15} therefore implement a voltage divider circuit whose total resistance and series combination is modeled by R_{12}. The first-order temperature compensated reference voltage is consequently given by

$$V_{REF} = K_1 V_{BE} + K_2 K_3 \Delta V_{BE} = K_1 \left(V_{BE} + \frac{K_2 K_3}{K_1} \Delta V_{BE} \right), \tag{3}$$

where K_1, K_2, and K_3 are

$$K_1 = \frac{(R_{14} + R_{15}) \| R_{12}}{[(R_{14} + R_{15}) \| R_{12}] + R_{11}}, \quad (4)$$

$$K_2 = \frac{R_{14} + R_{15}}{R_{15}}, \quad (5)$$

and

$$K_3 = 1 + \frac{R_{11} \| R_{12} \| (R_{14} + R_{15})}{R_{13}}. \quad (6)$$

The lateral PNP devices of the process were characterized for parameters like forward beta (BF), Early voltage (VAF), and saturation current (IS), among others. The values of these parameters were found to be 100A/A, 6V, and 3fA, respectively. This high beta allows base currents to be neglected while deriving Eq. (2)-(6).

Results: The proposed circuit was fabricated with AMI's 0.6μm CMOS process technology ($V_{TN} \approx 0.7V$ and $|V_{TP}| \approx 0.9V$) through the MOSIS design facility. The temperature coefficient of 20 samples, showing a sub-bandgap output of 890.5mV, is presented in Fig. 4(a). The transient load-induced variation of the reference when subjected to a load current step of 0-5mA with 100ns rise and fall times, shown in Fig. 4(b), is a measure of the circuit's ability to suppress load-dump effects.

To gauge the noise-shunting capabilities of the proposed circuit against the state-of-the-art, a current-mode 890mV sub-bandgap reference was built by sourcing 49μA into an 18kΩ-10pF output resistor-capacitor combination, as illustrated in Fig. 5(a). To emulate noise injection through parasitic coupling capacitors, a noise current of roughly 125μA was injected into the reference (state-of-the-art $V_{REF\text{-}SOA}$ and proposed V_{REF}), as shown in Figs. 5(a) and 5(b). A comparison of the transient response of the two circuits (Fig. 5(c)) shows how the proposed reference suppresses most of the broadband ac noise

injected, quickly recovering its output to the desired level. The frequency spectra of the two waveforms (Fig. 5(d)) reveal that the proposed circuit (V_{REF}) further rejects noise by a factor of 30.8-8.1dB ($V_{REF-SOA}$-to-V_{REF} noise power ratio) at 500kHz-4MHz.

Conclusions: A 0.9V, 34.7ppm/°C, 5mA, low output impedance 0.6μm CMOS sub-bandgap reference has been designed, fabricated, and evaluated. The principal features of the proposed circuit are low impedance and sub-bandgap output voltages, concurrently, the combination of which was not found in literature, patents, or commercial products without the use of series shunt-regulators, which degrade accuracy.

References

1 C.Lee, K. McClellan, and J. Choma Jr., "A supply-noise-insensitive CMOS PLL with a voltage regulator using dc-dc capacitive converter," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1453-1463, Oct. 2001.

2 K. Manetakis, "CMOS micro-power output stage for integrated voltage references," *IEE Electronics Letters*, vol. 40, pp. 917-918, 22 July 2004.

3 A.P. Brokaw, "A simple three-terminal IC bandgap reference", *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 388-393, Dec. 1974.

4 M.G.R. Degrauwe, O.N. Leuthold, E.A. Vittoz, H.J. Oguey, and A. Descombes, "CMOS voltage references using lateral bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 6, pp. 1151-1157, Dec. 1985.

5 E. A. Vittoz, "MOS transistors operated in the linear bipolar mode and their application in CMOS technology," *IEEE J. Solid-State Circuits,* vol. 18, pp. 273-289, 1983.

6 K.N. Leung, P.K.T. Mok, "A sub-1-V 15ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, pp. 526-530, April 2002.

7 H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, pp. 670-674, May 1999.

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Figure Captions

Fig. 1. Reference-regulator low impedance circuit and its adverse treatment of noise and offset.

Fig. 2. (a) Concept and (b) temperature behavior of proposed reference.

Fig. 3. Complete schematic of proposed low impedance, sub-bandgap reference.

Fig. 4. (a) Temperature dependence of trimmed samples and (b) transient load regulation.

Fig. 5. Noise rejection measurements: set-up for (a) the state-of-the-art sub-bandgap reference and (b) proposed circuit and corresponding ac-coupled (c) transient and (d) frequency ($V_{REF\text{-}SOA}$-to-V_{REF} noise power ratio) response.

Figure 1

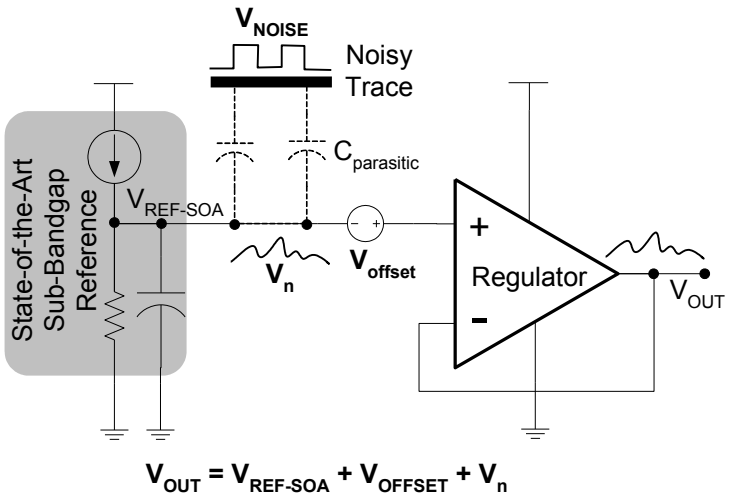

V_NOISE
Noisy Trace
C_parasitic
State-of-the-Art Sub-Bandgap Reference
V_REF-SOA
V_n
V_offset
+
Regulator
-
V_OUT
V_OUT = V_REF-SOA + V_OFFSET + V_n

Figure 2

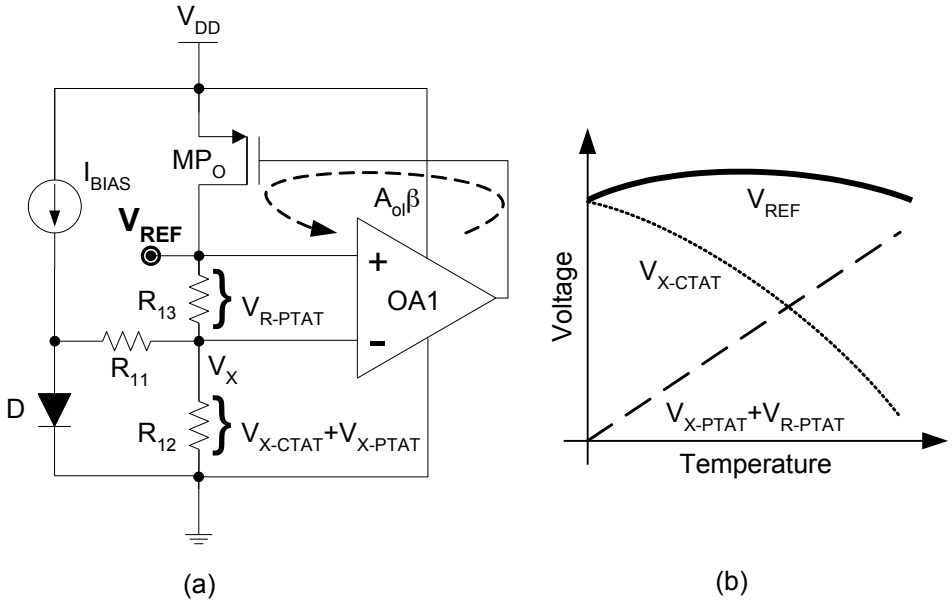

V_DD
MP_O
I_BIAS
A_olβ
V_REF
+
OA1
-
R_13
V_R-PTAT
R_11
V_X
D
R_12
V_X-CTAT+V_X-PTAT
(a)
Voltage
V_REF
V_X-CTAT
V_X-PTAT+V_R-PTAT
Temperature
(b)

Figure 3

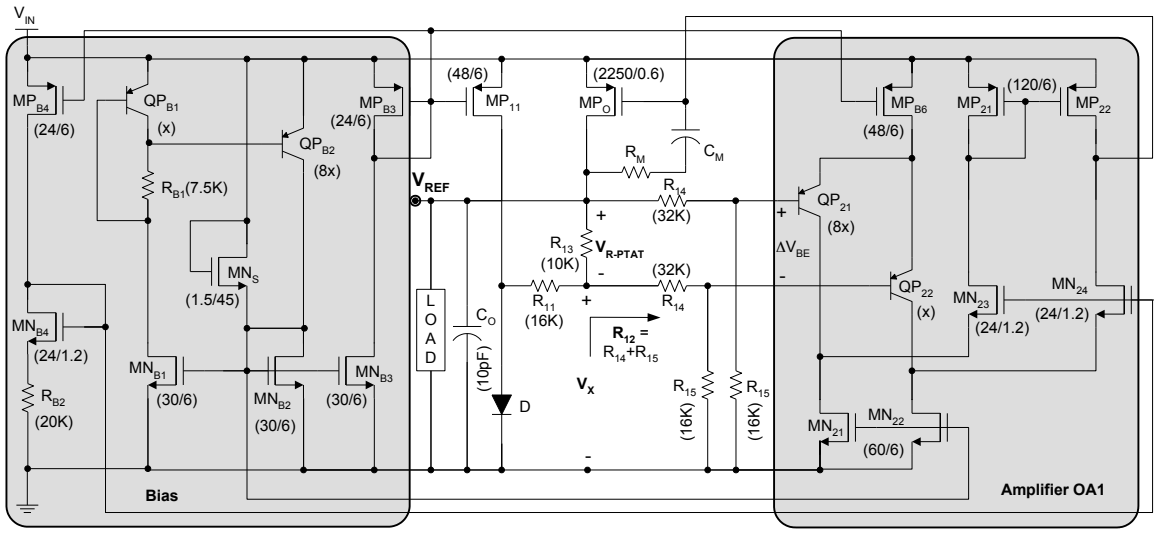
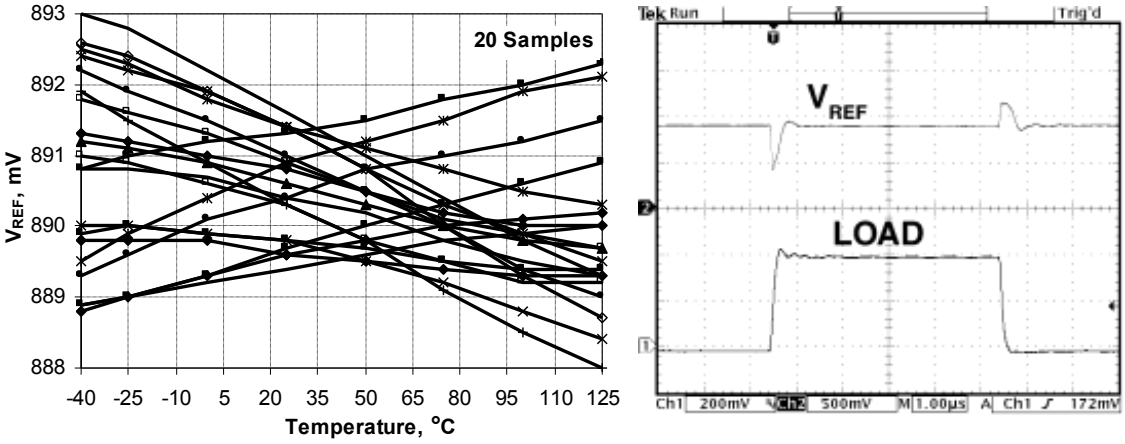
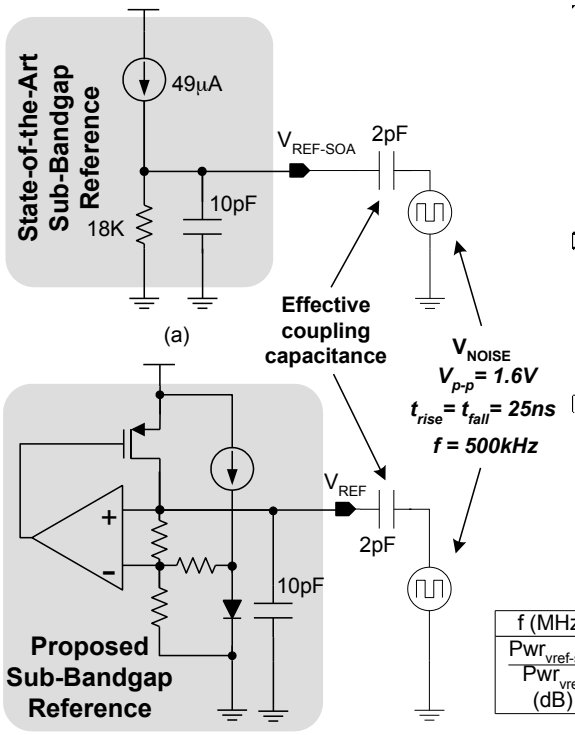

V_IN
MP_B4
(24/6)
QP_B1
(x)
R_B1(7.5K)
MN_S
(1.5/45)
MN_B4
(24/1.2)
R_B2
(20K)
MN_B1
(30/6)
MN_B2
(30/6)
MP_B3
(24/6)
MN_B3
(30/6)
QP_B2
(8x)
Bias
V_REF
(48/6)
MP_11
LOAD
C_O
(10pF)
D
(2250/0.6)
MP_O
R_M
C_M
R_14
(32K)
R_13
(10K)
V_R-PTAT
R_11
(16K)
(32K)
R_14
R_12 = R_14+R_15
V_X
R_15
(16K)
R_15
(16K)
MP_B6
(48/6)
QP_21
(8x)
ΔV_BE
QP_22
(x)
MP_21
(120/6)
MP_22
MN_23
(24/1.2)
MN_24
(24/1.2)
MN_21
MN_22
(60/6)
Amplifier OA1

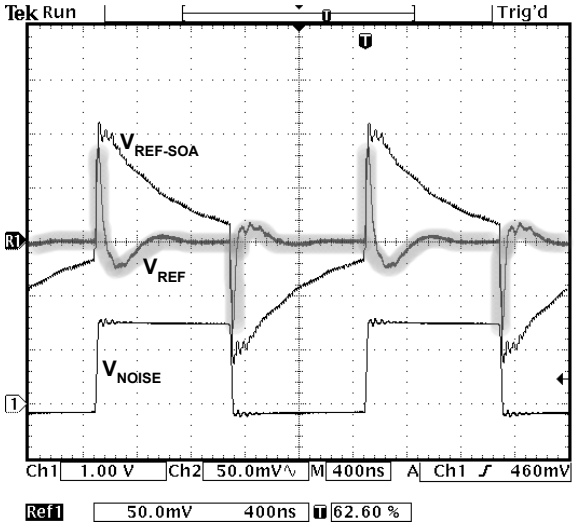
Figure 4


20 Samples
893
892
891
890
889
888
V_{REF}, mV
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature, °C
Tek Run
Trig'd
V_{REF}
LOAD
Ch1 200mV
Ch2 500mV
M 1.00µs
A Ch1 172mV

(a) (b)

Figure 5





(c)

f (MHz)	0.5	1	2	4	8	16	32	64	128	256
$\frac{Pwr_{vref-soa}}{Pwr_{vref}}$ (dB)	30.8	9.25	8.7	8.1	-9.5	-3.0	14.4	14.8	16.1	12.5

(d)