Dual-Source Hysteretic Switched-Inductor 0.18-µm CMOS Charger–Supply System

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Abstract: Although miniaturized fuel cells store more energy than lithium-ion batteries and super capacitors, they source less power, which means they cannot power as many functions. Their power-dense counterparts, however, cannot sustain life for long, which is why mixing technologies is appealing. Still, microsystems are tiny and react quickly, so their supply circuits must also be small and fast. For this reason, the dual-source hysteretic single-inductor 0.18-µm CMOS charger–supply system presented and discussed here draws constant power from an energy-dense source and supplementary power from a rechargeable power-dense battery. The prototyped system supplies and responds to 1–4-mA load dumps within one or two clock cycles with 73% peak efficiency and recharges the battery with excess power from the energy-dense source. When managed to draw supplementary power from a battery this way and loaded with a microsystem that idles at 10 µW and peaks to 4 mW, as in the case of typical wireless sensors, the combined weight of the sources required is 68% less than those of the state of the art.

Index Terms: Single switched inductor, hysteretic control, switching dc–dc converter, dual sources, multiple inputs, multiple outputs, and CMOS charger and supply.

I. MICROSYSTEMS

Wireless microsensors and other emerging microsystems require highly integrated and functionally dense solutions that operate for months or years at a time [1]–[2]. Since they idle and sense, collect, process, and transmit information, they draw a wide range of power levels

[3]–[4]. Unfortunately, energy-dense sources cannot supply high power and their power-dense counterparts cannot sustain power for long [5]. And no single technology is both energy and power dense [6]. This is why dual-source systems are normally smaller [7].

The dual-source hysteretic switched-inductor CMOS charger–supply system prototyped and presented here is fast, compact, and power efficient. Plus, it draws power from a power-dense source only when needed to fully leverage the operational life benefits of the energy-dense counterpart. To illustrate the limits and advantages of this technology, Sections II and III discuss miniaturized sources, mixed sources, and the state of the art in mixed-source supplies. Sections IV–VI then describe the prototyped system, its power losses, and its measured performance. Section VII ends by drawing relevant conclusions.

II. MIXED SOURCE

To sustain both low average power consistently and high transmission power sporadically in single-source systems, designers must oversize either an energy-dense source to supply more power or a power-dense device to store more energy. In these high peak-to-average power scenarios, sharing space between two complementary sources and sizing one for lifetime and the other for peak power requires less overall space [8]. In other words, drawing assistance from a power-dense source to supplement an energy-dense device is both more compact and longer lasting than either technology can be on its own.

A sensor can, for example, consume 4 mW for 1% of the time when transmitting data, 1.2 mW for another 1% when sensing, 1 mW for yet another 1% when processing, and 10 μW for the remaining 97% of the time when idling [4]. For this, the 1-kWh/kg direct methanol fuel cell (DMFC) [9] that can supply the average 72 μW needed to supply the system for one month is

lighter at 50 mg than the corresponding lithium-ion battery at 250 mg [10]. Notwithstanding, the DMFC that can supply 4 mW is heavier at 400 mg than the corresponding lithium ion at 20 mg. Fortunately, the 50-mg DMFC that can sustain the system for one month and the 20-mg lithium ion that can supply 4 mW together weigh less at 70 mg than the 400-mg DMFC and 250-mg battery required to sustain the system.

III. The State of the Art in Mixed-Source Supplies

Power-supply circuits should be energy efficient and compact to fully reap the volume savings gained from using mixed sources. They must also be flexible because the voltage and power levels that sources supply and loads demand are diverse and mismatched. Linear regulators are not ideal in this respect because they can supply loads efficiently only when their output voltages are slightly below their input voltages [11]. Similarly, switched capacitors are efficient only for a narrow range of input and output voltages [12]. Switched inductors, on the other hand, can draw and supply power efficiently across a wide range of input and output voltages [13]–[14].

The simplest way of managing several inputs and outputs efficiently is to allocate one switched inductor to each input–output pair. Several inductors, however, require substantial space. Although transformers can reduce volume by sharing one core, the core and windings still occupy considerable real estate [15]. Ultimately, the best way to save space is to share one inductor, and to time-multiplex that inductor between all inputs and outputs [14], which is what the single-inductor, multiple-output (SIMO) systems in [16]–[19] achieve.

With only one input, however, [16] and [18]–[19] must oversize one energy-dense source to supply peak power or one power-dense source to sustain loads for extended periods. Even with two sources, [17] suffers from similar tradeoffs because one of its sources is not always available,

so the remaining source must nonetheless supply all the power and energy needed. To avoid this sacrifice, the system should draw peak power from a power-dense source and average power from an energy-dense source. This functionality, however, is largely absent in the state of the art.

IV. Proposed Dual-Source Hysteretic Converter

The charger–supply system in Fig. 1a draws constant power P_{ED} from an energy-dense source v_{ED} and variable power P_{PD} from a power-dense rechargeable device v_{PD} to supply a load. When lightly loaded, the system recharges v_{PD} with excess v_{ED} power. For this, the network connects inductor L_O so it can energize from either v_{ED} or v_{PD} and drain into either the load at v_O or v_{PD}. L_O essentially transfers energy packets between v_{ED}, v_{PD}, and v_O in discontinuous-conduction mode (DCM), draining L_O fully before re-energizing it again from the same or from another source. Because the power-supply system derives power from two sources to supply a load and recharge a battery, the system manages multiple inputs and multiple outputs.

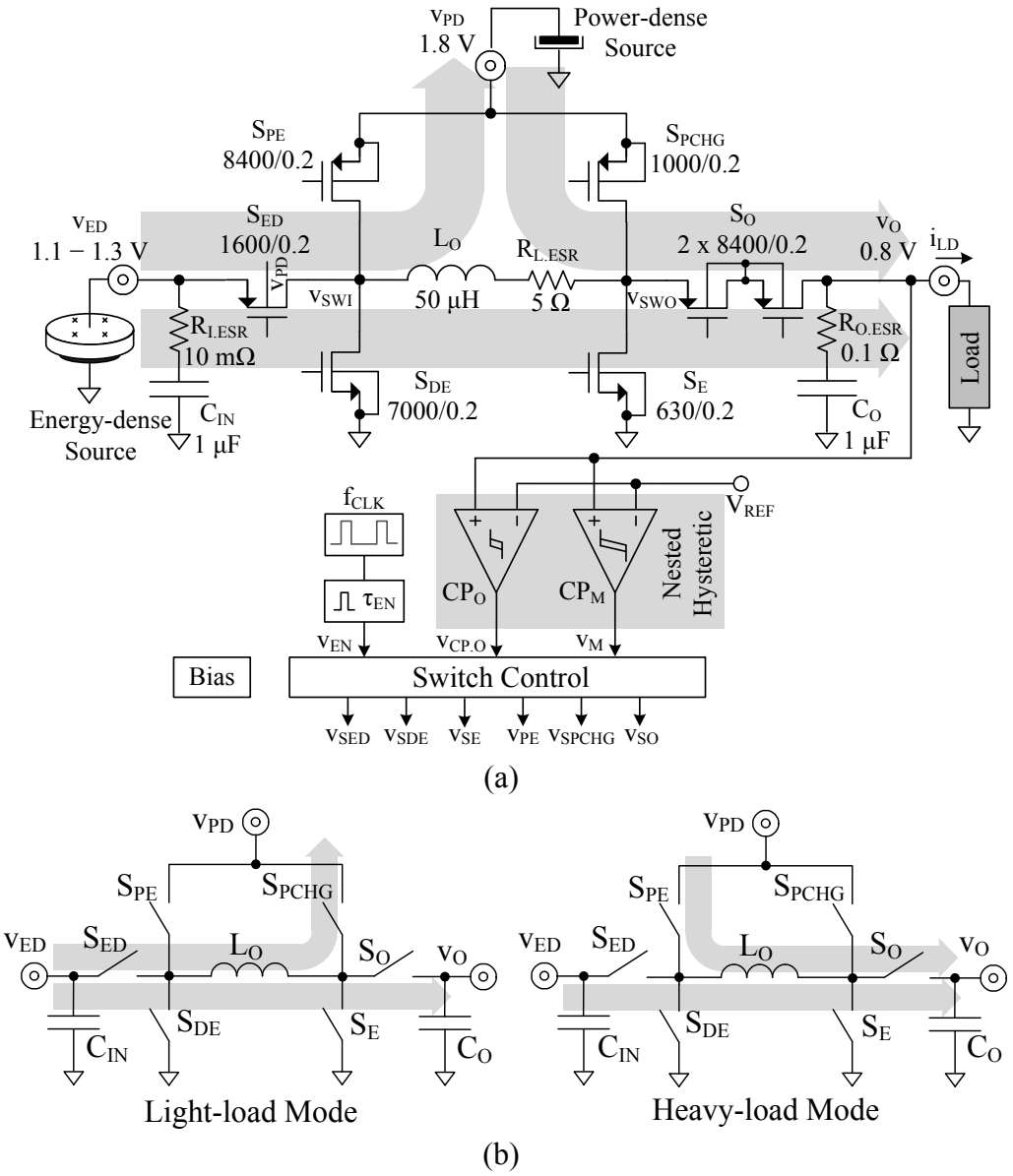


Fig 1. (a) Dual-source hysteretic charger–supply system and (b) energy flow across the switched-inductor network.

A. Energy Flow

Light-Load Mode: When energy-dense power P_{ED} exceeds load power P_{LD}, the system supplies P_{LD} to the output v_O from P_{ED} and excess P_{ED} power to the rechargeable power-dense source v_{PD}. In this mode, S_{ED} and S_E in Fig. 1 close to energize L_O from the energy-dense source v_{ED}. After a

fixed energizing time τ_{EN}, S_{ED} and S_E open and CP_O determines where to drain L_O. If v_O is below CP_O's lower threshold, S_{DE} and S_O close to drain L_O into v_O; otherwise, S_{DE} and S_{PCHG} close to deplete L_O into v_{PD}. In other words, the system in light-load mode draws power from one input source v_{ED} to service two outputs: v_O and v_{PD}.

Heavy-Load Mode: When energy-dense power P_{ED} is unable to sustain load power P_{LD}, v_O falls below the lower threshold of the mode-control comparator CP_M in Fig. 1, which prompts the system to draw supplementary power from the power-dense source v_{PD}. In this mode, the system closes S_{PE} and S_O in Fig. 1 to energize L_O from v_{PD} directly into v_O in buck-mode fashion. S_{PE} then opens and S_{DE} closes to deplete L_O into v_O. If i_L reaches zero and v_O still needs power, the system opens S_{DE} and closes S_{PE} again to start another energizing event from v_{PD} to v_O. Since power-dense power P_{PD} exceeds load power P_{LD}, v_O generally rises across this time.

If v_O is above the upper threshold of CP_O when i_L reaches zero, CP_O commands the system to open all switches. At the onset of the next clock cycle, the system again starts by extracting power from the energy-dense source v_{ED}. S_{ED} and S_E therefore close to energize L_O from v_{ED} and S_{DE} and S_O close afterwards to drain L_O into v_O. But since v_{ED}'s power P_{ED} is not high enough to sustain P_{LD}, v_O falls when it receives P_{ED} from L_O. So when v_O falls below CP_O's lower threshold, the system again draws P_{PD} from v_{PD} to raise v_O back to CP_O's upper threshold. As a result, the system in heavy-load mode extracts power from two sources v_{ED} and v_{PD} to supply one output v_O.

B. Switching Sequences

The energy- and power-dense sequences of the system refer to the switching events that allow the system to derive power from the energy- and power-dense sources v_{ED} and v_{PD}. So, since the network only derives power from v_{ED} when lightly loaded, the switches never shift out of the

energy-dense sequence. When heavily loaded, though, the system alternates between the two sequences to supplement v_{ED}'s power P_{ED} with v_{PD}'s power P_{PD}.

Energy-Dense Sequence: The rising edge of an internal 40-kHz clock f_{CLK} in Fig. 2 starts every switching cycle in Fig. 3a by drawing and delivering one energy packet E_{ED} from v_{ED} to v_O. For this, switches S_{ED} and S_E close at 0 µs to energize L_O from v_{ED} across a fixed 1.5-µs energizing time τ_{EN} and peak L_O's current to $i_{L(PK).ED}$. S_{ED} and S_E then open, and if v_O is below CP_O's upper threshold, S_{DE} and S_O close to drain L_O into v_O at 1.5 µs. This continues until comparator CP_{IOZ} senses when the voltage across S_O nears zero, which corresponds to L_O's current i_L reaching zero. All switches open at that point until the onset of f_{CLK}'s next switching cycle.

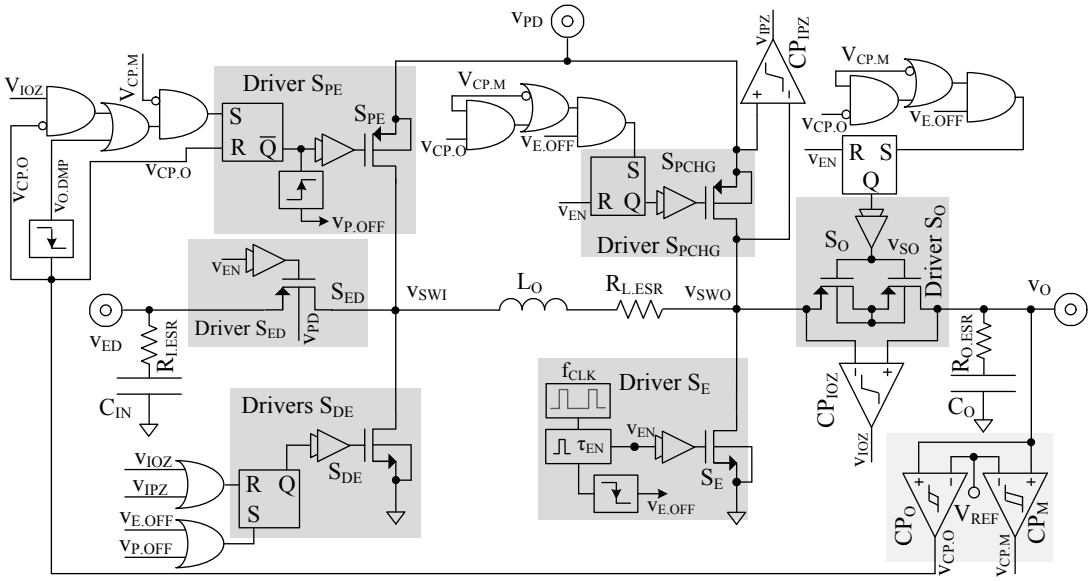
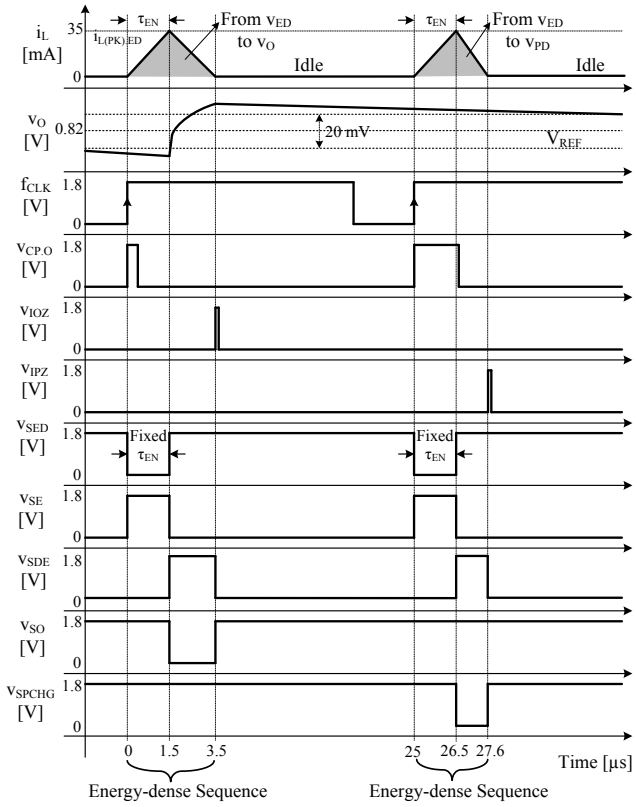
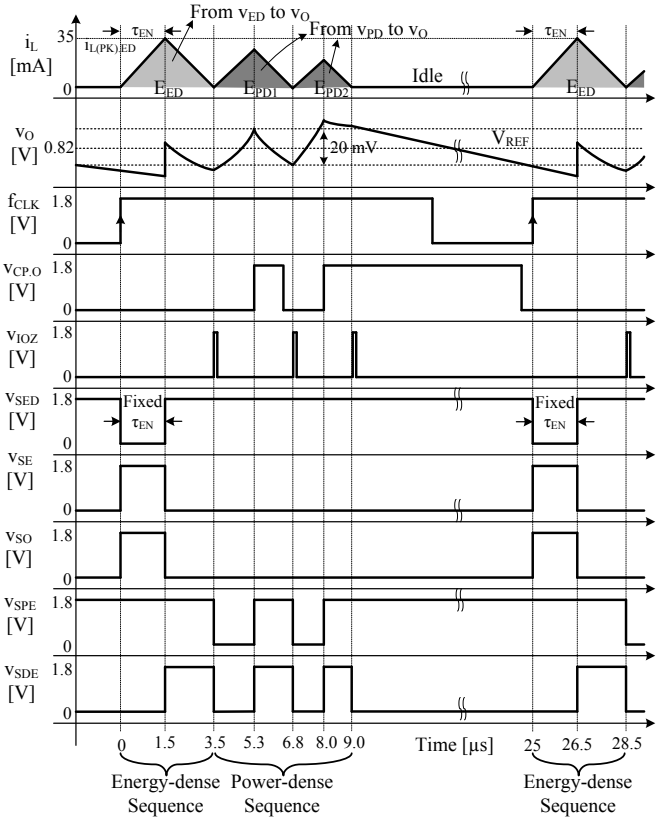


Fig. 2. Detailed system.


i_L [mA]
35
$i_{L(PK),ED}$
τ_{EN}
From v_{ED} to v_O
Idle
From v_{ED} to v_{PD}
v_O [V]
0.82
20 mV
V_{REF}
f_{CLK} [V]
$v_{CP,O}$ [V]
v_{IOZ} [V]
v_{IPZ} [V]
v_{SED} [V]
Fixed τ_{EN}
v_{SE} [V]
v_{SDE} [V]
v_{SO} [V]
v_{SPCHG} [V]
1.8
0
0 1.5 3.5
25 26.5 27.6
Time [µs]
Energy-dense Sequence
Energy-dense Sequence

(a)


From v_{ED} to v_O
From v_{PD} to v_O
i_L [mA]
35
$i_{L(PK),ED}$
τ_{EN}
Idle
E_{ED}
E_{PD1}
E_{PD2}
v_O [V]
0.82
20 mV
V_{REF}
f_{CLK} [V]
$v_{CP,O}$ [V]
v_{IOZ} [V]
v_{SED} [V]
Fixed τ_{EN}
v_{SE} [V]
v_{SO} [V]
v_{SPE} [V]
v_{SDE} [V]
1.8
0
0 1.5 3.5 5.3 6.8 8.0 9.0
25 26.5 28.5
Time [µs]
Energy-dense Sequence
Power-dense Sequence
Energy-dense Sequence

(b)

Fig. 3. Simulated waveforms in (a) light-load and (b) heavy-load modes.

If on the other hand v_O is above CP_O's upper threshold after L_O's τ_{EN}, S_{DE} and S_{PCHG} close to charge v_{PD} with L_O's energy. This is why v_O rises past 1.5 µs and continues to fall after 26.5 µs in Fig. 3a, because L_O drains into v_O at 1.5 µs and into v_{PD} at 26.5 µs. Here again, another comparator CP_{IPZ} senses when the voltage across S_{PCHG} nears zero to open-circuit L_O. To save energy, both CP_{IOZ} and CP_{IPZ} operate only when needed, after L_O's τ_{EN} until CP_{IOZ} or CP_{IPZ} trips to open S_{DE}. In other words, τ_{EN}'s falling edge enables CP_{IOZ} (or CP_{IPZ}) and CP_{IOZ}'s (or CP_{IPZ}'s) output disables CP_{IOZ} (or CP_{IPZ}). Irrespective of which output receives L_O's energy, L_O's τ_{EN} and f_{CLK} set v_{ED}'s average current I_{ED}, which across 1.5 µs and with 40 kHz is 1.5 mA.

Power-Dense Sequence: The system only resorts to the power-dense sequence in the heavy-load mode, when energy-dense power P_{ED} is insufficient to sustain load power P_{LD}. When this happens, the energy packet E_{ED} that L_O draws from v_{ED} at 0 µs in Fig. 3b and delivers to v_O at 1.5 µs does not raise v_O above CP_O's upper threshold. This commands the network to energize L_O from v_{PD} immediately after L_O drains E_{ED} into v_O at 3.5 µs. Therefore, with S_O already engaged at the end of the energy-dense sequence, S_{PE} closes to energize L_O from v_{PD} to v_O in buck-mode fashion until v_O rises above CP_O's upper threshold at 5.3 µs to trip CP_O. Afterwards, S_{PE} opens and S_{DE} closes to deplete L_O into v_O until CP_{IOZ} again senses that L_O's current nears zero. This way, L_O delivers the first power-dense energy packet E_{PD1} to v_O.

If v_O again drops below CP_O's lower threshold before f_{CLK} rises again, as Fig. 3b shows at 6.8 µs, L_O energizes from v_{PD} another time and delivers a second power-dense packet E_{PD2} to v_O. As with every sequence, the system waits for L_O's current i_L to be zero before re-energizing L_O, so L_O still operates in DCM. This way, the system delivers consecutive energy packets to v_O

until the packets satisfy the load. Once satisfied, v_O does not droop below CP_O's lower threshold and, as a result, all switches open and the system idles between 9.0 and 25 μs in Fig. 3b.

If v_O drops below CP_O's lower threshold while the system idles, before the onset of the next switching cycle, the system sends additional power-dense pockets until it again satisfies the load. The system then idles again until f_{CLK} rises to start another switching sequence. If the system cannot satisfy the load, f_{CLK} keeps the system from initiating additional power-dense packets when f_{CLK} starts another switching cycle. If this happens, the system is sourcing as much power as it can.

C. Feedback Control

Every clock cycle prompts L_O to draw an energy packet E_{ED} from v_{ED}. CP_O determines where to drain L_O (to v_O if below CP_O's lower threshold or to v_{PD} otherwise) and whether or not L_O should draw supplementary power from v_{PD} (if v_O remains low after v_{ED}'s E_{ED}). Comparator CP_M determines which mode to engage: supply v_O with power from both v_{ED} and v_{PD} if v_O falls below CP_M's lower threshold or supply v_O and recharge v_{PD} with power from v_{ED} otherwise. Therefore, when v_O falls below both lower thresholds, L_O draws energy from v_{ED} and v_{PD} to supply v_O. When v_O rises above CP_O's upper threshold, L_O stops drawing additional energy packets from v_{PD}, and when above CP_M's upper threshold, L_O recharges v_{PD} with part or all of v_{ED}'s E_{ED}. In other words, the system adjusts L_O's connectivity to regulate v_O about CP_O's and CP_M's reference V_{REF}.

Stability: Transfer inductor L_O and output capacitor C_O in dc–dc converters introduce two poles p_L and p_C to the feedback loop that regulates v_O, and if L_O disconnects from v_O at any time, also a right-half-plane zero z_{RHP}. Here, however, energizing and draining L_O from and to 0 A in DCM ensures the average voltage across L_O is zero across L_O's conduction time, so L_O's p_L disappears

[20]. Plus, fully draining L_O into v_O keeps feed-forward signals from inverting v_O, so z_{RHP} also disappears [20]. And because R_{ESR} limits how much current C_O can shunt, R_{ESR} eventually cancels the effects of p_C, which means R_{ESR} introduces a left-half-plane zero z_{LHP}. This system is therefore widely stable, because the power stage includes no other low-frequency poles than p_C and z_{LHP} recovers phase.

In this case, L_O supplies energy-dense packets E_{ED} from v_{ED} and supplementary power-dense packets E_{PD} from v_{PD} to v_O when heavily loaded. Because L_O draws the same energy E_{ED} from v_{ED} every switching cycle T_{SW}, v_{ED} supplies a fixed amount of charge across T_{SW}. This means, v_{ED} supplies a "constant" current to v_O, so neither v_{ED} nor its energy packets E_{ED} affect the feedback dynamics of the system.

In heavy-load mode, the system regulates v_O by adjusting the number of E_{PD} energy packets that L_O draws from v_{PD}. Several E_{PD}'s across T_{SW} amount to a variable current source i_l whose peak $i_{l(pk)}$ CP_O controls. If the voltage across R_{ESR} overwhelms that of C_O, v_O rises with L_O's i_l after each E_{PD} until i_l satisfies the current that produced Δv_O in the first place in $\Delta v_O/R_{ESR}$, so i_l rises until it peaks at v_o/R_{ESR} or $i_{l(pk)}$ in peak current-mode fashion [21].

In light-load mode, CP_O determines which output should receive v_{ED}'s energy packet E_{ED}. As such, L_O delivers E_{ED} to v_O whenever v_O falls below CP_O's lower threshold and to v_{PD} otherwise. In delivering one E_{ED} across T_{SW}, L_O supplies constant current. In other words, L_O is a current source that CP_O directs into either v_O or v_{PD}. This means, like before, that C_O establishes the dominant low-frequency pole of the system and its R_{ESR} introduces a phase-saving zero. Note v_{PD} is an unregulated low-impedance output that absorbs excess v_{ED} power.

D. Duty-Cycled Operation

Luckily, not all system components must operate continuously across T_{SW}. Comparators CP_{IOZ} and CP_{IPZ}, for example, need to sense i_L only while L_O de-energizes through S_O to v_O or S_{PCHG} to v_{PD}. Therefore, the system enables CP_{IOZ} or CP_{IPZ} at the end of the energizing period τ_{EN} and disables whichever is on after CP_{IOZ} or CP_{IPZ} in Fig. 2 trips. This way, the system reduces the energy that CP_{IOZ} and CP_{IPZ} consume by 90%. Unfortunately, because load dumps are unpredictable, the system cannot similarly duty-cycle CP_O.

E. Feedback Hysteretic Comparators CP_O and CP_M

Fig. 4 shows the push–pull topology that implements output and mode comparators CP_O and CP_M. Load mirrors M_{M1}–M_{M2} and M_{M3}–M_{M4} implement a positive feedback loop that establishes 20 mV of hysteresis for CP_O and 50 mV for CP_M. Mirror currents then fold and meet at v_{O1} to drive inverter M_{I1}–M_{I2} and output CP_O's $v_{CP.O}$ and CP_M's $v_{CP.M}$ from Fig. 2.

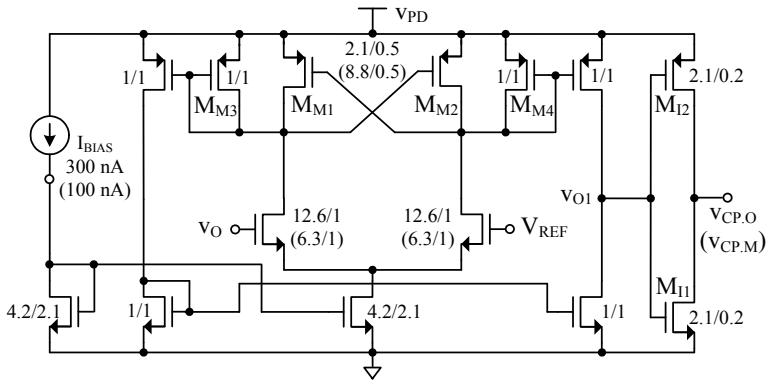


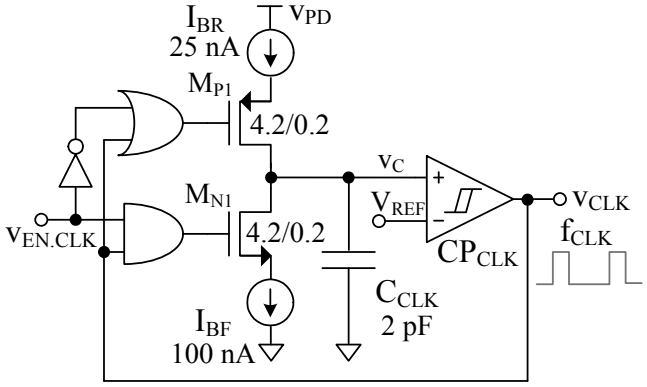
Fig. 4. Feedback comparators CP_O (and CP_M) biased with 300 nA (and 100 nA).

F. Clock and Pulse Generators

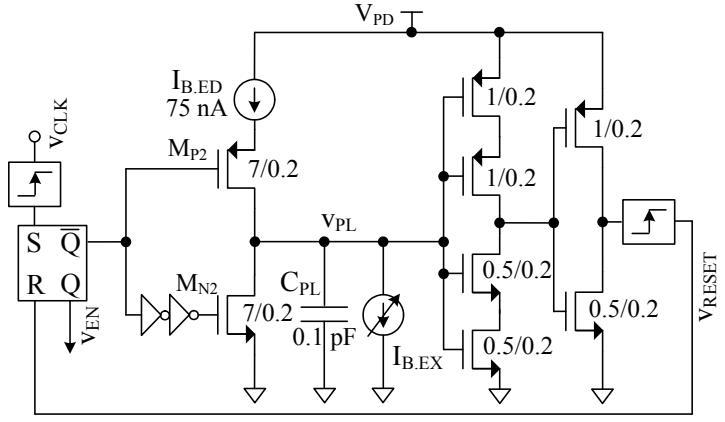
Once enabled by $v_{EN.CLK}$, the clock and pulse generators in Fig. 5 start and set L_O's energizing time τ_{EN} in Fig. 2. For this, bias currents I_{BR} and I_{BF} in Fig. 5a charge and discharge capacitor C_{CLK}. So when comparator CP_{CLK} closes M_{P1}, I_{BR} charges C_{CLK} until C_{CLK}'s voltage v_C crosses

CP_{CLK}'s upper threshold, at which point CP_{CLK} trips to open M_{P1} and close M_{N1}. With M_{N1} closed, I_{BF} discharges C_{CLK} until v_C crosses CP_{CLK}'s lower threshold, which prompts CP_{CLK} to open M_{N1} and close M_{P2}, and as a result, start another sequence. v_C therefore ramps up and down and CP_{CLK}'s output v_{CLK} alternates states at 40 kHz.

With every rising transition in v_{CLK}, M_{P2} in Fig. 5b closes to steer $I_{B.ED}$ into capacitor C_{PL}. C_{PL}'s voltage v_{PL} therefore rises until the inverter v_{PL} drives trips and prompts the SR latch to open M_{P2} and close M_{N2}, the result of which is to pull v_{PL} quickly to ground. v_{PL} then remains low until v_{CLK} rises to open M_{N2} and again close M_{P2}. In other words, v_{PL} slews up and v_{EN} pulses across a short fraction of v_{CLK}'s period t_{CLK}. Since $I_{B.EX}$ sinks some of $I_{B.ED}$, adjusting $I_{B.EX}$ programs v_{EN}'s pulse width τ_{EN}.



(a)



(b)

Fig. 5. (a) Clock and (b) pulse generators.

V. Power Losses

The system consumes conduction, gate-drive, and quiescent power. Power switches in the conduction path dissipate 310 μW of Ohmic conduction power when supplying 2 mA to the load. Of those, as Table I shows, output switch S_O consumes 280 μW. Parasitic gate capacitances also require 16 μW and bias and comparators in the system another 16.1 μW. Considering S_O loses more than 50% of all the 517 μW lost, increasing S_O's width–length ratio by 5× would have saved about 200 μW at the expense of increased silicon area.

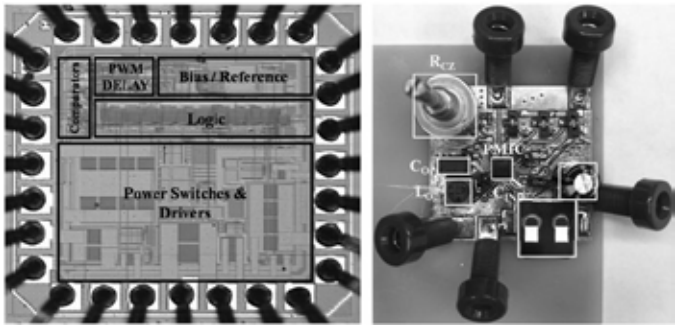
Table I. Simulated Power Losses

Category	Block	Power Losses
Conduction	Power Switches	310 μW (280 μW in S_O)
	L_O's $R_{L.ESR}$: 4 Ω	170 μW
	C_O's R_{ESR}: 0.1 Ω	2.9 μW
Gate Drive	Power Switches	16 μW
	Logic Gates	1.4 μW
Quiescent Losses	Reference/Bias	6.1 μW
	Clock/Delay Gen.	3.8 μW
	CP_{IOZ} and CP_{IPZ}	7.0 μW
	CP_O and CP_M	3.0 μW
Total Losses		**517 μW when I_{LD} is 2 mA**

VI. Measured Results

The 840×840-μm^2 0.18-μm CMOS die photographed in Fig. 6a and two-layer board in Fig. 6b implement the system proposed in Figs. 1–2. An 11×11×5-mm^3 600-mAh zinc-air cell that generates about 470 Wh's per 1 kg from ambient air together with a 2×1×1-mm^3 1-μF tantalum capacitor comprise the energy-dense source and an 8×8×12-mm^3 1-F super capacitor charged to 1.8 V the power-dense counterpart. Here, for testability, the zinc-air cell emulates a DMFC and the super capacitor a thin-film lithium ion. The power stage uses a 6×6×2-mm^3 50-μH inductor

with 4 Ω of equivalent series resistance (ESR) to supply power and a 7×4×1-mm^3 1-μF capacitor with 0.1 Ω of ESR to suppress ripples in the output v_O. The clock frequency of the system is 40 kHz.



(a) (b)

Fig. 6. Prototyped (a) 0.18-μm CMOS die and (b) printed circuit board.

A. Regulation Performance

When the load pulls 2 mW, the converter is in the heavy-load mode and delivers about 1.5 mW from the energy-dense source with one energy packet E_{ED}, as Fig. 7a shows, and 0.5 mW from the power-dense source with two energy packets E_{PD1} and E_{PD2}. L_O's inductor current peaks at different points when delivering E_{PD1} and E_{PD2} because v_O's steady-state point rises with E_{PD}'s and CP_{IOZ}'s input-referred offset keeps L_O from fully de-energizing before the subsequent cycle. As a result, E_{PD1} differs slightly from E_{PD2}. Still, v_O ripples 20 mV about CP_O's V_{REF}, which is 0.80 V. In addition, when lightly loaded, as Fig. 7b depicts, the system delivers ten of eleven packets of energy to the rechargeable power-dense battery and v_O ripples roughly 5 mV about 0.823 V.

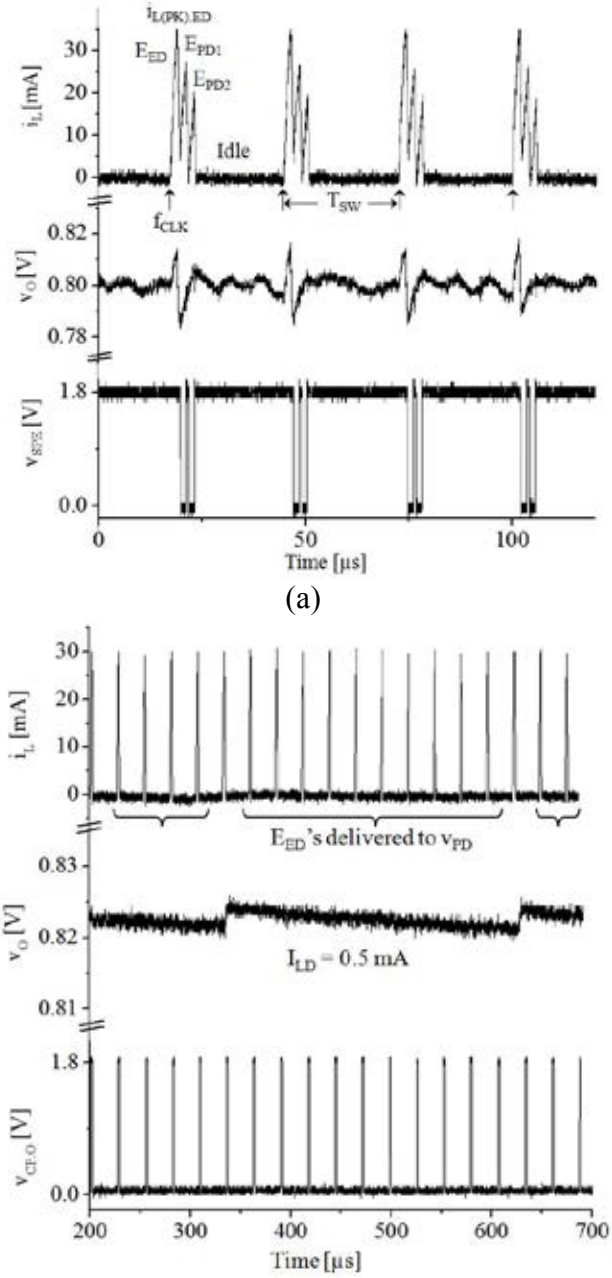
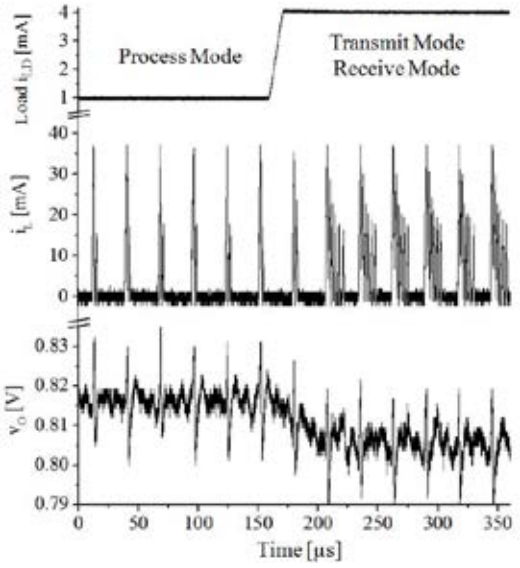


Fig. 7. Measured current and voltage waveforms in (a) heavy-load and (b) light-load modes.

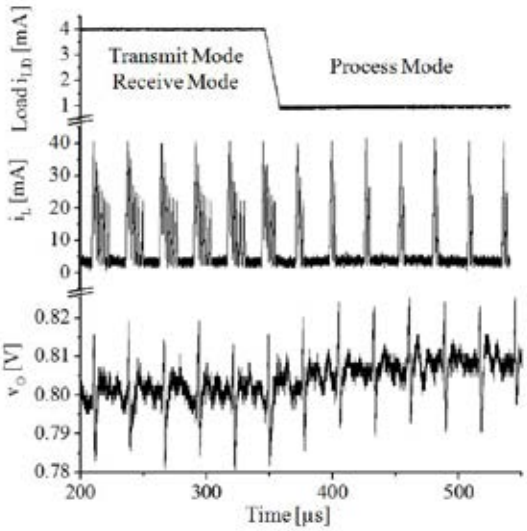
The output includes perceptible noise with respect to its ripple mainly because the hysteretic window is small at 20 mV. With such tight hysteresis, noise in the board easily couples into the output, which can not only trigger inadvertent transitions but also affect other components in the

system like the reference and bias generator. With over 30 mA of peak current, C_O's R_{ESR} of 0.1 Ω and board resistances also contribute over 3 mV of noise into the 20-mV window.

In response to the rising and falling 1–4-mA load dumps of Fig. 8, v_O shifts 12 mV or 1.5% between 0.803 and 0.815 V. Under hysteretic control, the converter responds within one clock cycle and adjusts the number of energy packets it delivers from v_{PD} automatically according to the load. The steady-state shift in v_O is load regulation, which is the result of finite gain across the feedback loop.



(a)



(b)

Fig. 8. (a) Measured responses to 1–4-mA and (b) 4–1-mA load dumps.

B. Power-Conversion Efficiency

Power-conversion efficiency η_C is how much input power P_{IN} from v_{ED} and v_{PD} reaches v_O as P_O:

$$\eta_C \equiv \frac{P_O}{P_{IN}} = \frac{P_O}{P_{ED} + P_{PD}}, \tag{1}$$

where P_{ED} and P_{PD} refer to the power that v_{ED} and v_{PD} supply. In this case, η_C peaks to 73% when supplying 1 mA to the load, as Fig. 9 demonstrates. Overall, η_C remains above 65% across the 0.5–8-mA load range. η_C does not rise above 73% because, as Table I shows, output switch S_O and L_O's $R_{L.ESR}$ consume substantial power. In fact, at the expense of silicon area, increasing S_O's width–length ratio would raise η_C. Similarly, reducing $R_{L.ESR}$ would also raise η_C, but at the expense of volume because L_O would have to be physically larger. In other words, larger systems outperform their miniaturized counterparts.

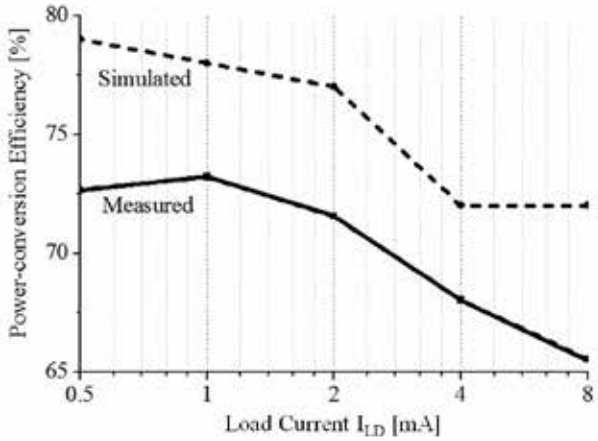


Fig. 9. Power-conversion efficiency across load current.

Generally, measurements were roughly 5% to 8% lower than simulations predicted. This discrepancy is the result of several factors. For one, basic CMOS models do not emulate well the

parasitic series resistances and substrate currents that power transistors typically incorporate. Secondly, the printed circuit board introduces parasitic series resistances to ground, the output, and both input sources that, again, simulations do not account well. In this respect, a multi-layer board can expand the supply and ground planes and reduce their resistive effects.

Table II. Performance Summary and Comparison against the State of the Art

	[16] JSSC '09	[17] ISSCC '13	[18] TCAS II '12	[19] TCAS II '09	[22] ISSCC '14	This work
Topology	SIMO Buck–Boost	SIDITO Buck–Boost	SIMO Boost	MO Buck–Boost	SIDIDO Buck–Boost	SIDIDO Buck–Boost
Efficiency at 0.1 mW	80%	83%	60%	80%	70%	72%
Peak Efficiency	93%	83%	81%	83%	83%	73%
Output Voltage	1.25	1, 1.8, 3	2.5, 3.0	2 ~ 12	0.8	0.8
Load Dump	25 mV	–	50 mV	20 mV	40 mV	30 mV
Output Capacitor	33 µF	–	10 µF	10 µF	1 µF	1 µF
Load Range	0 – 125 mW	0 – 10 mW	0 – 150 mW	0 – 450 mW	0 – 8 mW	0 – 8 mW
Inductor	10 µH	–	1 µH	4.7 µH x 2	50 µH	50 µH
Process Technology	0.25 µm	0.18 µm	0.5 µm	0.5 µm	0.18 µm	0.18 µm
Source required to sustain the 0.01–4-mW load in Sec. I	430-mg DMFC Or 320-mg Li Ion	480-mg DMFC Or 310-mg Li Ion	490-mg DMFC Or 430-mg Li Ion	480-mg DMFC Or 330-mg Li Ion	74.5-mg DMFC + 24.1-mg Li Ion Tot.: 98.6 mg	73-mg DMFC + 27-mg Li Ion Tot.: 100 mg
Response Time	< 10 clock cycles*	N/A (Open-loop)	< 12.5 clock cycles	< 10 clock cycles*	< 8 clock cycles	< 2 clock cycles
Switching Frequency	660 kHz	10/20 kHz	500 kHz	1 MHz	40 kHz	40 kHz

C. Performance Comparison

Table II summarizes the performance of the prototyped single-inductor multiple-input multiple-output (SIMIMO) charger–supply and those of similar, though not exactly alike state-of-the-art systems. The driving advantage of the prototyped system over the state of the art is the feedback intelligence with which it determines when to derive power from a power-dense source and when to steer excess energy from an energy-dense source into the rechargeable power-dense battery. The ultimate benefit here is the space savings that results when supplying a system whose peak power is substantially above its average, which is typical in wireless microsensors.

In the case of the load described in Section I, for example, the system mostly idles at 10 μW and peaks to 4 mW to dissipate 72 μW on average. For this, first consider that the weight W_{FC} of DMFC required to supply the power $P_{IN(PK)}$ that a converter with a power-conversion efficiency $\eta_{C(PK)}$ demands when delivering peak output power $P_{O(PK)}$ depends on the DMFC's power density PD_{FC}:

$$W_{FC} = \frac{P_{IN(PK)}}{PD_{FC}} = \frac{P_{O(PK)}}{\eta_{C(PK)} PD_{FC}}. \tag{2}$$

Similarly, the energy density ED_{LI} of a lithium ion determines the weight W_{LI} of the battery required to sustain the power $P_{IN(AVG)}$ that a converter with a power-conversion efficiency $\eta_{C(AVG)}$ demands when outputting average output power $P_{O(AVG)}$ for one month is

$$W_{LI} = \frac{P_{IN(AVG)} t_{1\text{-MONTH}}}{ED_{LI}} = \frac{P_{O(AVG)} t_{1\text{-MONTH}}}{\eta_{C(AVG)} ED_{LI}}. \tag{3}$$

So to sustain the aforementioned load, the SIMO buck–boost converter in [16] requires a 430-mg DMFC to supply the 4-mW peak load or a 320-mg lithium ion to sustain 72 μW for one month. [17]–[19] must similarly oversize the DMFC to 480–490 mg to supply the 4-mW peak or the lithium ion to 310–430 mg to sustain 72 μW for one month. Since the system presented here draws average power from the energy-dense source and burst power from the power-dense counterpart, W_{FC} depends on $P_{O(AVG)}$ and W_{LI} on $P_{O(PK)}$:

$$W_{FC} = \frac{P_{IN(AVG)} t_{1\text{-MONTH}}}{ED_{FC}} = \frac{P_{O(AVG)} t_{1\text{-MONTH}}}{\eta_{C(AVG)} ED_{FC}}, \tag{4}$$

$$W_{LI} = \frac{P_{IN(PK)}}{PD_{LI}} = \frac{P_{O(PK)}}{\eta_{C(PK)} PD_{LI}}, \tag{5}$$

and

$$W_{TOT} = W_{FC} + W_{LI}. \tag{6}$$

As a result, the prototyped converter requires a 27-mg lithium ion to supply 4-mW peaks and a 73-mg DMFC to sustain 72 μW for one month. When combined, the proposed technology requires 100 mg, which is 68% less weight than what the lightest state-of-the-art counterpart requires.

Although largely unexplained in such a short format, [22] incorporates similar dual-source intelligence to this work, except [22] only draws one energy packet per sequence from the power-dense source and controls it via pulse-width modulation (PWM). With only one packet, switching losses are lower than in this work and high-load efficiency is therefore higher. This is why [22]'s weight is slightly lower at 98.6 mg than this work's 100 mg. Where this technology shines over [22] is in speed, because the nested hysteretic loops that feedback comparators CP_O and CP_M comprise react to load dumps as soon as they detect changes in v_O. As a result, the system responds within one or two clock cycles, as opposed to the more than eight clock cycles that PWM and other schemes require [23]. In other words, this system suffers considerably less load-dump variations than competing converters. And the system remains in regulation without the aid of off-chip compensation components as long as the voltage across the equivalent series resistance (ESR) of the output capacitor C_O overwhelms that of C_O [21]. This means, this solution can be fast and compact, both of which are critical in micro-scale applications whose loads vary vastly across time.

VII. Conclusions

The hysteretic dual-source single-inductor 0.18-μm CMOS switching charger–supply fabricated and presented here supplies 0.5–8 mA and regulates the output to 0.8 V within 1.5% with peak and average efficiencies of 73% and 70%. When heavily loaded, the system draws constant power from an energy-dense source and supplementary peak power from a rechargeable power-

dense battery. Otherwise, when lightly loaded, the system recharges the battery with excess power from the energy-dense source. This way, when loaded with a microsystem that idles at 10 μW and peaks to 4 mW, the system requires sources that weigh 68% less than those of the state of the art. The dual-source system also responds to load dumps within one switching cycle by redirecting power from the energy-dense source and adjusting the number of energy packets the power-dense battery delivers. The charger–supply is fast and widely stable without off-chip compensation components because the voltage across C_O's equivalent series resistance (ESR) dominates over that of C_O. While higher ESRs reduce efficiency and raise noise, responding quickly to load dumps is imperative in miniaturized applications. Microsensors, to cite a driving example, which cannot accommodate large capacitors and inductors, suffer from vast load dumps when they wake and transmit data wirelessly. In these cases, response time and overall size are paramount.

ACKNOWLEDGMENT

The authors thank Paul Emerson, Dr. Pooya Forghani, and Texas Instruments for their support and for fabricating and packaging the prototyped IC.

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