A Fast and Reliable Top-Level Simulation Strategy for Mixed-Signal ICs and its Application to DC–DC Converter Circuits

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Abstract – Top-level, transient, transistor-based simulations are a critical step in the product-development cycle of mixed-signal integrated circuits (ICs). These simulations are normally performed just before fabrication and unfortunately impose cumbersome bottlenecks in the design flow. Verification is an iterative process by nature, whereby each problem found requires another simulation to ensure a proper fix is in place, and because of the complexity of a large system, minor errors can cost days, increasing design time and time-to-market. This paper proposes a top-level transistor-based simulation strategy with minimal time overhead. The strategy is to start with a quick, all macro-model system simulation and gradually substitute one transistor-level sub-block at a time for each additional run. For optimal results, less computationally intensive blocks, which can be determined from a proposed set of screening simulations, are replaced first. The proposed strategy was tested and applied to a buck, current-mode switching regulator, and the results show that simulation overhead is least for linear analog functions (e.g., op-amps) and worst for high speed nonlinear circuits (e.g., signal generators). Nonlinear and bi-stable analog blocks like bandgap references take more time to simulate than op-amps and less than low frequency digital functions like power-on-reset, which in turn are less intensive than ramp and pulse generators.

I. INTRODUCTION

A set of top-level transient simulations is usually necessary to verify the functionality of mixed-signal integrated circuits (ICs) just before fabrication. For highest fault coverage, all transistor-level simulations should be performed. Unfortunately, the simulation time for a complex system using all transistor-level models is many times prohibitively long, each simulation taking hours to days to complete. A switching dc-dc regulator constitutes one such mixed-signal example, with complex analog and high power switching digital circuits embedded onto a single substrate. The resulting simulation scenario demands the simulator to simultaneously resolve a vast number of equations at each step of a transient simulation run, which typically exceeds 1,000 switching cycles for start-up alone and incurs in the order of several hours to days of CPU time. As a result, considering the competitive time-to-market nature of the semiconductor industry, most designers concentrate their efforts on exhaustive, transistor-level, sub-block designs and opt for simple top-level simulations using a combination of transistor-based and behavioral models to *partially* verify inter-block connectivity and basic system functionality. That is to say, designers sacrifice top-level verification for time-to-market, which is not ideal and sometimes

costly. Forfeiting better top-level simulations may mask interface and parasitic problems like inadvertent supply-to-ground resistive links, which translate to leakage currents. This problem is exacerbated with the growing demand for higher integration of system-on-chip (SoC) solutions. Sacrificing verification is difficult to justify when high yields are necessary to compete and turn a profit, which is why the need for quicker transistor-based top-level simulations is paramount.

The approach of state-of-the-art simulations for mixed-signal systems is to develop better behavioral models and partitioning circuits to analog and digital functional blocks [1-9]. The models, unfortunately, lack the electrical details of parasitic junction diodes and diffusion resistors present in silicon-based electronics, the effects of which are seen during top-level system operation (e.g., leakage currents, unexpected loading events, oscillations, etc.). Literature on simulating specific types of circuits, like dc-dc switching converters [10-15], also focus on developing simplifying models, which are extremely useful in the system design phase, but relatively ineffective in the verification phase, where transistor-based models are necessary to identify parasitic electrical faults in the system.

This paper proposes a top-level transient simulation strategy for mixed-signal circuits to minimize the verification time, or equivalently, maximize the fault coverage by using as much transistor-level models as possible in top-level simulations, while meeting verification-time deadlines. The proposed solution is to identify and delay replacement of transistor-based models of computationally extensive circuits, detecting most of the errors first, through relatively quick simulations. The rest of the paper is organized as follows. In Section II, a typical mixed-signal circuit and its respective macro-models are reviewed and used as a case study for the foregoing verification strategy. The proposed replacement strategy and screening set of simulations are then introduced in Section III. In Section IV, top-level simulations of a pulse-width modulated (PWM) current-mode buck (step-down) dc-dc converter are performed and evaluated to gauge the effectiveness of the proposed strategy, the result of which is an optimal replacement order that, once determined, eliminates the need for screening simulations. Conclusions are ultimately drawn in Section V.

II. SWITCHING DC-DC CONVERTERS

A. Operation

Switching regulators are widely popular in consumer and military applications, especially the portable market because they convert variable voltages into stable, predictable, and suitable supplies without incurring significant power losses, and therefore increasing the battery life and requiring less heat sinks and board real estate [16-17]. The circuit accomplishes this by periodically storing magnetic energy into an inductor and later relinquishing it almost losslessly to the load and relevant output capacitor. The

energy charge and transfer cycles of the scheme not only force the circuit to conduct high currents but also to switch periodically. This switching is complicated by the fact that the duty cycle must be regulated by a feedback control loop to ensure the output voltage is reliable and controlled.

Figure 1 illustrates the schematic of a typical pulse-width modulated (PWM) current-mode buck (step down) switching dc-dc converter. The power train, which is comprised of high- and low-side power switches M_H and M_L, inductor L, and capacitor C, is responsible for storing and transferring energy from input supply V_{in} to load I_L. Error amplifier EA, comparator CMP, signal generator, bandgap reference voltage, driver and dead time control (DTC), and current-sensing blocks constitute the analog control loop responsible for regulating the output voltage to a stable and predictable value [16-17]. In practice, power-on-reset, start-up, protection, and mode-changing circuits are also included for safety, reliability, and performance.

By alternately switching high- and low-side power devices M_H and M_L on and off, V_{ph} is switched from input supply V_{in} to ground, the average of which is reflected at the output as a result of the LC filter properties. Output voltage V_o is therefore the average of V_{ph}, which is in turn a function of how often high-side switch M_H is on, in other words, its duty-cycle D and V_{in} ($V_{out} = V_{in}D$). Modulating duty-cycle D to regulate V_o is accomplished by comparing V_o and the reference via the amplifier, consequently generating slow-moving control signal EA_{out}, which ultimately sets duty-cycle D when compared against the inductor current. Resistors R_a, R_b, and R_c and capacitor C_z comprise the loop-compensating filter. The driver and dead-time control circuit is used to rapidly turn on and off large power transistors, while simultaneously avoiding momentary shoot-through events (i.e., high- and low-side switching shorts) [16-17]. As can be appreciated, the analog and switching complexities of this system are vast, when considering every sub-block is designed with numerous transistors, each of which introduce several nodes, parasitic elements, and non-linear semiconductor current-voltage relationships.

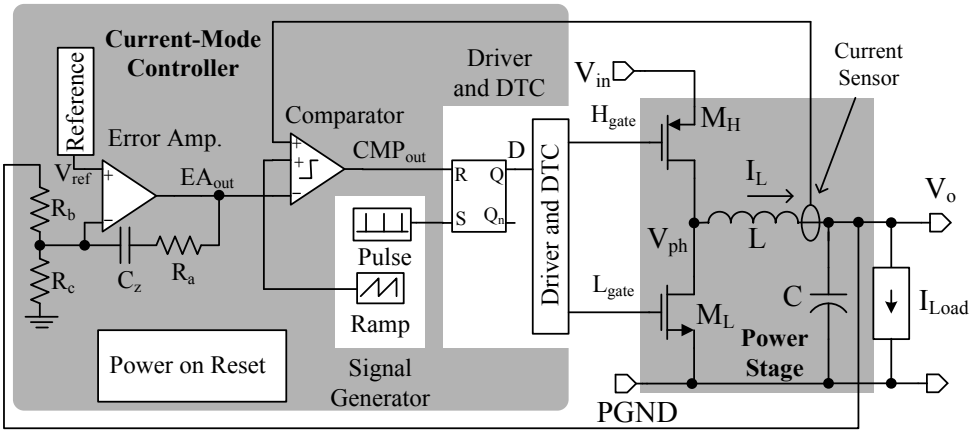

Figure 1 A current-mode buck (step-down) pulse-width modulated (PWM) switching regulator circuit.

B. Macro Models

Accurate yet simple behavioral and functional models are not only important and useful in the system definition and design phases of mixed-signal circuits but also in the proposed top-level verification strategy. These macro models are typically implemented with a combination of high-level hardware description languages (e.g., VerilogA) [18-20] and ideal electrical SPICE components (e.g., independent and dependent voltage and current sources) [18, 21] under a Cadence platform, the same platform used for IC design, transistor-level simulations, and physical layout, which is built to seamlessly interface behavioral-based macro-model and Spice-level signals via Spectre, a built-in Cadence simulator. For the same reason, sharing the platform is also important for seamless macro-to-transistor level transitions. And to take full advantage of this, the top-level symbol of the macro-model should be designed to mimic that of the transistor-level block to minimize interconnectivity changes and maintain the integrity of the top-level schematic. Additionally, macro models should be comprehensive, having all input-output signals and enable-disable pins, to ensure the full system connectivity is truly tested.

The macro models predict the DC (power efficiency and load and line regulation performance) and transient response of the switching regulator almost as accurately as the all transistor-level models. However, they do not verify other IC-related specifications like leakage, quiescent, and transient supply currents, all of which are sensitive to various parasitic effects present in the system, like inter-block loading and short-circuit events, which is the inspiration behind the use of transistor-based models for the verification process in the first place. Below is a description of the models used in this work, which were verified and validated against their all transistor-level counterpart with functional and parametric Cadence-environment simulations.

Power Train

In the case of a step-down DC-DC converter, as shown in Figure 1, the power train consists of high-side and low-side power switches M_H and M_L (and related parasitic devices), inductor L, and capacitor C, and for higher accuracy, the equivalent series resistances (ESRs) of the power inductor and output capacitor. As it turns out, many important supply specification parameters, such as power efficiency, load and line regulation, output voltage ripple, and transient load-dump response, are strongly dependent on these components and how they perform. Luckily, this section is only comprised of six devices and approximately eight nodes (including ESRs), and is therefore responsible for only a small fraction of the total simulation time. As a result, given the critical nature of the block and its low overall impact on simulation time, the circuit is not macro-modeled but used as is, in its all transistor-level configuration.

Error Amplifier and Comparator

Figure 2 illustrates the macro model used for both amplifiers and comparators, which captures key specification parameters like gain, bandwidth, and input and output common-mode ranges. Voltage buffer "buf" decouples and isolates the input impedance section comprised of R_{in} and C_{in} from the input common-mode limiting section, and R_{lim} limits the current into the circuit. This buffer can take the form of an ideal voltage-controlled voltage source, or programmed as a Verilog-AMS component. Ideal Spice diodes D_1 through D_8 are used to clamp the input and output signals to within specified limits (e.g., between $V_{ss}+V_2$ and $V_{dd}-V_1$ and $V_{ss}+V_4$ and $V_{dd}-V_3$) and internal nodes within the supply rails to prevent internal capacitors from charging and discharging to unrealistic values (e.g., ±1,000 V), which would unnecessarily delay the circuit (this last feature is not included in conventional macro models [21] but included here for accuracy). The amplifier gain and bandwidth are set by $g_{m1}R_1$ and $1/R_1C_1$, respectively, and the output pole by r_o and the circuit's loading capacitance, which is external to the macro model. In many cases, the amplifier's output is pinned out of the chip and its loading capacitor is often not well-defined so it is best to consider worst-case values and specify r_o accordingly. When used as a comparator, the delay time (t_d) is determined by time-constant R_1C_1 and C_1 is therefore defined to satisfy the following expression [21]:

$$t_d = 2.2R_1C_1. \tag{1}$$

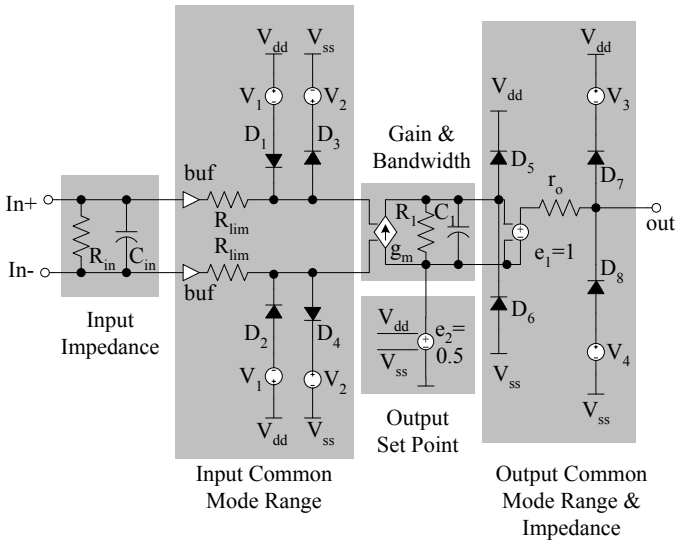

Figure 2. Proposed amplifier and comparator macro model.

Digital Components

RS-latch, power-on-reset, and driver and dead-time control circuits are among some of the key digital circuits used in a switching regulator. The power-on-reset block, a good portion of which amounts to a start-up state machine, is usually the most complicated section, consisting of several flip-flops and gates, whereas driver and dead-time control circuits consist of inverters, gates, and delay elements. Verilog-AMS within the Cadence IC design environment is used to macro-model these circuits [19-21]. As an example, Figure 3 shows the code used to implement the driver and dead-time control (DTC) circuit, where dead time is defined with an absolute delay function and drive capabilities with rise- and fall-time delays (t_r and t_f).

```
Module DTCv(Hgate, Lgate, vddd, vssd, in);
output Hgate, Lgate;
input in, vddd, vssd;
electrical Hgate, Lgate, in, vddd, vssd;
real inL, xn, y;
real t1, t2;
parameter real vtran;
parameter td = 5n, tr = 5n, tf = 5n, tdead=20n;
analog begin
        if (V(in) > vtran) inL = 1; else inL =  0;
        t1 = absdelay (xn, tdead);
        t2 = absdelay (y, tdead);
        xn = !(inL&&t2);
        y = !(!inL &&t1);
        V(Hgate) <+ transition (y ? V(vddd) : V(vssd), td, tr, tf);
        V(Lgate) <+ transition (xn ? V(vssd) : V(vddd), td, tr, tf);
end
end module
```

Figure 3. Driver and dead-time Verilog-AMS macro model code.

Bias and Signal Generators

The reference block, which consists of a bandgap reference circuit loaded with a buffer-resistor ladder combination to generate various bias voltages and currents, is modeled with independent DC voltage and current sources and impedance defining resistances, conforming to Norton- and Thevenin-equivalent circuits. The signal generator block, which synthesizes various ramp, pulse, and clocking signals, is modeled with independent, time-defined Spice voltage sources, such as PWL and the like. Some Verilog-AMS blocks are added to model additional features such as enable/disable functions. For example, the voltage reference operates only when enabled by the power-on-reset block, and it returns an *OK* signal to the power-on-reset block when working within acceptable limits (i.e., when fully operational). All these signals are interfaced within the behavioral models and through the Cadence environment.

The intent of the macro-modeled blocks is to verify system functionality (i.e., architecture), identify how key block-level performance parameters affect the system, and ascertain permissible ranges for them. The macro models only emulate those parameters that are fundamental and vital to a particular function, such as gain, bandwidth, etc. are for an amplifier, and can predict the effects of these parameters on the system accurately. The effects of circuit details not included in the model will not necessarily appear in macro-model simulations, which is why all-transistor-level simulations are necessary before tape-out. Increasing the accuracy of the model, however, improves its ability to predict performance and system sensitivities, but with diminishing benefits and ease, the balance of which is ultimately decided by the designer based on experience.

III. TOP-LEVEL VERIFICATION FLOW

A. Design flow

Design flow typically starts after a market or research segment and application have been identified and defined, establishing specifications for a target system. A suitable top-level system architecture is then designed and simulated using simple behaviorally based macro models. The sensitivity of the system to a spread of values, and the stability of the system under various L-C combinations is of particular importance, is best verified and characterized at this stage, with an all macro-model simulation, during which specifications for each macro model (i.e., sub-block) are ascertained. This part of the process constitutes the *system design* phase, illustrated in Figure 4. At this point, transistor-level design, simulation, and verification of each sub-block against its specific target specifications are performed, both nominally and over process corners and temperature extremes. Since the simulations are relatively short, given the relatively low number of transistors used and the computing power of state-of-the-art computers, quasi-exhaustive verification is often achieved. Finally, before having the design fabricated (i.e., before *tape-out*), all the sub-blocks are interconnected and simulated together, which constitutes the transistor-based, top-level system. Verification is by nature an iterative process, however, whereby each problem found requires another simulation to ensure a proper fix is in place, and because of the complexity of a large system, minor errors can cost days, increasing design time and time-to-market.

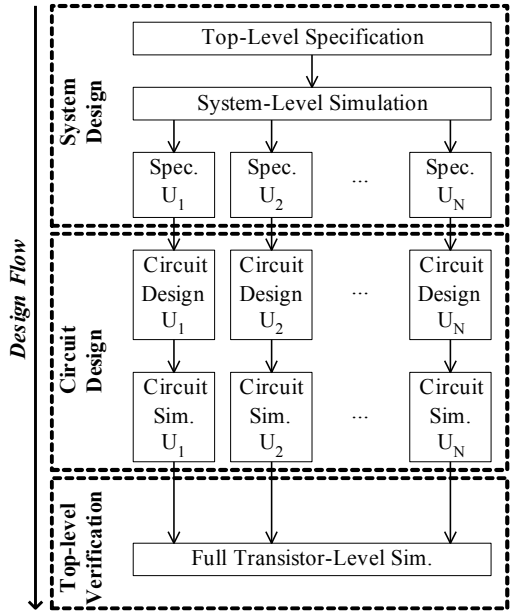

Figure 4 Traditional design flow of integrated electronic systems.

B. Proposed top-level simulation plan

The proposed strategy is to use the all behaviorally based macro-model simulation used in the system-design phase and selectively replace each sub-block, one at a time, with its appropriate transistor-level circuit in the final verification phase, as shown in Figure 5, gradually transitioning from an all macro-model to a full transistor-level simulation. The sub-blocks that are first substituted must be the least time-consuming circuits to simulate, consequently fully debugging and verifying connectivity and the system performance parameters associated with that specific sub-block. Substituting the next least time-consuming sub-block, and keeping the first one in place, accomplishes similar goals for the new block. The process continues until all of the blocks are fully replaced with their circuit-level models. A set of screening simulations are therefore developed to determine the optimal replacement order.

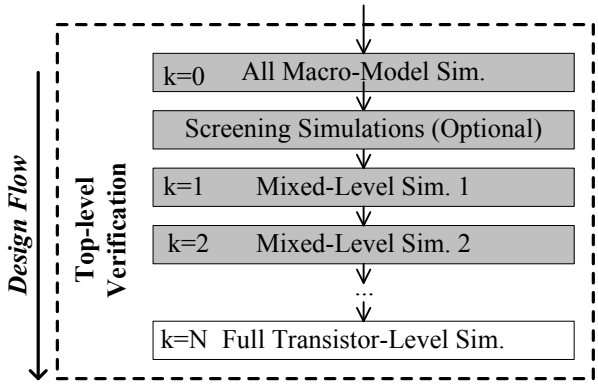

Figure 5 Proposed top-level verification sequence of complex, mixed-signal systems.

The expected value of the simulation time of the proposed strategy, excluding the optional screening simulations, which are non-recurring in nature, is the summation of the various intermediate simulations,

$$E\left(t_{Total\_Proposed}\right) = \sum_{k=0}^{N} \overline{m}_k t_{sim-k}, \tag{2}$$

where $\overline{m}_k$ is the average number of iterations a circuit is simulated at each given step and t_{sim-k} is the simulation time of the k^{th} verification step in the top-level verification phase. The two extreme steps correspond to the all behaviorally based macro-model and the all transistor-level simulations with 0 and N for k, respectively. The expected value for the simulation time of the conventional approach (i.e., a single, all transistor-based top-level simulation) is, on the other hand,

$$E\left(t_{Total\_Conv.}\right) = \overline{L} t_{sim-N}, \tag{3}$$

where $\overline{L}$ is the average number of iterations the top-level circuit is simulated and t_{sim-N} is the simulation time of a single, all transistor-level run. The basic goal of the proposed strategy is for the expected value of the simulation time to be equal to or shorter than in the conventional approach, considering that iterations are necessary to identify problems and verify solutions. The premise here is that the number of iterations of the most time-consuming all-transistor circuit with the proposed strategy is low enough and its overall fault coverage large enough to merit its use,

$$\overline{m}_N < \overline{L}. \tag{4}$$

Most errors, especially the ones due to connectivity, are typically found early in quick simulations since $t_{sim-0} < t_{sim-1} < ... < t_{sim-N}$, effectively decreasing the number of iterations required to simulate each subsequent step in the process (i.e., $\overline{m}_0 > \overline{m}_1 > ... > \overline{m}_N$), the net result of which is a reduction in the iterations required to simulate the costly all-transistor circuit (Figure 6).

In practice, each sub-block in a system affects full transistor-level simulations differently and only a select few tend to be mostly responsible for prolonged computational times [18]. Therefore, verification time is minimized if less computationally intensive blocks are replaced earlier in the proposed process. Thus, the optimal replacement strategy is one where each subsequent mixed-signal simulation time t_{sim-i} is the shortest possible out of all possible choices (Figure 7).

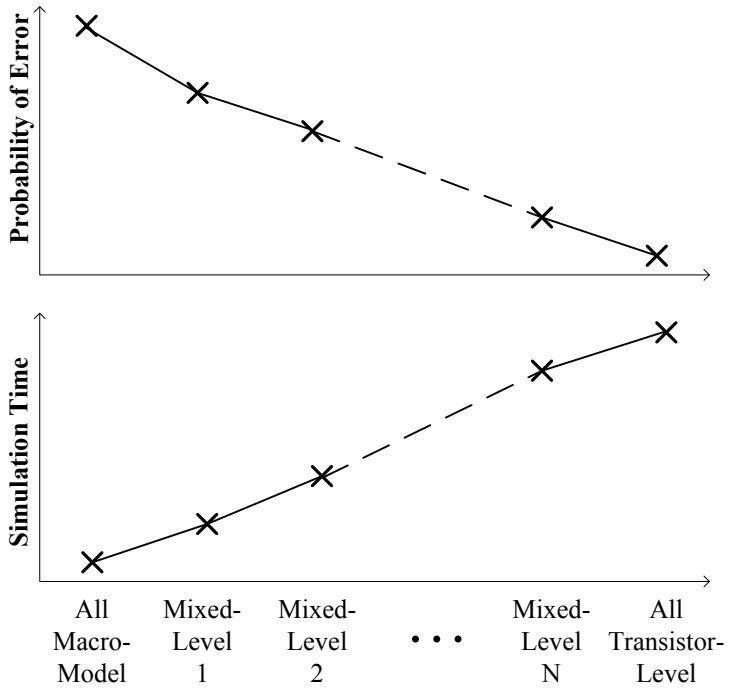

Figure 6 Predicted simulation time and probability of finding errors at a given simulation step of the proposed strategy.

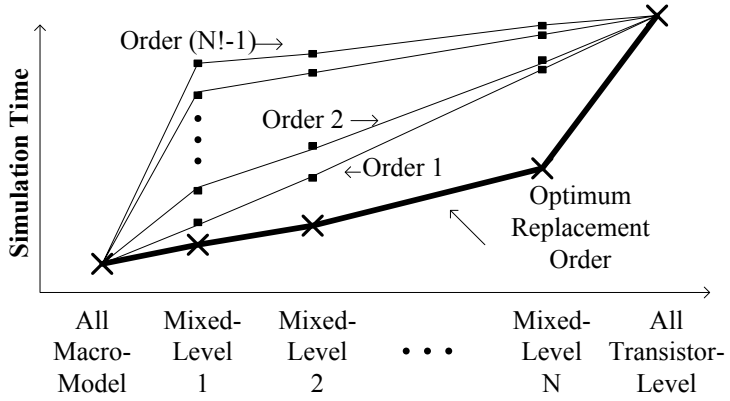

Figure 7 The proposed strategy verification time is minimized if circuit blocks are replaced based on their simulation time expense (i.e., optimum replacement order).

C. Determining the optimal replacement order from a set of screening simulations

The time it takes to finish a transient simulation is the summation of times each discrete step in the simulation incurs to compute a solution,

$$t_{sim} = \sum_{k=1}^{N_{Steps}} t_k \ , \tag{5}$$

where N_{Steps} is the total number of steps in the simulation, which is controlled by the simulator to achieve a certain level of accuracy [22]. The computation time of each time step is mostly dominated by the time

required to solve the matrix of equations for which the Newton-Raphson (NR) method is used until the solution satisfies the given time-step and NR tolerances,

$$t_k = (1 + N_{Time\text{-}Adj}) N_{Iteration} t_{NR}, \quad (6)$$

where $N_{Iteration}$ is the number of iterations required to solve the NR matrix, t_{NR} is the time required to solve each matrix iteration, and $N_{Time\text{-}Adj}$ is the number of time-step adjustments used to satisfy step tolerance for each time step. Average simulation time $\overline{t_{sim}}$ is therefore

$$\overline{t_{sim}} = N_{Steps} t_{NR} \cdot \overline{(1 + N_{Time\text{-}Adj}) N_{Iteration}}, \quad (7)$$

where $\overline{(1 + N_{Time\text{-}adj}) N_{Iteration}}$ is the average number of loop iterations at each step.

The t_{NR} is almost constant for a given topology and proportional to the number of circuit nodes cubed (i.e., nodes^3) [22], which explains why complex circuits have long simulation times. $N_{Iteration}$ depends on the linearity of the models, and the convergence of the NR method. N_{Steps} and $N_{Time\text{-}Adj}$ depend on frequency of operation of the circuits. As a result, a less complex circuit can be computationally more intensive if its transistor-level models superimpose a significant increase in N_{Steps}. Although predictions can be made about the effects of various blocks on simulation time, generally it is not possible to determine how the transistor-level model of each block slows down the simulation just by investigating netlist data (i.e., number of equations and nodes).

To determine the optimal replacement order, a screening set of simulations is proposed. The idea is to perform a set of mostly macro-level model simulations where only one macro model at a time is replaced with its respective transistor-level model (N simulations for N blocks). Consequently, the top-level blocks can be ranked and therefore replaced in the subsequent set of screening simulations according to their respective simulation times. Although screening simulations add overhead, they are only performed here to study the nature of the problem and project general conclusions, which are to be drawn later. Consequently, these screening simulations are not an essential part of the proposed verification process for ICs but simply the means through which an optimal replacement order is extracted for a general class of circuits.

IV. NUMERICAL CASE-STUDY RESULTS

To evaluate the proposed strategy, a case study of a representative mixed-signal environment such as a current-mode, pulse-width modulated (PWM) buck (step-down) dc-dc converter (Figure 1) is analyzed within the context of simulation time. The goal is to determine an optimal replacement sequence from a set of screening simulations. Evaluating the resulting replacement order will shed insight into the computational needs of the various components comprising the mixed-signal environment, especially

switching regulators, most of which have similar functional units (i.e., error amplifier, comparators, bandgap reference, drivers and dead-time control, power train, and power-on-reset and related start-up control electronics). To decouple convergence issues from the purpose of the foregoing study, convergence problems were avoided by carefully synthesizing macro models to define all possible states (i.e., all outputs were defined for all possible input conditions). Convergence problems with transistor-level simulations, on the other hand, are often sensitive to the simulator's transient tolerance setting, and to use a consistent testing environment, all simulations were performed with the transient tolerance setting for which the all transistor top-level simulation converged.

The 0.5µm CMOS switching regulator circuit shown in Figure 1 was designed to convert a Lithium-Ion (Li-Ion) battery voltage (2.7-4.2V) to a constant 1.5V output voltage with ±3% accuracy, source up to 1A of load current at a switching frequency of 1MHz, and soft-start within 0.5ms. The pertinent functional blocks of this design are the output power stage, signal generator, driver and dead-time control (DTC) circuit, error amplifier, comparator, voltage reference, and power-on-reset block. The power stage consisted of a 3.9µH inductor, 47µF output capacitor, and PMOS and NMOS power switches with typical turn-on resistances of 65mΩ and 27mΩ, respectively. A summary of the parameter values for the prototype current-mode controller shown in Figure 1 is listed in Table 1.

Table 1. Design parameters and simulated specifications for the prototype current-mode buck converter shown in Figure 1.

Design Parameter/Specification	Value
L	3.9µH
C	47µF
R_a	15kΩ
R_b	1kΩ
R_c	2kΩ
C_z	20nF
Switching Frequency	1MHz
Current-Sensing Gain	0.5V/A
Compensation Ramp Slope	0.1A/µs
Voltage-Loop Gain Bandwidth	100kHz
Error Amplifier GBW	10MHz
Summing Comparator Delay	<70ns for 10mV overdrive
Output Voltage	1.5V
Maximum Load Current	1A
Load Regulation (I_{load}=0->0.8A, V_{in}=3.3V)	-0.4%
Output Voltage Ripple (Steady State + Transient (0-1A)	<±50mV
Soft Start Time	0.5ms

The complete design process (i.e., system and block-level design and top-level verification) was executed within a Cadence platform, an industry standard that integrates macro- and transistor-based circuits with their physical layout representation and verifies their schematic-to-physical mappings via simulations, layout-versus-schematic, and design-rule checking tools. To best qualify and verify the functionality and response of the supply circuit to various loads, a 1.5ms transient benchmark simulation was defined that included various load current transitions. With this simulation, which is performed at each step of the proposed simulation process (i.e., from the all macro-based to the all transistor-based simulation), start-up time, soft-start performance, steady-state operation, output voltage ripple, load regulation, and transient response to load variations are all tested.

After the design was completely finished, simulations were repeated to ascertain and record simulation times and transient points of each mixed-level simulation step using Spectre simulator on an Ultra 10 Sun computer with *moderate* and *trapezoidal* tolerance and integration settings, respectively. First, an all macro-model simulation of the system was performed, with the exception of the power stage for which no behavioral model was used, as discussed earlier in the text, because of its critical role in determining accuracy, load and line regulation, and dynamic response performance and relative low impact on simulation time (it only consists of six electrical components and ten nodes). Then, screening simulations where only one macro-model at a time was replaced with its transistor-based equivalent in all macro-model simulation were performed (i.e., six simulations for six blocks), and their simulation time and performance characteristics were recorded. The results of the screening simulations, which are tabulated in Table 2, showed that the error amplifier incurred the least computational overhead on simulation time, followed by the comparator, bandgap reference, power-on-reset, driver, and wave generator circuits.

Table 2. Case study results of the top-level replacement sequence.

Blocks / Experiments	Power Stage	Amplifier	Comparator	Reference	Power-on-Reset	Driver	Signal Generator	No. of Nodes	No. of Equations	No. of BSIM Models	No. of Tran. Steps	Simulation Time (s)	Normalized Simulation Time
Start													
All Macro	T	M	M	M	M	M	M	138	221	24	186K	897	NA
Trial 1- *Screening Sim.*													
All Macro	T	M	M	M	M	M	M	138	221	24	186K	897	1x
Amplifier	T	T	M	M	M	M	M	136	200	86	186K	1.44K	1.6x
Comparator	T	M	T	M	M	M	M	154	214	94	186K	1.55K	1.72x
Reference	T	M	M	T	M	M	M	205	275	73	190K	1.79K	1.99x
Power-on-Reset	T	M	M	M	T	M	M	253	325	268	187K	3.6K	4.02x
Driver	T	M	M	M	M	T	M	173	242	128	122K	7.47K	8.32x
Signal Generator	T	M	M	M	M	M	T	313	287	391	190K	11.8K	13.2x
Trial 2													
All Macro - 1	T	T	M	M	M	M	M	136	200	86	186K	1.44K	1x
Comparator	T	T	T	M	M	M	M	148	196	122	186K	1.76K	1.22x
Reference	T	T	M	T	M	M	M	205	258	135	190K	1.82K	1.26x
Power-on-Reset	T	T	M	M	T	M	M	251	304	330	187K	4.11K	2.86x
Driver	T	T	M	M	M	T	M	167	224	156	120K	8.38K	5.83x
Signal Generator	T	T	M	M	M	M	T	313	370	453	190K	13.0K	9.08x
Trial 3													
All Macro - 2	T	T	T	M	M	M	M	148	196	122	186K	1.76K	1x
Reference	T	T	T	T	M	M	M	215	251	171	325K	3.28K	1.87x
Power-on-Reset	T	T	T	M	T	M	M	330	354	415	187K	7.27K	4.13x
Driver	T	T	T	M	M	T	M	179	220	192	134K	10.0K	5.70x
Signal Generator	T	T	T	M	M	M	T	323	362	489	189K	13.8K	7.85x
Trial 4													
All Macro - 3	T	T	T	T	M	M	M	215	251	171	325K	3.28K	1x
Power-on-Reset	T	T	T	T	T	M	M	330	354	415	327K	7.16K	2.18x
Driver	T	T	T	T	M	T	M	246	274	241	797K	9.60K	2.92x
Signal Generator	T	T	T	T	M	M	T	390	416	538	425K	13.3K	4.06x
Trial 5													
All Macro - 4	T	T	T	T	T	M	M	330	354	415	327K	7.16K	1x
Driver	T	T	T	T	T	T	M	361	378	485	802K	18.1K	2.53x
Signal Generator	T	T	T	T	T	M	T	505	525	782	428K	19.8K	2.67x
Last Step													
All Macro - 5	T	T	T	T	T	T	M	361	378	485	802K	18.1K	1x
All Transistor	T	T	T	T	T	T	T	536	544	852	650K	30K	1.66x

Next, the results of the screening simulations were verified against various mixed-level simulations. For instance, the screening results showed that the driver incurs more computation time than the power-on-reset block, and if this is indeed true, it follows that the driver incurs more time whether or not the error amplifier, comparator, and reference are replaced with their transistor-level models. Consequently, each of the remaining macro-models was replaced with their transistor-level equivalents, one at a time, and their simulation performance recorded and compared. This process was repeated for every subsequent step in the replacement sequence, resulting in a total of 22 simulations, one for all macro models, six for the screening process, five to verify the replacement order results of the next 5 circuit blocks (screening process for a subset of the blocks), four to verify the results of the next 4 blocks, and so on, the outcome of which is also summarized in Table 1. The results of all mixed-level simulations, from the five- to the two-block screening process, confirmed the consistency of the replacement order found with the first set of screening simulations, verifying the sequence to be in fact the optimal simulation arrangement.

Figure 8 illustrates the switching behavior and regulating performance of the all macro- and all transistor-based prototype DC-DC current-mode converter during and past start-up conditions (first 1.5ms), when the output is exposed to 0-1A, 5kHz, 50% duty-cycled load dumps. These simulating conditions reveal start-up, switching, and transient response as well as steady-state behavior and proneness to instabilities, all of which are critical metrics of the design. The purpose of this complex simulation set-up is to show how well the 15-minute all macro-model simulation resembles the 8-hour all transistor-based counterpart, indicating the ability of the macro-model simulation to predict and detect possible issues in relatively short time spans. The slight “bump” more prevalently seen at the beginning of the macro-based simulation is also present in the all transistor counterpart, but to a lesser degree. The reason for this difference is the slew-rate limited operation of the all transistor error amplifier circuit when operated at its lowest input common-mode range, a parameter that was not included in its macro model, which explains why the output is unable to rise as quickly in the all-transistor case.

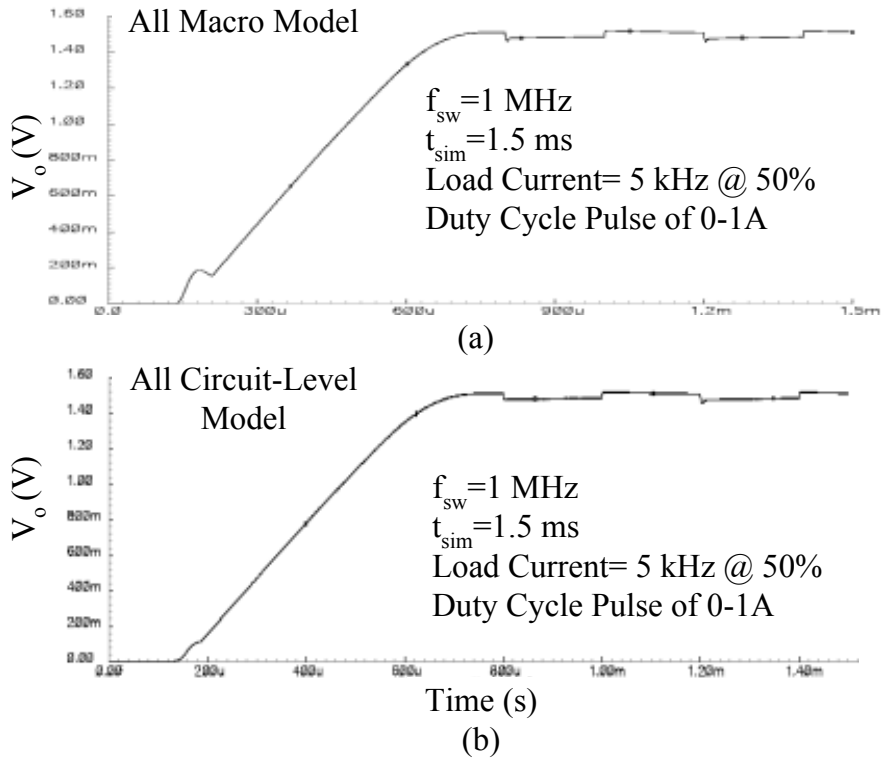

Figure 8. Top-level start-up transient waveforms of the regulator's output voltage using (a) all macro- and (b) all transistor-based simulations.

The results of the case study presented show that the transistor-level models of the signal generator and driver circuits account for approximately 60% of the total simulation time because of their high frequency spike and glitch content, and this is in spite of the relative simplicity of the driver block, which has less transistors, nodes, and working equations than the reference and power-on-reset functions. The transistor-level models of the analog building blocks (i.e., error amplifier, comparator, and reference) were only responsible for 11% of the total simulation time. Generally, linear analog blocks incur the least overhead, followed by nonlinear analog blocks like comparators and bi-stable bandgap references, low frequency digital functions like power-on-reset, and finally high speed driver and signal generator circuits. Within these broad categories, computation time of course increases with the number of working nodes, that is to say, with the number of transistors and therefore number of equations.

According to the results of the case study, if the proposed strategy is used for top-level simulations, the screening simulation takes 460 minutes and following iterations of the mixed-level simulations incur 29, 54, 119, and 301 minutes, respectively, compared to the 499 minutes required by the all transistor-based simulation. Consequently, if no errors were to be found, the proposed sequence (mixed-level simulations and an all transistor-level simulation) incurs 1,017 min. of simulation time,

which is equivalent to approximately two all-transistor-level simulations, yet at least 6 top-level simulations would be tested. And if a set of screening simulations were to be included, which is not a requirement, given the results of the study, the proposed sequence (screening simulation set, mixed-level simulations, and an all transistor-level simulation) incurs 1,462 min. of simulation time, roughly the equivalent of 3 all transistor-based top-level simulations, but actually verifying 11 simulations.

In practice, the benefits of the strategy are even more pronounced. Given, the complexity of the system, errors occur that invariably necessitate iterations, and iterations in the proposed scheme incur the least time (15 min. for the first level, 29 min. for the second, and so on). In fact, most top-level errors are the result of incorrect inter-block connections, which can be detected and corrected at the first level of the proposed sequence, when simulations take up about 15 min. As the replacement sequence advances, the design is cleared of these errors, leaving only a few all transistor-based top-level simulations to perform to detect IC-related issues like leakage, quiescent, and transient supply currents. The proposed replacement sequence is therefore potentially capable of detecting many errors in the same time frame the traditional, all transistor-based simulation would have taken to detect less than a few. In the case of an extremely complex system, where all transistor-level top-level simulations are computationally prohibitive (e.g., simulation time of a few weeks because of convergence problems and such), the screening simulation suite can be used to capture top-level connectivity errors, in addition to determining the convergence culprit of the all-transistor top-level simulation. Isolating the convergence issue allows the designer to verify the rest of the system by simply replacing the problem circuit with its macro-model circuit.

The results of the case study generally apply to dc-dc converter circuits, given the similarity of the functional units. What is more, because of the qualitative nature of the blocks, the results can be further extrapolated to mixed-signal environments. More specifically, highly linear and analog blocks incur the least computational effort, whereas high frequency nonlinear blocks incur the most. Bandgap references are nonlinear analog blocks because they are bi-stable in nature (i.e., they require start-up circuits to ensure they work in the correct state) and are therefore more computational intensive than op-amps and even comparators. Start-up and low frequency digital blocks, which simply ascertain a state, require less time than high frequency digital circuits, which in turn require less time than more complex digital circuits (with feedback) like clock and ramp generators. Depending on how these characteristics apply to a given class of mixed-signal circuits, screening simulations may or may not be eliminated.

V. CONCLUSIONS

Increasing fault coverage and decreasing simulation time of top-level simulations are conflicting requirements. To mitigate this adverse relationship, a series of mixed-level simulations have been

proposed and verified, whereby each block of an all macro-model simulation is replaced with its equivalent transistor-level circuit, one at a time, with the least time-consuming blocks first. To determine the optimal replacement sequence, screening simulations were performed where an all macro-model setup was modified by replacing only one of its macro models with its respective transistor-level model, one at a time. To verify this within the context of a mixed-signal environment, a switching buck regulator case was tested and evaluated, from which an optimal replacement order was determined. The results show the analog linear blocks are the least time-consuming, accounting for 11% of the total simulation time, and driver and signal generator circuits are the most time-consuming, accounting for approximately 60% of the time. These results can be extended to all dc-dc converter circuits because of the similarities of the functional blocks, and even some mixed-signal environments because of the nature of the effects – linear analog blocks incur less time than high frequency digital blocks with feedback. In the end, in the time that only three all transistor-based simulations are performed, more than 11 top-level simulations can be analyzed with the proposed strategy, which significantly increases the fault coverage in the same time. The benefits are even more pronounced when errors in the circuit exist, which the proposed strategy will more than likely catch earlier in the sequence and therefore incur less overall time to resolve. The proposed strategy also highlights how macro-model based simulations can be used to verify system functionality (i.e., architecture), identify how key block-level performance parameters affect the system, and ascertain permissible ranges for them, all before any transistor-level design is attempted. Ascertaining these target specifications in this fashion is a useful means of mitigating risk and accelerating the entire design cycle, which is why more details on this, although not presented here for brevity, merit time and scrutiny.

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