One Clock-Cycle Response 0.5µm CMOS Dual-Mode ΣΔ DC–DC Bypass Boost Converter Stable over Wide $R_{ESR}LC$ Variations

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***Abstract*—Power supplies in portable applications must not only conform and adapt to their highly integrated on-chip and in-package environments but also, more intrinsically, respond quickly to fast load dumps to achieve and maintain high accuracy. The frequency-compensation network, however, limits speed and regulation performance because it must cater to all combinations of filter capacitor C_O, inductor L, and C_O's equivalent series resistance R_{ESR} resulting from tolerance and modal design targets. As such, it must compensate the worst-case condition and therefore restrain the performance of all other possible scenarios, even if the likelihood of occurrence of the latter is considerably high and the former substantially low. Sigma-delta (ΣΔ) control, which addresses this issue in buck converters by easing its compensation requirements and offering one-cycle transient response, has not been able to simultaneously achieve high bandwidth, high accuracy, and wide $R_{ESR}LC$ compliance in boost converters. This paper presents a dual-mode ΣΔ boost bypass converter, which by using a high-bandwidth bypass path only during transient load-dump events, was experimentally 1.41 to 6 times faster than the state of the art in current-mode ΣΔ boost supplies, and this without any compromise in $R_{ESR}LC$ compliance range (0-50mΩ, 1-30µH, and 1-350µF).**

***Index Terms*—LC filter compliance, switching dc-dc supplies, ΣΔ boost converters, load transient response.**

I. Introduction

In portable applications like cellular phones, PDAs, and the like, integrated BiCMOS and CMOS switching dc-dc supply circuits reduce cost, size, component count, and design complexity (from a user's perspective). One of the critical bottlenecks in obtaining a fully integrated solution, however, is the frequency-compensation circuit, which is designed around off-chip power LC filter devices to obtain optimal performance [1]. The fact is mode-rich state-of-the-art applications, manufacturing tolerances, and parameter drifts expose dc-dc converter integrated circuits (IC) to wide variations in output capacitance C_O, power inductance L, and C_O's equivalent series resistance R_{ESR}, inducing considerable changes in loop-gain and transient response, compromising feedback stability or transient response. As a result, to guarantee stability and high bandwidth with a fixed on-chip frequency-compensation circuit, the design necessarily constrains $R_{ESR}LC$ values within a narrow target range [1]. This is especially detrimental in compact high-performance multiple input-output converters [2]-[3] where the on-chip or in-package LC filter is variable by design to dynamically accommodate the diverse loading conditions of the system.

Unclocked or asynchronous sigma-delta (ΣΔ) buck converters [4]-[8] are self-compensating and free of the speed-stability tradeoffs of most dc-dc converters because the control loop in these converters resembles current-mode control by indirectly sensing the inductor current ripple via the ripple voltage it drops across C_O's R_{ESR}. In other words, the ESR voltage mostly sets the terminal ripple voltage of C_O, impressing the inductor ripple current information on the output voltage and achieving current-mode-like control. The resulting single-pole-like response yields higher bandwidth and more explicit control over the output ripple voltage [7].

Extending this technique and its benefits to boost converters, which are popular in portable electronics for boosting battery voltages to 3.3-5V, is not straightforward because the inductor current does not fully flow to C_O. Consequently, in realizing ΣΔ control in boost converters, the feedback circuit must explicitly sense and mix inductor current with the sensed output voltage [9]. Such techniques, however, resurrect the limiting speed-stability tradeoffs ΣΔ control averted in buck converters in the first place, forcing the designer to adjust current and voltage gains thereby reducing the loop bandwidth in order to accommodate large $R_{ESR}LC$ filter values.

This paper presents a dual-mode boost ΣΔ bypass controller IC that overcomes the aforementioned speed-stability compromise by introducing a high-speed bypass mode (and circuit) that engages only during transient load-dump events, achieving both high bandwidth and wide $R_{ESR}LC$ compliance. To this end, Section II first reviews and discusses the stability requirements of ΣΔ converters and their resulting transient response to fast load dumps. Section III then describes the proposed dual-mode technique and the design of its IC-prototype embodiment, followed by experimental results in

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Section IV; Section V draws relevant conclusions.

II. ΣΔ CONVERTERS

A. ΣΔ Control in Buck Converters

A ΣΔ buck converter, as shown in Fig. 1, controls the frequency and duty cycle of PMOS switch S_M by comparing rippling output voltage v_O via sensed voltage v_S against dc reference V_{REF} with comparator CP_V. Operationally, ac inductor ripple current i_l flows into C_O and its R_{ESR} (which is relatively large in these converters at 100-250mΩ to ensure its voltage -v_{esr}- overwhelms ac capacitor voltage v_c) [7] as capacitor displacement current i_c, forcing ac output ripple voltage v_o to mimic i_l ($v_o \approx v_{esr} = i_l R_{ESR}$). As a result, in regulating v_o, the converter also regulates i_l, which in the process simplifies the frequency response of the converter to that of a single-pole system, as in current-mode control, guaranteeing stability, irrespective of $R_{ESR}LC$ values.

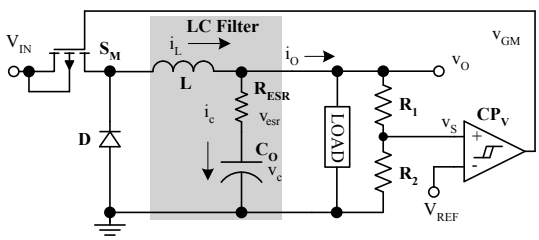


Fig. 1. Circuit schematic of a switching ΣΔ buck converter.

In a positive load-step transient event, when load current i_O suddenly rises, comparator CP_V detects the voltage droop the now larger i_O induces on v_O and consequently switches S_M on indefinitely (i.e., at 100% duty cycle) until v_O returns within CP_V's predefined hysteretic window limits, that is, within an acceptably low margin of V_{REF}. During S_M's on time, the inductor voltage being nearly constant at $V_{IN} - V_O$, inductor current i_L slews in a single switching cycle until it fully supplies i_O and recharges C_O back to V_{REF} [8]. In other words, only the inductor and capacitor slew-rate limits and second-order delays across the comparator and switch set the response time (effective bandwidth) of the system. Note a negative load dump undergoes a similar but reversed response.

B. ΣΔ Control in Boost Converters

Unlike buck converters, ac inductor ripple current i_l in boost converters does not flow completely to output capacitor C_O because reverse-biased diode D (shown in Fig. 2) temporarily disconnects L from v_O (and C_O) when switch S_M conducts all of i_L to ground. The resulting ac ripple voltage in v_O does not fully reflect the behavior of i_l, as it does in buck converters with non-negligible R_{ESR} values, which means ΣΔ control in boost converters cannot rely on v_O alone [9]. The negative feedback loop in a boosting supply must therefore sense, scale, and mix i_L with v_O explicitly (e.g., mix $i_L R_I g_{mi}$ and $v_O g_{mv}$ into R_S as scaled sum v_{SUM}) to achieve current-mode-like control characteristics. A hysteretic comparator then modulates S_M's frequency and duty cycle based on how the scaled sum (v_{SUM}) of the ripples compares against a user-defined hysteresis window. Note the voltage feedback loop modulates the effective inductor reference current $v_{I.REF}/R_I$, which is also the average inductor current I_L (or low-pass filtered -LPF- version of i_L) to whatever is necessary to fully supply i_O.

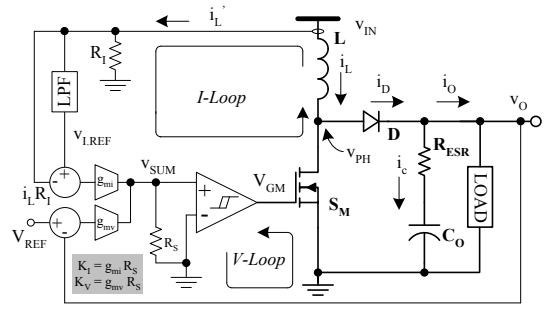


Fig. 2. Circuit schematic of a switching ΣΔ boost converter.

Within the context of averaged small-signal analysis, the relatively high-gain, low-bandwidth voltage control loop (V Loop) of the system effectively embeds a higher bandwidth, lower gain current loop (I Loop), as shown Fig. 3 [10]. At low frequencies, below low-pass filter pole p_{LPF}, $i_L R_I$ nearly equals $v_{I.REF}$ and the gain of the current loop is practically zero, but increasing with frequency until reaching its highest possible gain at frequencies past p_{LPF}. The current loop's gain again drops at high frequencies, past the complex LC double poles, when the ac voltage across L decreases. Given that i_L is, for all practical purposes, regulated to higher frequencies and therefore is a current source to the outer voltage loop at moderate-to-high frequencies, C_O and effective load resistance R_O set the dominant low-frequency pole of the system while L and R_O invoke right-half plane zero z_{RHP} [11].

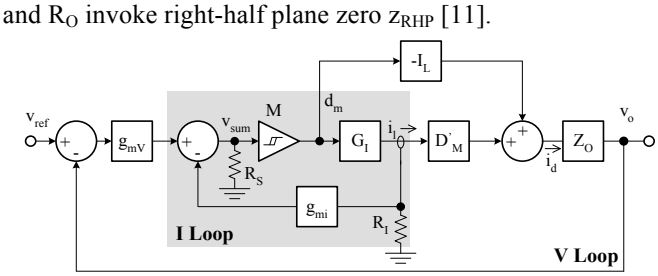


Fig. 3. Small-signal equivalent control diagram of switching ΣΔ boost converter at moderate-to-high frequencies.

For stable conditions to prevail, the unity-gain frequency of the voltage loop (i.e., the system -$f_{V.0dB}$-) must fall below z_{RHP} and i_L must remain a current source (i.e., current loop must stay closed with considerable loop gain) for the frequency range of interest to the voltage loop [10]. As such, $f_{V.0dB}$ must stay below both z_{RHP} and current-loop bandwidth $f_{I.0dB}$:

$$f_{0dBV} \approx \frac{g_{mv} D_M'}{2\pi R_I g_{mi} C_O} << f_{0dBI} \approx \frac{R_I g_{mi} R_S M V_O}{2\pi L}, \quad (1)$$

and

$$f_{0dBV} \approx \frac{g_{mv} D_M'}{2\pi R_I g_{mi} C_O} < z_{RHP} = \frac{D_M' V_O}{2\pi L I_L}, \quad (2)$$

or

$$\frac{L I_L}{V_O C_O} = \frac{L I_O}{C_O V_O D_M'} < \frac{R_I g_{mi}}{g_{mv}}, \quad (3)$$

where D_M is the duty-cycle of S_M, D_M' is (1-D_M), and M is the modulator gain. Note z_{RHP} and $f_{I.0dB}$ shift to lower frequencies with increasing inductance values, which means $f_{V.0dB}$ must also decrease accordingly, in an ideal case. LPF pole p_{LPF}, whose location indicates the lowest frequency at which the current loop is closed, must also be below the worst-case value

of $f_{V.0dB}$ to ensure there is enough gain for i_L to remain a current source:

$$p_{LPF} \tilde{<} f_{V.0dB}\big|_{min} = \frac{D_M'^2 V_O}{2\pi L I_L}. \quad (4)$$

Ultimately, the system responds to a load dump at the speed of the voltage loop, whose bandwidth is $f_{V.0dB}$, allowing switch S_M to cycle multiple times before restoring v_O back to its target window. LPF pole p_{LPF} limits the extent to which i_L naturally responds to a load dump by allowing moderate-to-high frequency ac error-correcting signals through the current loop. In other words, the current loop limits (while attempting to regulate) the rising and falling rates of average i_L below i_L's maximum possible slew-rates of V_{IN}/L and $(v_O - V_{IN})/L$. Because $f_{V.0dB}$ and p_{LPF} both decrease with increasing L, with the former also decreasing with decreasing C_O, the worst-case LC combination, from the perspective of stability, occurs at the highest L and lowest C_O, the condition for which gains $R_I g_{mi} R_S$ and $g_{mv} R_S$ and pole p_{LPF} are adjusted and transient-response performance over the entire LC filter range is sacrificed.

III. Proposed Dual-Mode ΣΔ Controller IC

The proposed ΣΔ boost controller IC in Fig. 4 overcomes the transient-response degradation associated with the worst-case LC combination by bypassing the main voltage loop (and its $f_{V.0dB}$) with a fast (and lower low-frequency loop-gain) feed-forward path only during transient events. The stability requirements of the main loop set the acceptable $R_{ESR}LC$ range for the system while the high-bandwidth bypass path allows the system to respond in one cycle at the maximum possible inductor current slew rate, the response of which is similar to ΣΔ buck converters. The transient improvement is achieved on chip (i.e., without an off-chip frequency compensation circuit) and without sacrificing LC compliance.

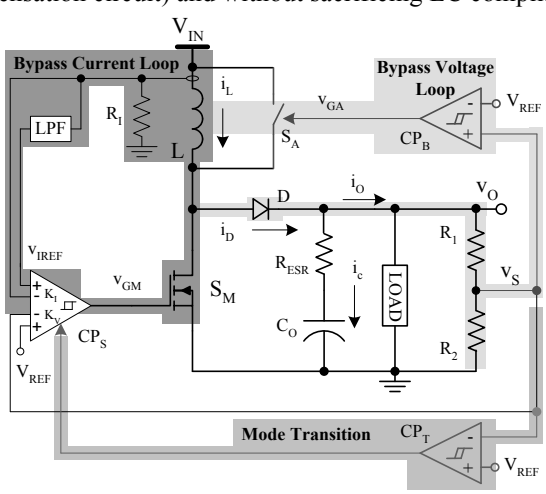


Fig. 4. Simplified schematic of the proposed dual-mode ΣΔ boost converter.

A. Steady-State and Bypass Operation

The basic objective of the bypass mode is to override nominal equivalent average inductor current reference $I_{L(nom)}$ ($v_{I.REF}/R_I$) to a higher value almost instantly only during load dumps and allow the bypass voltage loop to control and limit how much of the extra current in L flows to v_O. Initially, during steady-state conditions, the bypass circuit is inactive and load current i_O and S_M's average off duty cycle D_M' (i.e., one minus S_M's average on duty cycle D_M) set the nominal average inductor current $I_{L(nom)}$ required to support a given i_O, which is higher than i_O because S_M steers a portion of i_L away from v_O to ground according to D_M:

$$I_{L(nom)} = \frac{I_O}{D_M'} = \frac{I_O}{1\text{-}D_M}. \quad (5)$$

In the bypass mode, however, independent loops regulate i_L to a value higher than $I_{L(nom)}$ and sensed output voltage v_S to V_{REF}, as depicted in the equivalent circuit of Fig. 5.

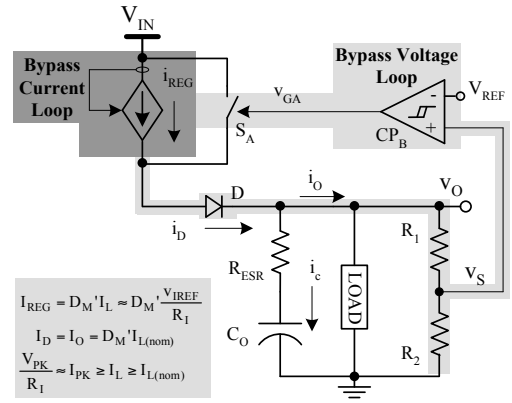


Fig. 5. Equivalent circuit of the proposed ΣΔ converter in the bypass mode.

The current loop, which modulates switching frequency f_{SW} and S_M's duty cycle d_M, has higher bandwidth and appears as a current source for frequencies of interest to the lower bandwidth bypass voltage loop controlling auxiliary switch S_A. In the bypass mode, inductor current i_L is regulated at a value I_{PK} or V_{PK}/R_I that is greater than $I_{L(nom)}$ (i.e., I_L required to support I_O). This means, unless otherwise limited, average diode current I_D is now higher than I_O, as a result of which C_O recharges quickly. Once v_O is back within the hysteretic window limit of bypass comparator CP_B and about to surpass its upper boundary, CP_B and S_A divert excess current away from D through S_A until i_O again discharges v_O to CP_B's lower window limit. The switching cycle repeats as average inductor current I_L gradually drops back to $I_{L(nom)}$, at which point the bypass loop stops switching and S_A remains open. Note as long as I_L exceeds $I_{L(nom)}$, the bypass voltage loop, by independently regulating v_O with higher loop gain than the current loop, ensures the voltage inputs of summing comparator CP_S are virtually short-circuited (i.e., $v_S \approx V_{REF}$), as shown in Fig. 6, allowing CP_S to regulate i_L exclusively.

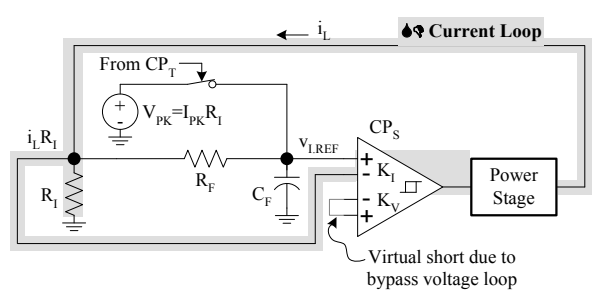


Fig. 6. Simplified conceptual circuit schematic of the dual-mode ΣΔ converter in bypass mode, as the bypass loop virtually shorts v_S and V_{REF} and the current loop regulates i_L to $v_{I.REF}/R_I$.

With respect to stability, as already mentioned, the unity-gain frequency of the current loop ($f_{I.0dB}$) must exceed that of the bypass voltage loop ($f_{B.0dB}$) so the inductor appears as a current source in the voltage loop, eliminating the complex conjugate pair associated with LC in the voltage loop [12]. Because the unity-gain bandwidth of a ΣΔ loop is its switching frequency, S_M's switching frequency ($f_{I.0dB}$) must exceed that of S_A ($f_{B.0dB}$). Therefore, since $f_{I.0dB}$ depends on the rising and falling rates of $i_L R_I$ as it traverses CP_S's hysteretic current window H_I,

$$f_{I.0dB} = \left(\frac{H_I}{R_I}\right)^{-1}\left(\frac{L}{V_{IN}} + \frac{L}{V_O - V_{IN}}\right)^{-1} = \frac{V_{IN}(V_O - V_{IN})R_I}{V_O H_I L} \qquad (6)$$

and $f_{B.0dB}$ on how fast excess i_D (i.e., $D_M'I_L - I_D$) and I_O charge and discharge output capacitor C_O between CP_B's hysteretic voltage window H_V,

$$f_{B.0dB} = \left(\frac{H_V(R_1 + R_2)}{R_2}\right)^{-1}\left(\frac{C_O}{I_O} + \frac{C_O}{(D_M'I_L - I_O)}\right)^{-1}, \qquad (7)$$

to force $f_{I.0dB}$ to be greater than $f_{B.0dB}$, C_O must exceed

$$C_O \geq \left(\frac{H_I}{H_V}\right)\left(\frac{I_O L}{V_O R_I D_M'}\right)\left(\frac{R_2}{R_1 + R_2}\right) \equiv C_{O(min)}, \qquad (8)$$

where the R_1-R_2 divider represent the effect of the resistive feedback factor on H_V and $C_{O(min)}$ the minimum stable output capacitance.

B. Transient Response and Mode Transition

During a positive load-dump event, when I_O suddenly rises and v_O droops in response, as shown in Fig. 7, the dual-mode converter enters its bypass mode, raising i_L to peak value I_{PK} (or V_{PK}/R_I) in a single switching cycle of S_M. Subsequently v_O (or v_S) is pulled back to $V_{REF}(R_1+R_2)/R_2$ (or V_{REF}) in a single switching cycle of S_A. Transient-detect comparator CP_T in Fig. 4 perceives the load dump and engages the bypass mode by sensing when v_S drops below V_{REF} by a preset threshold value of ΔV_{BP} (e.g., 2.5% of V_{REF}) (after the delay the comparator requires to switch: t_d). Then, CP_T clamps $v_{I.REF}$ to peak voltage V_{PK}, the value of which sets the maximum current the circuit can drive. Switch S_M therefore remains closed ($t_{t.M(on)}$) until i_L reaches V_{PK}/R_I (I_{PK}), the new value of $v_{I.REF}/R_I$. After S_M resumes switching and regulating i_L about I_{PK}, S_A remains open and allows all diode current i_D to flow to v_O until C_O recharges to $(V_{REF}+H_V/2)\cdot(R_1+R_2)/R_2$. Beyond this point, CP_B and S_A regulate v_S about V_{REF} by switching S_A, in other words, by steering excess inductor current away from C_O.

Ultimately, output voltage v_O droops in response to load dump Δi_O until i_L reaches I_{PK}. First, excess current Δi_O discharges C_O during delay t_d while v_S reaches $V_{REF} - \Delta V_{BP}$. Then, while S_M raises i_L from $i_{L(avg)}$ (or $v_{I.REF}/R_I$ or $I_{L(nom)1}$) to I_{PK} (or V_{PK}/R_I), i_D is zero and full load current I_O discharges C_O, yielding a total variation (Δv_O) of

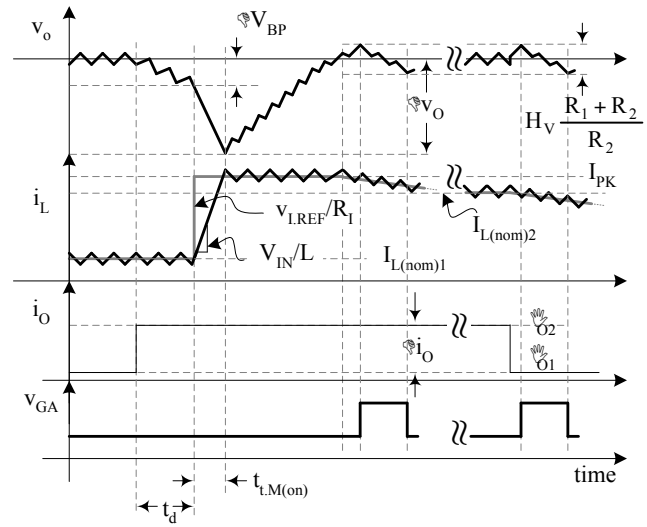


Fig. 7. Transient-response performance when presented with fast load-steps (positive and negative).

$$\Delta v_O = \Delta V_{BP} + \left(\frac{I_O}{C_O}\right)t_{t.M(on)}$$
$$= \Delta V_{BP} + \left(\frac{I_O}{C_O}\right)\left[\frac{(I_{PK} - I_{L(nom)1})L}{V_{IN}}\right]$$
$$= \Delta V_{BP} + \left(\frac{I_O}{C_O}\right)\frac{(V_{PK} - v_{I.REF})L}{R_I V_{IN}}. \qquad (9)$$

Note the ratio of L and C_O sets the dominant part of Δv_O.

Once sensed output voltage v_S is within the hysteretic voltage window of CP_B, to transition back to steady state, $i_{L(avg)}$ must somehow fall back to whatever value ($I_{L(nom)}$) is necessary to sustain I_O, reducing to zero the amount of excess current i_L that bypass comparator CP_B steers away from v_O through S_A. To that end, introducing a series negative offset voltage $V_{I.OS}$, as shown in Fig. 8, ensures i_L is always above its target (i.e., $i_{L(avg)}$ is greater than $v_{I.REF}/R_I$), forcing the loop to gradually decrease both $i_{L(avg)}$ and the excess current. Finally, when i_L is low enough to be able to fully supply i_O, and the excess current ($D_M'I_L$–I_O) is zero, the bypass loop stops switching (i.e., disengages), which means the main voltage loop now regulates v_O via S_M (Fig. 4) to its target. In other words, henceforth, $i_{L(avg)}$ equals $I_{L(nom)}$. Note the transition is continuous, allowing S_A to stop switching without incurring irregularities in S_M.

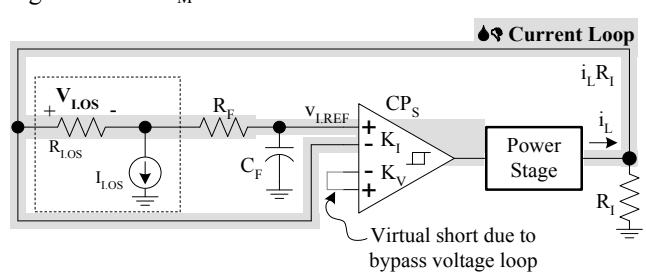


Fig. 8. Equivalent converter circuit in bypass mode with added offset voltage $V_{I.OS}$ to ensure $v_{I.REF}/R_I$ is slightly below $i_{L(avg)}$.

During a negative load dump, when i_O suddenly drops, as also shown in Fig. 7, $i_{L(avg)}$ automatically exceeds its new steady-state target and v_O rises above its target. As a result,

bypass comparator CP_B engages and diverts current away from v_O until v_S again drops to V_{REF}–$H_V/2$ (in one cycle of S_A). The circuit gradually transitions back to steady state in the same manner as described earlier, through $V_{I.OS}$.

IV. Experimental Results and Discussion

A. IC Design

The proposed dual-mode ΣΔ bypass converter was designed, fabricated, and evaluated using a 0.5µm, 5V CMOS process. The circuit embodiment of the converter, as shown in Fig. 9, employs a differential-signal processing scheme to attenuate the effects of substrate noise on the high-bandwidth ΣΔ loops [10]. For simplicity, series resistor R_I senses i_L with the understanding more power efficient techniques are possible and recommended [13]. Current-sense amplifier A_{DI}, which monitors the voltage across R_I, includes an internal RC filter that generates differential current reference $v_{I.REF}$. Differential preamplifier A_{DV} buffers and amplifies sensed output voltage v_S by 5V/V to decrease the effects of offsets and hysteretic window limits in posterior amplifiers and comparators on v_S and v_O (i.e., improve accuracy); A_{DV} drives differential summing amplifier A_{DS}, bypass hysteretic comparator CP_B, and transient-detect hysteretic comparator CP_B.

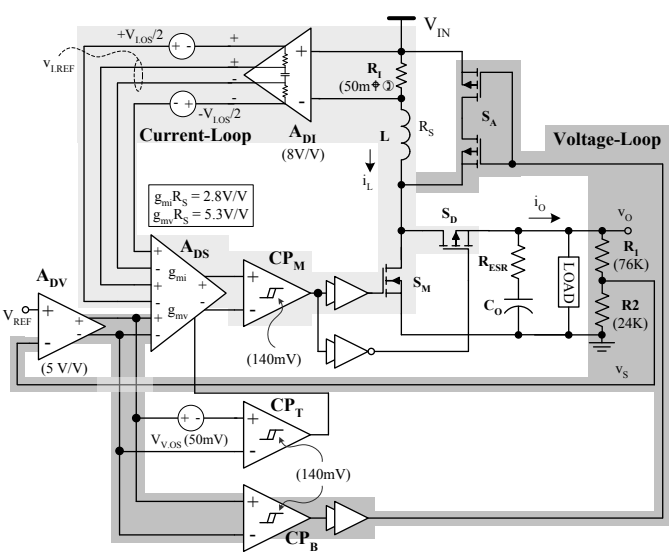
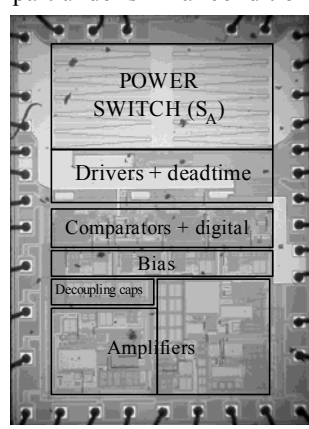


Fig. 9. 0.5µm CMOS circuit embodiment of the proposed dual-mode ΣΔ bypass boost converter.

For ease of design and reliability, main, bypass, and transient-detect comparators CP_M, CP_B, and CP_T adopt the same circuit architecture, which is designed to yield a hysteretic window of 140mV. The bypass threshold voltage (ΔV_{BP}) is composed of half the comparator hysteretic window plus an additional offset of 50mV ($V_{V.OS}$) that is added between CP_B and CP_T. Differential current-sense amplifier A_{DI} includes a 40mV offset voltage ($V_{I.OS}$) at its output to ensure i_L is below its target by $V_{I.OS}/R_I$ during the bypass mode, to gradually transition back to steady state after a load dump. The designed offsets are sufficiently large to dwarf the transistor mismatch-induced offsets in A_{DI}, CP_B, and CP_T and ensure the polarities of $V_{V.OS}$ and $V_{I.OS}$ remain unchanged across process and temperature corners.

In the absence of deep-N or buried layer isolation structures, the bulk of a single PMOS transistor serving the function of auxiliary switch S_A could not be connected to the highest potential (v_O) because of latch-up concerns. Whenever the switching node flies above v_O following the turn-off of S_M, S_A's body diode can conduct engaging the parasitic vertical PNP transistor present, channeling considerable current to the substrate. A second PMOS device is therefore added in series to use its reverse-biased body diode to block the foregoing current. And during normal operating conditions, when v_O is higher than V_{IN}, as the body diode of the first blocks the current of the second.

The proposed ΣΔ controller 0.5µm IC was designed to supply power from a 2.7-4.2V Li-Ion battery and drive a 0-1A load at 5V ± 5% with as wide an $R_{ESR}LC$ range as possible (0-50mΩ, 1-30µH, and 1-350µL was achieved). The total silicon surface area the IC occupied was 1.9 x 2.6 mm (Fig. 10). The peak efficiency of the converter was 93% at 0.4A with a biasing quiescent current of 1.5mA. The total output voltage variation of the converter in response to a 0.1-1A load dump (Δi_O) with 5mΩ, 5.6µH, and 53µF of $R_{ESR}LC$ was 200mV, which constitutes a 4x improvement over its non-bypassed counterpart under similar conditions (800mV).



V_{IN}	2.7-4.2V
V_O	5V ± 5%
I_O	0-1A
$R_{ESR}LC$ space	0-50mΩ 1-30µH 1-350µF
η_{peak}	93%
I_Q	1.5mA
Δv_O(5.6µH, 53µF, 0.1-1A)	0.23V
Process	0.5µm CMOS
Die size	(1.9 x 2.6) mm²

Fig. 10. Die photograph and performance summary.

B. LC Compliance

The measured $R_{ESR}LC$ space for which the converter was stable is 0-50mΩ, 1-30µH, and 1-350µF, as illustrated in Fig. 11. This range was determined by subjecting the converter to 0.1-1A load dumps with 100ns rise and fall times. The stability limit was observed as a loss of regulation for the proposed ΣΔ converter in the bypass mode, as the bypass loop was no longer able to control the loop, and sub-harmonic oscillations for the non-bypassed (state-of-the-art) ΣΔ boost converter [14].

The stability limits for both converters, with and without the bypass path, are reached when their respective current-loop bandwidths ($f_{I.0dB}$) approach their voltage-loop counterparts ($f_{B.0dB}$ and $f_{V.0dB}$), as that is when L ceases to be a current source for the voltage loop, be it the main loop or the bypass loop. As a result, because $f_{V.0dB}$ and $f_{B.0dB}$ increase with decreasing C_O and increasing I_O and $f_{I.0dB}$ and RHP zero z_{RHP} decrease with increasing L and decreasing V_{IN}, the highest L-I_O (30µH-1A) and lowest C_O-V_{IN} (12µF-2.7V) combination constitutes worst-case conditions. Since R_{ESR} essentially

introduces a left-half plane zero in the voltage loop, increasing R_{ESR} also increases $f_{V.0dB}$ and $f_{B.0dB}$, which means the above-mentioned limits along with the highest R_{ESR} value (50mΩ) describes the worst-case stability point of the converter. In other words, $C_{O(min)}$ increases with increasing L, I_O, and R_{ESR} and decreasing V_{IN}.

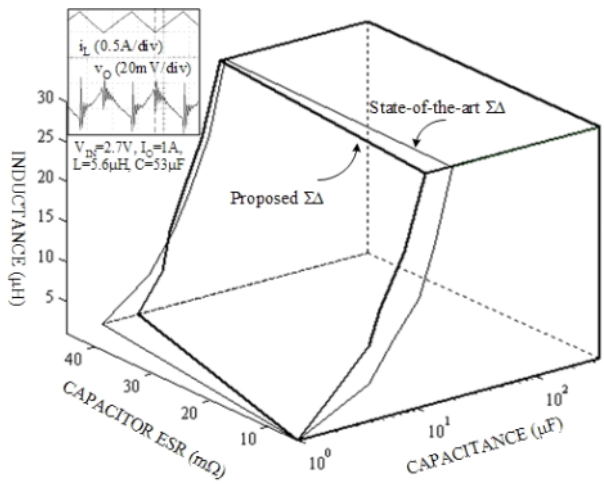


Fig. 11. Nominal steady-state snapshot of inductor current i_L and output voltage v_O ripples (inset) for the proposed solution and experimental $R_{ESR}LC$ stability space for both the proposed dual- and state-of-the-art single-mode boost ΣΔ converters.

The maximum capacitance was limited to 350μF as a practical limit for the intended portable application space (the circuit is stable at higher C_O values). Similarly, the maximum R_{ESR} value was limited to 50mΩ to keep the output voltage ripple acceptably low under a 1A load. Under these conditions and constraints, the stability spaces for the proposed and the state-of-the-art converters are approximately equal in "volume."

C. *Transient Load-Dump Performance*

As shown in Fig. 12(a), the transient-response variation of v_O (Δv_O) in response to 0.1-1A load dumps (Δi_O) with 100ns rise and fall times under 2.7V, 5.6μH, 53μF, and 5mΩ of V_{IN}, L, C_O, and R_{ESR} was 200mV for the proposed dual-mode scheme and 800mV for its single-mode state-of-the-art counterpart. While the proposed converter responds by increasing i_L above its target (to I_{PK} or V_{PK}/R_I) in one switching cycle of S_M, the state-of-the-art circuit increases i_L gradually, pulling v_O back to regulation in several cycles of S_M, which is why the proposed solution exhibits a four-fold improvement over its predecessor. In a negative load-step (Fig. 12(b)), while the excess inductor current is immediately bypassed by switch S_A in the proposed converter keeping the output voltage overshoot low (<75mV), the excess inductor energy causes a large voltage overshoot (600mV) in the state-of-the-art converter.

Decreasing (increasing) L increases (decreases) the rate at which i_L responds to a load dump, as shown in Fig. 13, thereby decreasing (increasing) the time v_O slews (reducing Δv_O). Similarly, increasing (decreasing) C_O decreases (increases) v_O's droop rate in response to a load dump (Fig. 14). Note increasing (decreasing) C_O also increases (decreases) the delay time between the load step and the onset of bypass threshold voltage ΔV_{BP} (t_d) (Fig. 7), which is why the onset of i_L rising shifts with C_O.

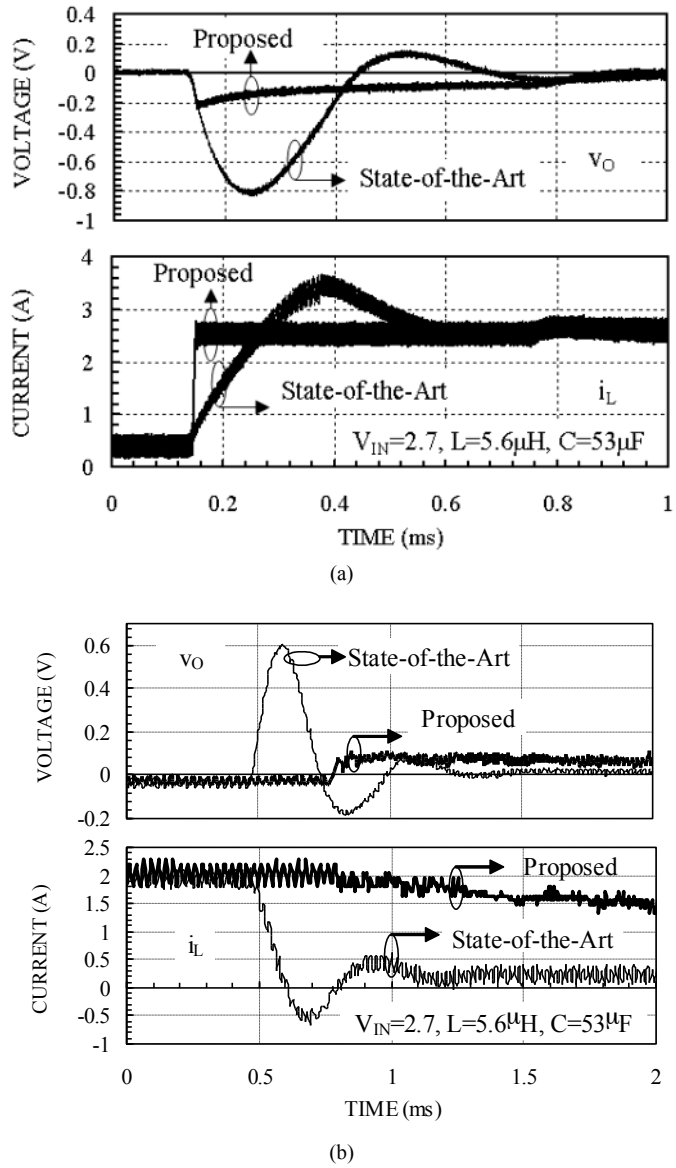


Fig. 12. Measured transient performance of the proposed dual-mode and state-of-the-art single-mode ΣΔ boost converters in response to (a) 0.1-1A and (b) 1-0.1A load steps.

Although transient-response performance for the proposed dual-mode scheme improves with decreasing L, the same is not true for the single-mode converter whose i_L response time is limited by the bandwidth of the loop, not L's slew rate. As a result, as illustrated in Fig. 15, the percentage improvement the dual-mode enjoys over its single-mode counterpart increases with decreasing L: 6- and 1.43-fold improvement at 1μH-36μF and 30μH-36μF, respectively.

Increasing C_O decreases v_O's transient droop in both converter cases, except bypass threshold voltage ΔV_{BP} effectively limits the extent to which a larger C_O decreases Δv_O in the proposed scheme. In the limit, increasing C_O to such an extent that Δv_O is less than ΔV_{BP} would prevent the bypass mode from ever engaging. As a result, the performance improvement in Δv_O is lower between the proposed and state-of-the-art solutions at higher C_O values: Δv_O for the proposed

and state of the art asymptotically converge as C_O increases.

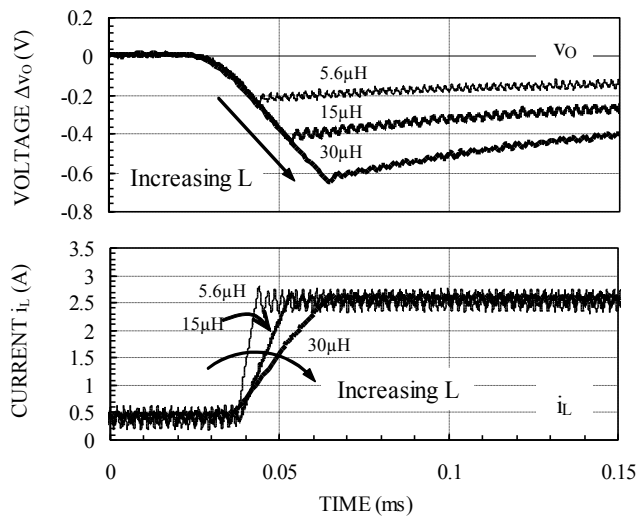


Fig. 13. Measured effects of L on the transient performance of the proposed dual-mode ΣΔ bypass boost in response to 0.1-1A load dumps, C_O=53μF.

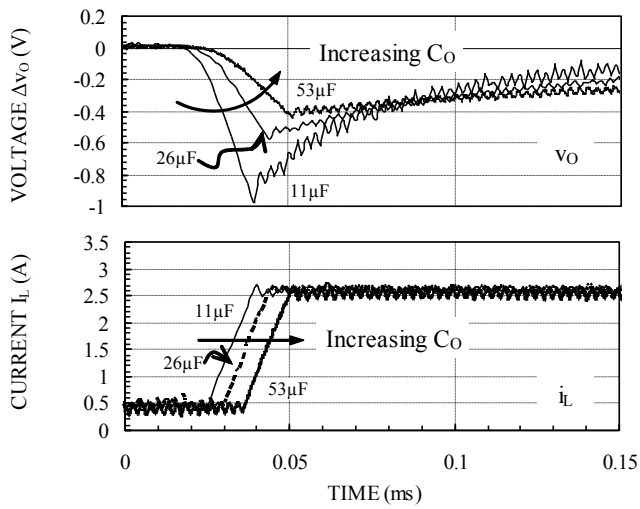


Fig. 14. Measured effects of C_O on the transient performance of the proposed dual-mode ΣΔ bypass boost converter in response to 0.1-1A load dumps.

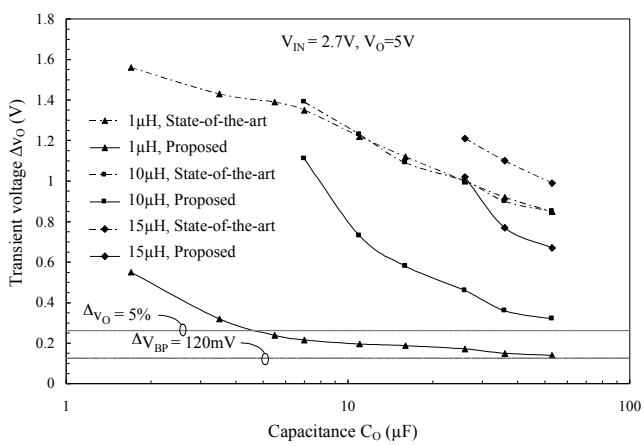


Fig. 15. Measured transient output voltage variation Δv_O under various LC combinations in response to 0.1-1A load dumps (Δi_O) for the proposed dual-mode and state-of-the-art single-mode ΣΔ converters.

D. Mode Transition

Figs. 16 and 17 illustrate how the proposed dual-mode ΣΔ bypass boost converter transitions from steady state to bypass mode and back in response to positive and negative 0.1-0.6A load dumps with an LC combination of 15μH and 53μF. As designed, the bypass mode ripple is larger at ±70mV ($\pm(H_V/2)\cdot(R_1+R_2)/(R_2A_{DV}) \approx \pm 140$mV/2) or ±1.4% than the steady-state counterpart, which is at ±15mV or ±0.3%. During a positive load dump (Fig. 16), when i_O suddenly rises, a load-induced drop in v_O exceeding the ΔV_{BP} limit engages the bypass mode and increases i_L to 2.5A (I_{PK}) in one switching cycle of S_M. As determined by offset V_{LOS}, the circuit then takes approximately 2.5ms to gradually decrease i_L back to its new target of roughly 1.3A, at which point S_A stops switching and the converter is back in steady state. During a negative load dump (Fig. 17), i_L is automatically above its target and S_A consequently starts diverting some of i_L back to V_{IN} almost immediately, until 2.5ms later, when i_L drops to its new target.

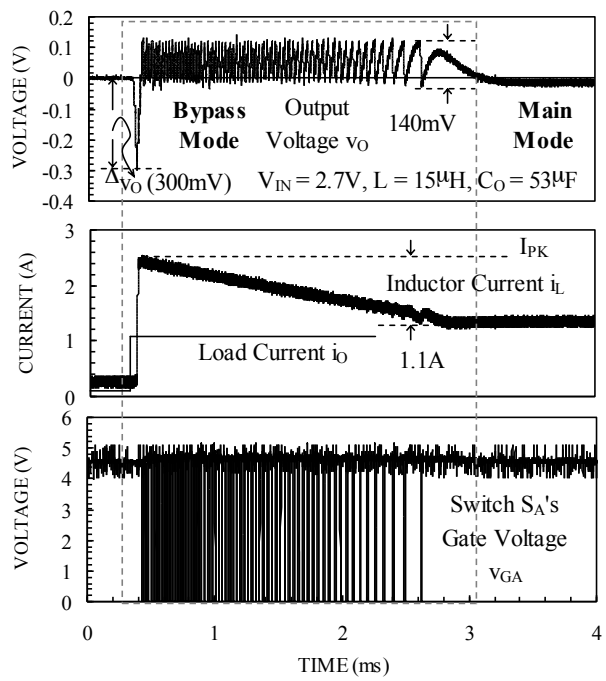


Fig. 16.Measured steady state-to-Bypass and back transitions in response to positive 0.1-0.6A load dumps (positive Δi_O).

The main drawbacks of the auxiliary bypass path are the silicon real estate, power, and switching noise associated with power switch S_A. The latter two shortcomings, however, are more often than not inconsequential because they only occur during transient events, which are typically sporadic, short, and seldom occur without significantly affecting the steady-state power efficiency (Fig. 18). The prominent disadvantage of the proposed solution is therefore additional silicon real estate for S_A because it carries substantial current. The transient-performance benefits of S_A and the bypass path that drives it, however, offset this cost.

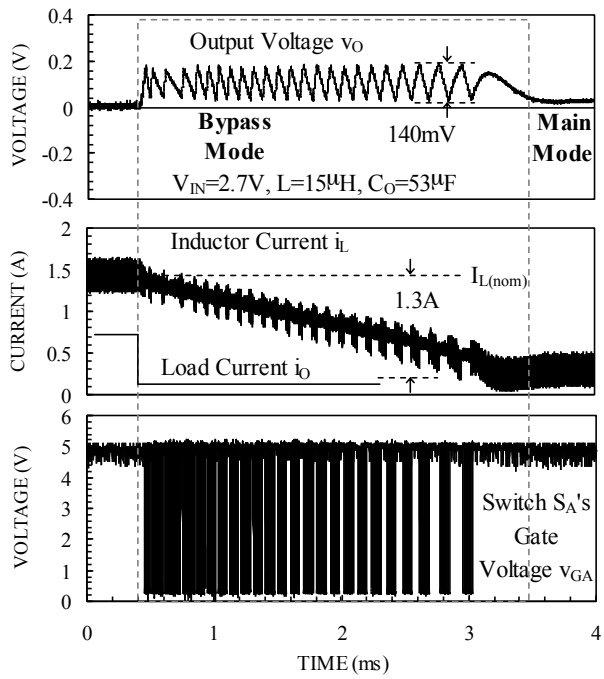


Fig. 17. Measured steady state-to-Bypass and back transitions in response to negative 0.6-0.1A load dumps (negative Δi_O).

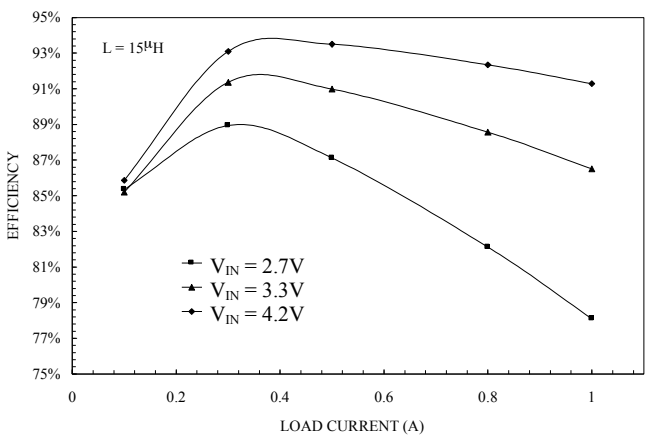


Fig. 18. Measured steady state efficiency Vs. load current I_O for the proposed converter.

V. Conclusion

A dual-mode ΣΔ bypass boost dc-dc controller 0.5μm CMOS IC that is stable for an R_{ESR}LC filter range of 0-50mΩ, 1-30μH, and 1-350μF and responds to positive and negative load dumps in one switching cycle has been proposed, designed, fabricated, and evaluated. The driving feature of the foregoing solution is a robust on-chip (i.e., smooth transitioning) ΣΔ bypass path that responds only during transient load dumps. While the converter increases inductor current i_L in one switching cycle in response to a sudden rise in load current i_O and uses it to quickly slew output capacitor C_O back to its target, it also limits how much of i_L flows to C_O in the case of a negative load dump, when i_O drops, limiting the total transient variation of output voltage v_O and therefore improving accuracy performance. The transient-response benefits of the proposed scheme, as compared to state-of-the-art single-mode ΣΔ converters, are highest at low values of L (e.g., 6x at 1μH and 1.41x or 40% improvement at 30μH) because L limits how fast i_L rises and falls to its targets. The main drawback of the proposed technique is the additional silicon real estate required for auxiliary power switch S_A, which is partially (and often completely) offset by its improved accuracy performance. In summary, the proposed dual-mode ΣΔ bypass boost converter is fast, widely LC compliant (robust), and easily implementable.

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