Title: Single-Inductor Fuel Cell–Li Ion Charger–Supply IC with Nested Hysteretic Control

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Abstract:

Microsystems must conform to microscale dimensions, store sufficient energy to last extended periods, and supply enough power to sustain, among others, wireless and sensor functions. Because batteries source moderate power with low energy densities, miniaturized devices benefit from deriving energy from fuel cells (FCs) and power from Li Ions, rather than relying on one source and over-sizing it to offset its deficiency. This paper presents a single-inductor, dual-input, dual-output (SIDIDO) charger-supply 0.5-µm CMOS IC with a nested hysteretic-control scheme that draws energy from a FC and conditions power to charge a Li Ion and supply a 1-V, 1-mA load. The IC dynamically adjusts to the load, charging the Li Ion with excess power from the FC during light loads and supplying power from both the FC and Li Ion otherwise. The fabricated prototype regulated its output to 1 V within 2.5% and responded to rising and falling 0.1–1-mA load dumps within 30 µs and 50 mV. The efficiency peaked at 32% because the load was low and the converter operated in continuous (rather than in discontinuous) conduction and sensed its inductor current via lossy sense resistors (instead of sense FETs) to manage risk and validate functionality.

Index Terms:

Single inductor, hybrid source, switching converter IC, fuel cell, hysteretic control.

I. Battery-Powered Microsystems

Advances in silicon and MEMS technologies are paving the way for smart, non-intrusive, and battery-powered microscale devices, such as wireless microsensors, whose impact on military, space, industrial, and biomedical applications [1]–[3] is to increase functionality (e.g., monitoring), improve performance (with dynamic control), and lower energy use (with *in-situ* intelligence). Powering these systems under such space constraints is challenging because batteries do not supply sufficient energy to last the lifetime demanded of them and fuel cells (FCs), atomic batteries, and harvesters do not source enough power to enable critical functions like telemetry and sensor-interface blocks. What is more, these devices must mode-hop between idle and other states to conserve energy, requiring their supplies to adjust and source diverse load levels [4]–[5].

1. Hybrid Sources

Power and energy densities do not correlate in microscale sources. Nuclear batteries and FCs, for example, are energy dense

but supply little power when compared to other equally sized sources [6]–[8]. In other words, these technologies outlast others when they supply little power but quickly outlive their usefulness when loaded beyond their capacities. In contrast, Li-Ion batteries store less energy but produce higher power, that is, source higher energy when supplying higher power under equivalent space constraints. However, over-sizing the battery (or FC) to meet energy (or power) demands is not functionally efficient in microscale applications. As a result, mixing complementary technologies like FCs and Li Ions offers a considerable advantage in size [9], which is why research in this area (as in portable [10] and wireless sensors [11]) is ongoing. Micromachined FCs, besides being small and storing 10× more energy than Li Ions, are low cost and dispel environment-friendly emissions [12]–[13]. Co-fabricating them with their conditioning and loading microelectronics also reduces footprint requirements and, as a result, improves signal integrity, now that connections are shorter and parasitic resistances and capacitances smaller [14]. FCs are also slow to respond, which is another reason for complementing them with Li Ions. In fact, having a Li Ion supply the system's burst load and allowing a FC to source the average power is a way of optimizing the tradeoff between integration and lifetime [15].

2. Multiple-Input Supply Circuits

Managing multiple sources means transferring and mixing energy and power between several inputs. In the case of a Li Ion, the battery is both an input when supplying power and an output when receiving charge from the system. Integration complicates matters because efficient supplies require μH power inductors, which are difficult to fabricate on chip. Co-packing one 2 mm × 2 mm × 1 mm off-chip inductor is possible and practical, but not more than one, which excludes transformer solutions [16]–[18].

Arbitrarily time-multiplexing a single inductor to manage multiple sources and loads is not optimal because the FC, for instance, would not be able to supply high power and, although the Li Ion could sustain low power levels, the Li Ion would not last as long as the FC. The single-inductor, dual-input converters in [19]–[20], for example, forego compensating for battery non-idealities in favor of accommodating for a possibly disconnected dc source and an intermittent harvester. Ultimately, combining microscale sources to extend life and reduce size force the system to manage and direct energy and power according to the state of its loads, the functionality of which is largely absent in the state of the art.

The single-inductor, dual-input, dual-output (SIDIDO) FC-Li Ion charger-supply first conceptually introduced in [21] and briefly evaluated in [22] employs nested hysteretic loops to navigate through two operating modes according to the state of its load. This paper expands that discussion by detailing the circuit and evaluating the operation and performance of the prototyped 0.5-μm CMOS IC. To that end, Section II overviews the system's energy-flow paths and corresponding feedback control. Sections III and IV discuss the design of the transistor-level circuits and the experimental results obtained and Section V draws conclusions.

II. Proposed Fuel Cell-Li Ion Charger-Supply System

The objective of the proposed system is to draw the optimum amount of power the FC can supply for its size from the FC and channel all or a fraction of it to the load, using the excess to recharge a battery. The system designer therefore allocates just enough FC area to supply the average power needed by the system, tank space for the fuel to last the lifetime needed, and package volume for the Li Ion to ably source power bursts. The system must consequently transfer energy from the FC to both the load and the Li Ion and from the Li Ion to the load. As a result, the converter (with one inductor only) must boost a FC's 0.5 – 0.7 V to a Li Ion's 2.7 – 4.2 V (via the FC-Li Ion path in Fig. 1) and a load at possibly 1 V (via the FC-load path) [23] and buck a Li Ion's 2.7 – 4.2 V to a load at 1 V (via the Li Ion-load path).

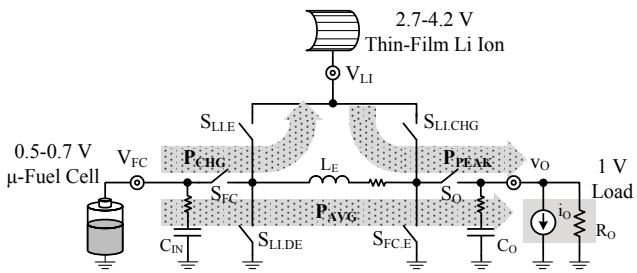


Fig. 1 Energy-flow (path) diagram of the proposed power stage

Note that eliminating the FC-load path (and allowing the Li Ion to supply all load levels) is possible but not optimal because (*i*) the FC outlasts the Li Ion during light loads and (*ii*) the converter incurs more power losses when conditioning FC power to charge the Li Ion and Li-Ion power to supply the load. The integrated switches of the converter therefore energize inductor L_E from either the FC or the Li Ion and subsequently de-energize it into either the load or Li Ion via separate and alternating energy-flow paths, according to the needs of the load.

1. Power Mixer

The converter regulates L_E's current i_L with hysteretic control to one of two predefined targets: I_{FC} or I_{LI}, depending on the source from which L_E draws energy. I_{FC} is sufficiently small (at 0.5 mA) to avoid stressing the FC's membrane electrode assembly beyond its rating (for overload protection) and high enough to reduce the percentage of fuel lost through the membrane as leakage (for load matching) [24]–[26]. I_{LI} is higher at 2.5 mA to supply the heavier loads that the small fuel cell cannot. In other words, L_E practically functions like a 0.5 or 2.5 mA current source. From a mechanical perspective, the FC's membrane should be just wide enough to supply the load's average needs (as I_{FC}) and the Li Ion large enough to never fully charge. If the Li Ion fully charges and i_O is zero, the charger-supply must shut down; but for proof of concept, the prototype does not include this form of protection.

During light loads, the system derives power from the FC only so the circuit regulates i_L to reference I_{FC} and average FC power P_{FC} equals $I_{FC}V_{FC}$. Because P_{FC} exceeds output power P_O in the light-load mode (LLM), the controller partitions (i.e., time-divides) P_{FC} to supply the load and charge the Li Ion, with load level i_O determining what fraction of P_{FC} to steer into the battery. Graphically, the solid line in Fig. 2 indicates the fraction of P_{FC} delivered to the load (as load-FC ratio $r_{LD/FC}$), which equates to the fraction of time the FC supplies the load, or said differently, how often the FC connects to the load. As a result, $r_{LD/FC}$ is zero when i_O is zero (Fig. 2) so the system disconnects from the load and directs all of P_{FC} into the battery. As i_O increases, the converter raises connectivity ratio $r_{LD/FC}$ to channel an increasing fraction of P_{FC} into the load (and a decreasing share into the battery):

$$P_O\big|_{LLM} \approx r_{LD/FC}P_{FC} \approx r_{LD/FC}I_{FC}V_{FC}, \tag{1}$$

and

$$P_{LI}\big|_{LLM} \approx (1 - r_{LD/FC})P_{FC}. \tag{2}$$

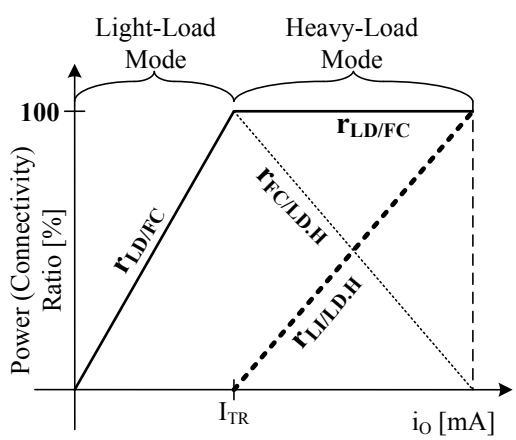


Fig. 2 Power (connectivity) ratios across load

When i_O's power P_O surpasses P_{FC} (past transition threshold I_{TR}, after $r_{LD/FC}$ reaches one), the converter enters the heavy-load mode (HLM) by augmenting P_{FC} with average Li-Ion power P_{LI}. Because the aggregate sum of average power levels P_{FC} and P_{LI} must sustain P_O in HLM, the supply draws energy more often from the battery (so average power P_{LI} increases) as i_O increases past I_{TR}. Accordingly, Li Ion-load (and connectivity) ratio $r_{LI/LD.H}$ (illustrated by the dotted line in Fig. 2) increases with i_O (as FC-load ratio $r_{FC/LD.H}$ decreases):

$$\begin{aligned} P_O\big|_{HLM} &\approx r_{LD/FC}P_{FC}\big|_{HLM} + P_{LI} = P_{FC} + P_{LI} \\ &= r_{FC/LD.H}I_{FC}V_{FC} + r_{LI/LD.H}I_{LI}V_{LI} \\ &= (1 - r_{LI/LD.H})I_{FC}V_{FC} + r_{LI/LD.H}I_{LI}V_{LI}. \end{aligned} \tag{3}$$

Raising $r_{LI/LD.H}$ decreases the FC's connectivity to the load so FC-load ratio $r_{FC/LD.H}$ is $r_{LI/LD.H}$'s complement. Notice instantaneous power $I_{LI}V_{LI}$ sets the converter's maximum output power, which happens when the converter only draws energy from the Li Ion,

when $r_{LI/LD.H}$ is one.

2. Circuit

Hysteretic comparator CMP_V in Fig. 3 senses and regulates v_O to $V_{O.REF}$ by steering what amounts to a current source (L_E) into or away from v_O at $f_{O.SW}$, the system's switching frequency. To CMP_V's feedback loop, L_E is practically a current source because comparator CMP_I regulates i_L at a switching frequency $f_{I.SW}$ that is higher than $f_{O.SW}$. Depending on the level of the load, mode comparator CMP_M dictates whether to draw i_L from the FC or both the FC and the Li Ion. R_S and $V_{I.REF}$ ultimately set i_L's regulation target to I_{FC} (when drawing energy from the FC) and I_{LI} (when deriving i_L from the Li Ion). Note I_{FC} is lower than I_{LI} because the FC cannot source the power the Li Ion can.

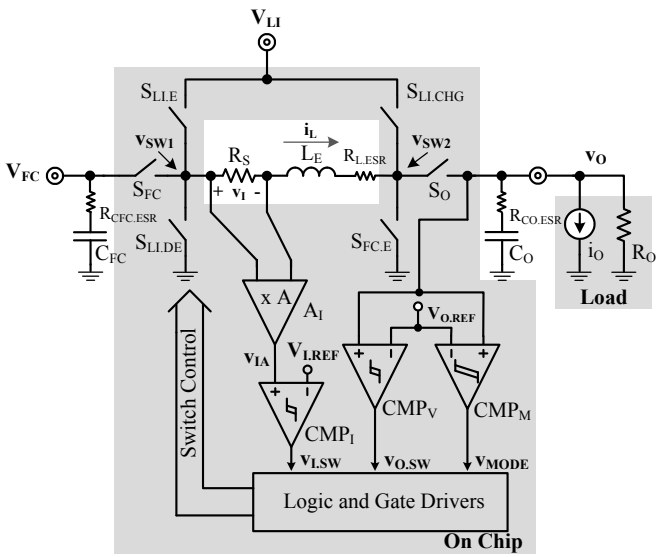


Fig. 3 System-level schematic of the proposed charger-supply system

Power Stage: In light loads, switch S_{FC} in the power stage shown in Fig. 3 remains closed and $S_{FC.E}$ energizes inductor L_E from the FC while S_O and $S_{LI.CHG}$ de-energize L_E into v_O and the Li Ion. Similarly, when heavily loaded and drawing energy from the FC, S_{FC} stays closed and $S_{FC.E}$ energizes L_E with the FC while S_O de-energizes L_E into v_O. When drawing energy from the Li Ion, S_O remains closed and $S_{LI.E}$ energizes L_E from the Li Ion and $S_{LI.DE}$ de-energizes L_E into v_O.

Hysteretic Current Control: The LC filter introduces a complex conjugate pair of poles in the frequency response that, if not properly handled, compromises the stability of the system. A conventional means of reducing the pair into a single dominant pole is to regulate inductor current i_L past the system's switching frequency $f_{O.SW}$ so that inductor L_E functions like a current source below $f_{O.SW}$ [27]. In like manner, the proposed converter uses hysteretic control to regulate i_L to I_{FC} and I_{LI} when drawing energy from the FC and the Li Ion, respectively, at a switching frequency $f_{I.SW}$ that exceeds the system's $f_{O.SW}$.

To regulate i_L, series resistor R_S senses i_L to produce v_I, amplifier A_I then amplifies v_I to generate v_{IA}, and hysteretic comparator CMP_I compares v_{IA} against current reference $V_{I.REF}$ to regulate v_{IA} within CMP_I's hysteretic window (Fig. 3). CMP_I's

output $v_{I.SW}$ then determines the connectivity of the switches, which the control logic implements. CMP_I's hysteresis and i_L's rising and falling rates (as set by L_E, V_{FC}, V_{LI}, and V_O) establish the switching frequency of the current loop ($f_{I.SW}$) and i_L's peak current $i_{L(PEAK)}$, where $f_{I.SW}$ exceeds $f_{O.SW}$ and $i_{L(PEAK)}$ falls below the FC's rated limit. CMP_I establishes the hysteresis in Fig. 4 with its inherent propagation delay. In other words, CMP_I senses when i_L surpasses target I_{FC} (when connected to the FC) and, after rising delay $t_{P.R}$ (~ 0.1 μs), its output $v_{I.SW}$ prompts the controller to end the energizing cycle, allowing i_L to peak at $I_{FC(MAX)}$. Similarly, CMP_I senses when i_L falls below I_{FC} and, after falling delay $t_{P.F}$ (~ 0.1 μs), when i_L reaches $I_{FC(MIN)}$, CMP_I trips. If $t_{P.F}$ is so long that i_L falls below zero, C_{FC} sinks the reverse current and the system continues to operate normally, provided i_L's average stays above zero. Notice that while using $t_{P.R}$ and $t_{P.F}$ to set current ripple Δi_L is not accurate, doing so establishes a small ripple, which is important to keep P_{FC} steady.

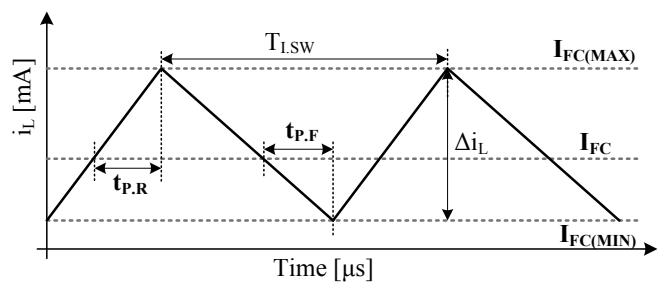


Fig. 4 Inductor current ripple through the FC-load path

Nested Hysteretic Output-Voltage Control: Each mode of operation steers inductor energy to regulate output voltage v_O to reference $V_{O.REF}$ within a hysteretic window (ΔV_O). In LLM, v_O rises to the upper window limit when the converter directs P_{FC} to v_O and droops to the lower limit when L_E disconnects (and the system charges the Li Ion). Similarly, v_O rises in HLM when the converter supplies the load with Li-Ion power P_{LI} and falls when using FC power P_{FC} (because P_{FC} is lower than P_{LI} by design). Hysteretic comparator CMP_V senses and regulates v_O to $V_{O.REF}$ within CMP_V's hysteretic window ΔV_O (Fig. 5). For that purpose, CMP_V's output $v_{O.SW}$ sets how often L_E de-energizes into v_O in LLM (as load-FC power and connectivity ratio $r_{LD/FC}$) and energizes from the Li Ion in HLM (as Li Ion-load power and connectivity ratio $r_{LI/LD.H}$).

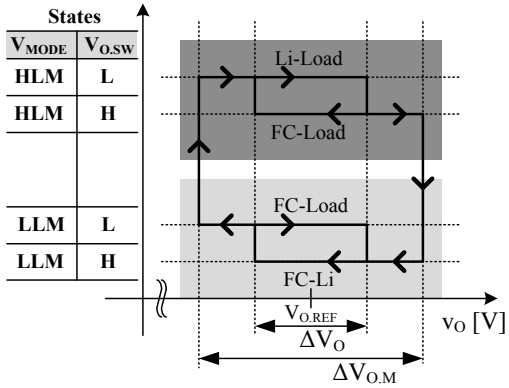


Fig. 5 The nested hysteretic windows that regulate the output in light- and heavy-load modes

With a wider hysteretic window $\Delta V_{O.M}$, CMP_M senses v_O to determine which mode of operation to assert. If P_{FC} is insufficient to satisfy the load, i_O pulls v_O to CMP_M's lower limit, prompting the converter (with v_{MODE}) to enter HLM. Conversely, when the converter sources more power than needed, the excess power pulls v_O to CMP_M's upper limit, triggering v_{MODE} to force the converter into LLM. Note v_O remains within smaller hysteretic window ΔV_O in steady state and only extends beyond ΔV_O to $\Delta V_{O.M}$ when i_O surpasses boundary limit I_{TR}, resulting in the nested hysteresis shown in Fig. 5 and v_O's response to 0.1 – 1-mA load transitions in Fig. 6.

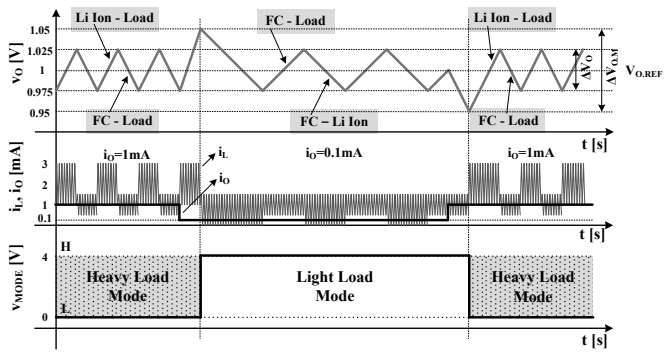


Fig. 6 Time-domain output-voltage, load-current, and mode-voltage waveforms in light- and heavy-load modes and across rising and falling load-dump transitions

<u>Switch-Control Logic</u>: CMP_I, CMP_V, and CMP_M's binary outputs $v_{I.SW}$, $v_{O.SW}$, and v_{MODE} determine the state of all the NMOS (S_{FC}, S_O, $S_{FC.E}$, $S_{LI.DE}$) and PMOS ($S_{LI.E}$, $S_{LI.CHG}$) switches in the power stage. In regulating i_L, for example, CMP_I toggles $v_{I.SW}$ up and down at $f_{I.SW}$ to energize and de-energize L_E. CMP_M and CMP_V switch at lower frequency $f_{O.SW}$ to determine from which source L_E should draw energy and to which output L_E should direct it. To this end, CMP_M transitions v_{MODE} high to place the system in LLM, which means L_E draws energy from the FC (and S_{FC} remains closed). In this mode, a low state for CMP_V's $v_{O.SW}$ prompts boost-like switches $S_{FC.E}$ and S_O to energize and de-energize L_E (at $f_{I.SW}$) from the FC into v_O. A high state similarly commands boost-like switches $S_{FC.E}$ and $S_{LI.CHG}$ to energize and direct L_E's energy (at $f_{I.SW}$) from the FC into the Li Ion. When CMP_M's v_{MODE} is low, the system enters HLM, where a low state for CMP_V's $v_{O.SW}$ prompts S_O and buck-like switches $S_{LI.E}$ and $S_{LI.DE}$ to energize and de-energize L_E (at $f_{I.SW}$) from the Li Ion into v_O. A high state here induces S_{FC} and boost-like switches $S_{FC.E}$ and S_O to energize and de-energize L_E (at $f_{I.SW}$) from the FC into v_O. Table 1 summarizes the operation just described in Boolean form.

TABLE 1. Switch-control logic equations.

Switch	Equations
S_{FC}	$v_{O.SW} + v_{MODE}$
S_O	$\left(\overline{v_{O.SW}} \cdot \overline{v_{MODE}} + v_{I.SW}\right) \cdot \left(\overline{v_{O.SW}} + \overline{v_{MODE}}\right)$

$S_{LI.E}$	$v_{I.SW} + v_{O.SW} + v_{MODE}$
$S_{FC.E}$	$(v_{O.SW} + v_{MODE}) \cdot \overline{v_{I.SW}}$
$S_{LI.CHG}$	$\overline{v_{O.SW} \cdot v_{MODE} \cdot v_{I.SW}}$
$S_{LI.DE}$	$\overline{v_{O.SW}} \cdot \overline{v_{MODE}} \cdot v_{I.SW}$

Generally, before control signals reach their respective gate terminals, an 8 kΩ-75 fF delay block and logic introduce dead time between the transitions of interconnecting switches to avoid shoot-through power. During this time, when all switches are momentarily off, body diodes conduct i_L and, in so doing, ensure L_E's conduction path is never disrupted. Once $S_{LI.E}$'s gate-control signal $G_{LI.E}$ trips low in Fig. 7, for example, $S_{LI.E}$ does not engage until after a delay after S_{FC} and $S_{LI.DE}$'s gate-control signals G_{FC} and $G_{LI.DE}$ transition low, during which time $S_{LI.DE}$'s body diode conducts.

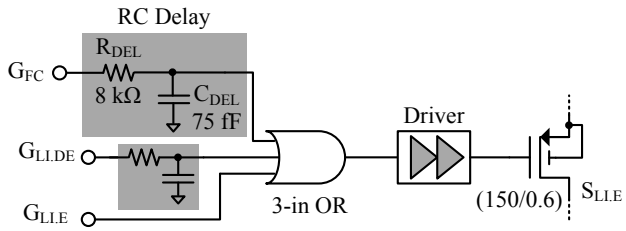


Fig. 7 Dead-time control circuit

Small-Signal Response: In LLM, when the system steers FC power P_{FC} into v_O and V_{LI}, CMP_I regulates i_L to I_{FC} at $f_{I.SW}$, so L_E is practically a $D_O I_{FC}$ current source at and below $f_{O.SW}$ (because $f_{I.SW}$ is higher than $f_{O.SW}$), where D_O is the switching duty cycle that the current loop sets for S_O. CMP_V, as a result, regulates v_O by determining how often to direct FC-derived current $D_O I_{FC}$ to v_O, as Fig. 8 shows, where CMP_V's $v_{O.SW}$ sets load-FC connectivity ratio $r_{LD/FC}$. Since V_{LI} is an unregulated low-impedance source, V_{LI} and its connectivity to L_E have no impact on the dynamics of the loop controlling v_O. Accordingly, in LLM, the MIMO system reduces to a single-input (V_{FC}), single-output (v_O) converter, where cross regulation does not apply.

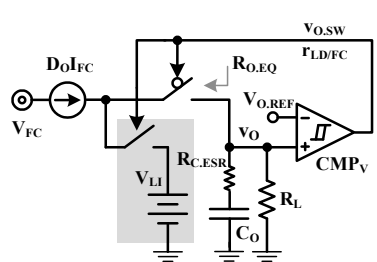


Fig. 8 Small-signal equivalent circuit in LLM

In HLM, the converter directs FC and Li-Ion power P_{FC} and P_{LI} into v_O in alternate switching cycles according to CMP_V's $v_{O.SW}$, which defines FC-load connectivity ratio $r_{FC/LD.H}$ and its complement Li Ion-load connectivity ratio $r_{LI/LD.H}$ (or $1 - r_{FC/LD.H}$).

Again, because CMP_I regulates i_L at $f_{I.SW}$ to I_{FC} or I_{LI}, depending on the source used, L_E is a current source equal to boost-equivalent $D_O I_{FC}$ in the FC cycle and buck-equivalent I_{LI} in the Li-Ion counterpart, as Fig. 9 illustrates.

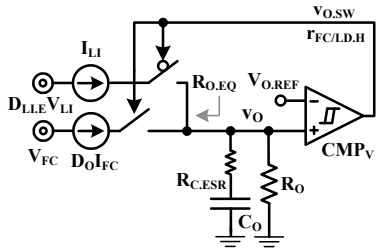


Fig. 9 Small-signal equivalent circuit in HLM

Note that boosting V_{FC} to v_O does not introduce a right-half-plane (RHP) zero like a conventional boost converter would because $r_{FC/LD.H}$ is the only control variable to v_O. The reason a RHP zero exists in boost converters in the first place is because the system modulates L_E's de-energizing duty cycle (D_O) to regulate v_O [27], and the current loop in this case switches S_O to regulate i_L to I_{FC} or I_{LI} irrespective of v_O, which means variations in v_O do not affect S_O's duty cycle D_O.

III. IC DESIGN

To validate the proposed charger-supply, an IC prototype was designed, fabricated, and tested using AMI's 0.5-µm CMOS process. As depicted in Fig. 3, power inductor L_E, fuel-cell capacitor C_{FC}, output capacitor C_O, and current-sense resistor R_S are off chip while power switches S_{FC}, $S_{LI.DE}$, $S_{LI.E}$, $S_{LI.CHG}$, $S_{FC.E}$, and S_O; logic and dead-time-control drivers; current, voltage, and mode comparators CMP_I, CMP_V, and CMP_M; current sensing amplifier A_I; and a biasing block are on chip (and supplied from Li-Ion voltage V_{LI}). Since the FC is more efficient when supplying dc current, the controller was designed to operate in continuous-conduction mode (CCM) [29]. In addition, to mitigate design risk (and noise) and concentrate on functionality, R_S senses i_L, rather than a noisier but less lossy sample-and-hold sense-FET circuit.

Power Stage: Given V_{FC} and v_O are relatively low at 0.5 – 0.7 V and 1 V, NFETs implement switches S_{FC}, S_O, $S_{LI.DE}$, and $S_{FC.E}$ (Fig. 10); PFETs implement $S_{LI.E}$ and $S_{LI.CHG}$ because they link to the highest voltage: V_{LI}. In sizing the switches, consideration for parasitic capacitances outweighed those for resistances because gate-drive losses at low power levels (below 1 mA) and higher switching frequencies (at roughly 2.5 MHz) dominate over conduction losses. As such, the aspect ratios for S_{FC}, $S_{LI.DE}$, $S_{FC.E}$, and S_O are 75/0.6 µm/µm and $S_{LI.E}$ and $S_{LI.CHG}$ are 150/0.6 µm/µm.

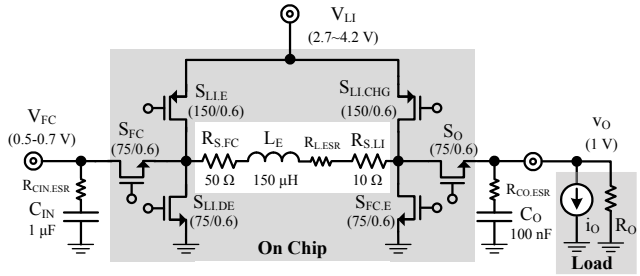


Fig. 10 Prototyped power stage

Because the FC has limited power range and response time, the circuit keeps ripple Δi_L low with a large L_E. Considering co-packaging L_E with the IC is important, L_E should also conform to a small footprint, which is why L_E is a 6.6 mm × 4.5 mm × 2.9 mm 150-μH surface-mount ferrite-core power inductor with 2 Ω of ESR. Because switching losses dominate, the design favors high L_E over low ESR because a lower ESR would only be possible with a lower L_E when constrained in volume. With L_E, V_{FC}, V_{LI}, and V_O set and CMP_I's hysteresis down to its lowest possible level, the current loop switches at roughly 2.5 MHz ($f_{I.SW}$). Δi_L is nevertheless considerable at 1 – 2 mA so the system uses a 1-μF tantalum capacitor (C_{FC}) to suppress the power variation the FC experiences on a cycle-by-cycle basis. At v_O, 100 nF (2 mm × 1 mm × 1 mm) slows v_O sufficiently to ensure $f_{I.SW}$ stays well above the system's $f_{O.SW}$. Recall that keeping v_O's regulation $f_{O.SW}$ below i_L's $f_{I.SW}$ allows the converter to perceive L_E as a current source.

Current Loop: The prototype splits current-sensing resistor R_S in Fig. 3 into $R_{S.FC}$ and $R_{S.LI}$ (and connects one or the other into A_I with M_{NFC1}-M_{NFC2} and M_{NLI1}-M_{NLI2}, as shown in Fig. 11) to ease A_I's ICMR requirements and keep noise injection low. When drawing energy from the FC, $R_{S.FC}$ remains attached to V_{FC} so $R_{S.FC}$'s terminal voltages hover at 0.5 – 0.7 V, which also means $R_{S.FC}$'s terminals do not generate switching noise for A_I to amplify. Placing $R_{S.LI}$ on the other side of L_E accomplishes similar results when deriving power from the Li Ion because $R_{S.LI}$ remains attached to v_O, keeping $R_{S.LI}$'s terminal voltages at 1 V (with a small ripple). A side benefit of splitting R_S in two is flexibility because $R_{S.FC}$ and $R_{S.LI}$ can independently and flexibly define i_L's regulation targets I_{FC} and I_{LI} with only one reference voltage $V_{I.REF}$:

$$V_{I.REF} \approx I_{FC} R_{S.FC} |A_I| = I_{LI} R_{S.LI} |A_I|, \tag{4}$$

so a 5-to-1 ratio between $R_{S.FC}$ and $R_{S.LI}$ sets I_{LI} to $5I_{FC}$. In other words, an $R_{S.FC}$ of 50 Ω, $R_{S.LI}$ of 10 Ω, A_I of –25 V/V, and $V_{I.REF}$ of 625 mV set I_{FC} and I_{LI} to 0.5 and 2.5 mA, respectively. This design flexibility was important to test the prototype fully.

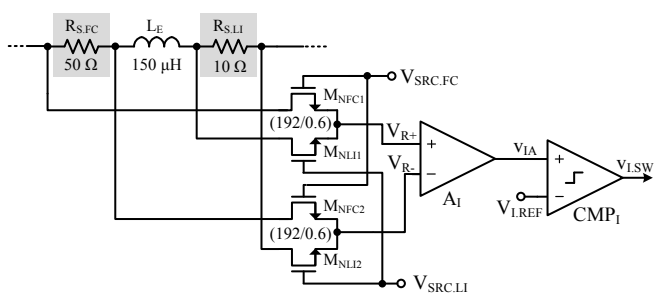


Fig. 11 Inductor current-sensing circuit

Differential amplifier A_I consists of a p-type differential pair loaded with an n-type mirror and cascaded with a Miller-compensated second stage (Fig. 12). The operational amplifier is in an inverting configuration where resistor ratio R_B/R_A sets the gain to –25 V/V. External tuning voltage V_{TUNE} connects to A_I's non-inverting input to attain a gain of one and raise A_I's output v_{IA} high enough to keep v_{IA} within the ensuing comparator's ICMR:

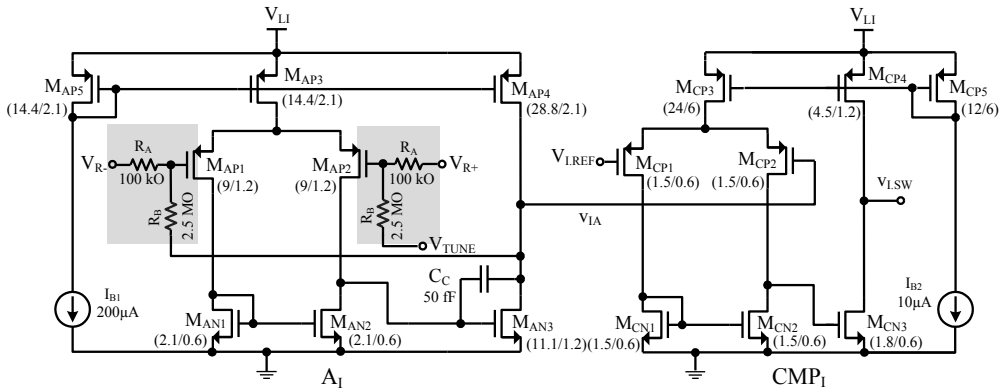
$$v_{IA} \approx (v_{R-} - v_{R+})A_I + V_{TUNE}\left(\frac{R_A}{R_A + R_B}\right)\left(\frac{R_A + R_B}{R_A}\right)$$

$$= (v_{R-} - v_{R+})\left(-\frac{R_B}{R_A}\right) + V_{TUNE}. \quad (5)$$

To follow L_E's fast changing current i_L, which switches at roughly 2.5 MHz, A_I needs 875 µA. A_I feeds a comparator (Fig. 12) whose p-type mirror-loaded input drives a common-source amplifier.

Fig. 12 Current-sense amplifier A_I and the regulating comparator it drives

Voltage Loop: Since both voltage-loop comparators CMP_V and CMP_M produce hysteresis and sense v_O, they share ICMR and bandwidth requirements, which is why their circuit topologies resemble. In particular, p-type input pairs feed a latching load whose positive feedback gain determines the circuit's hysteresis (Fig. 13). A folding class-AB gain stage follows to produce the rail-to-rail (binary-like) signal that feeds the switch-control logic. CMP_V and CMP_M only differ in that the latter produces a wider hysteretic window so CMP_M's positive feedback gain exceeds CMP_V's. As a result, mirror ratios M_{CN3}/M_{CN1} and M_{CN4}/M_{CN2} are greater in CMP_M at 2.1/1.2 µm/µm than in CMP_V at 2.1/1.65 µm/µm, producing hysteretic windows of 100 and 50 mV, respectively. Incidentally, these two nested hysteretic windows must, by design, correlate so the layout implementations of M_{CN1} – M_{CN4} must match accordingly (i.e., be close and surrounded by dummy devices in a common-centroid and cross-coupled configuration).



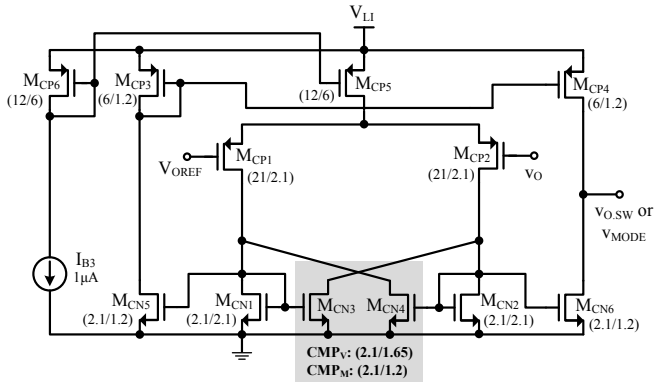


Fig. 13 Schematic for output-voltage and mode-controlling comparators CMP_V and CMP_M

Startup: When the system first starts, v_O is zero so both voltage-loop and mode comparators CMP_V and CMP_M in Fig. 3 force their respective outputs $v_{O.SW}$ and v_{MODE} to start at a low state, prompting the converter to enter HLM and to source power from the Li Ion. In this state, the circuit continually sources Li-Ion power so v_O necessarily rises. Once v_O surpasses CMP_V's upper threshold, the system downshifts to FC power. If the load exceeds this power, v_O falls to CMP_V's lower threshold and ripples about $V_{O.REF}$ in steady state (in HLM). Otherwise, if the load is light, v_O continues to rise with FC power to CMP_M's upper threshold, at which point the system enters LLM and allows CMP_V to steer FC power away from v_O until v_O reaches steady state. Although starting a power supply with its maximum-rated power is typically not advisable (because the sudden inrush of i_L may damage the power stage), power levels in this design are always low so the devices were able to accommodate all relevant power levels.

IV. Experimental Results

Fig. 14 shows the die photograph of the 0.5-µm CMOS (AMI) IC fabricated and its accompanying printed-circuit-board (PCB) prototype. The die occupied 1.0 mm × 0.5 mm of silicon area with the power devices using roughly 12%. To focus on proof of concept, the IC did not include short-circuit protection or battery-charging functions and two external supplies at 0.5 – 0.7 V and 2.7 – 4.2 V emulated the FC and the Li Ion, respectively.

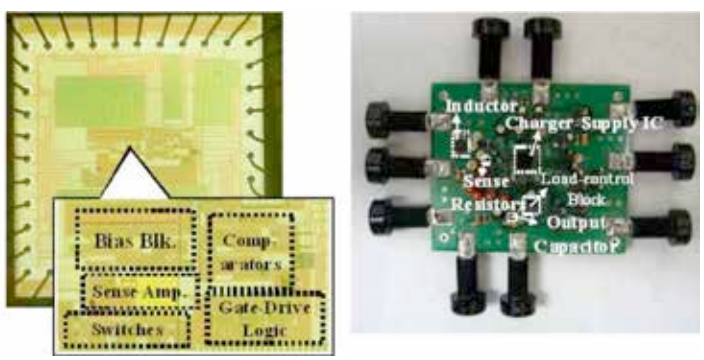


Fig. 14. 0.5-µm CMOS IC die photograph and corresponding PCB.

1. Operation

Current Regulation: Fig. 15a-c shows that the converter switches at roughly 2.5 MHz ($f_{I.SW}$) to regulate i_L through all energy-flow paths. When drawing energy from the FC and directing it to v_O, i_L ripples at 1 ± 0.5 mA, and when channeling current into the Li Ion, i_L ripples at 0.25 ± 0.75 mA, off its 1 ± 0.5 mA target. The reason for the disparity is i_L's falling rate when connected to the Li Ion is faster at $(V_{FC} - V_{LI})/L_E$ than its counterpart at $(V_{FC} - V_O)/L_E$ (when attached to the load) so the propagation delay across CMP_I produces a larger hysteresis (and offset) for the faster rate. This is a drawback because the momentary negative current that results (which peaks at –0.5 mA) discharges the battery. When steering power from the Li Ion

into v_O, i_L ripples at 2 ± 1 mA, which is slightly off its 2.5 ± 1-mA mark because of, again, delay mismatches. Since Fig. 16 demonstrates v_O is stable, integrated substrate and signal-propagation noise through the IC and PCB probably accounts for the ringing in the Li Ion-load path's i_L in Fig. 15c. Fig. 15d further illustrates the converter in dual-output mode (in LLM) as it switches from supplying the load at 1 ± 0.5 mA to charging the battery at 0.25 ± 0.75 mA. (These waveforms were extracted from $R_{S.FC}$ and $R_{S.LI}$'s terminal voltages.)

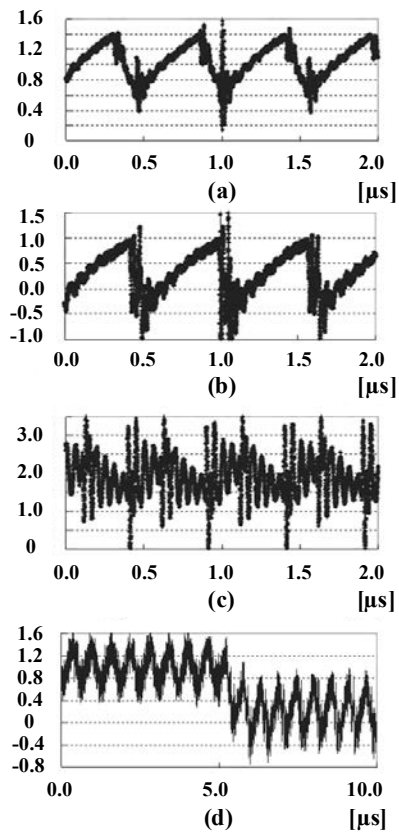


Fig. 15 Measured inductor-current waveforms through the (a) FC-load (b) FC-Li Ion, and (c) Li Ion-load energy-flow paths and (d) while transitioning from the FC-load to FC-Li Ion paths in dual-output mode (in LLM)

Voltage Regulation: The prototype regulates v_O within ±25 mV of its target (1 V) with CMP_V in both LLM when i_O is 0.1 mA and HLM when i_O steadies at 1 mA (Fig. 16, Table 2). Since CMP_M's v_{MODE} determines the converter's mode, a high state indicates the system is in LLM and a low state in HLM. In LLM, the light load discharges C_O slowly so v_O ripples at about 11 kHz. In HLM, the higher i_O discharges C_O faster so v_O ripples at 50 kHz, well below $f_{I.SW}$.

TABLE 2. IC performance summary.

Parameter	Value
Process	AMI 0.5 µm CMOS
Die Area	1.0 x 0.5 mm^2 (342 transistors)

Open-Circuit Fuel-Cell Voltage V_{FC}		0.5 – 0.7 V
Li-Ion Battery Voltage V_{LI}		2.7 – 4.2 V
i_L's Switching Frequency $f_{I.SW}$ +		2.5 MHz (nominally)
v_O's Switching Frequency $f_{O.SW}$ +		11 kHz (LLM) , 50 kHz (HLM)
Output Voltage v_O (and Δv_O) +		1 V ± 25 mV (±2.5 %)
v_O's 0.1 → 1 mA Load-Dump Response +		–50 mV (20 μs)
v_O's 1 → 0.1 mA Load-Dump Response +		+60 mV (30 μs)
Supply Power P_{DD} at 4 V	A_I *	3.5 mW
	CMP_I *	242.8 μW
	CMP_V & CMP_M *	28.8 μW
	Current Bias *	133.1 μW
	Control Logic *	1.0 nW
	Gate Drive	1.1 mW
	Total +	5.0 mW

+ Measured * Simulated

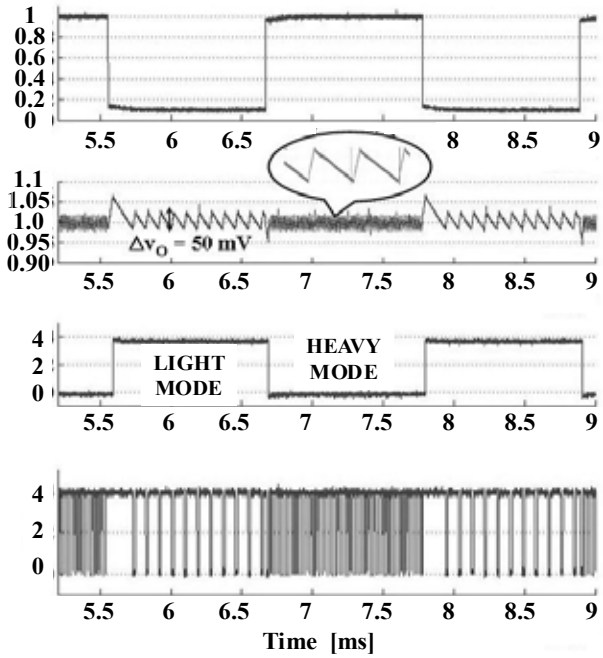


Fig. 16 Measured output, mode, and path-control voltages in light- and heavy-load modes and across rising and falling loads

During a rising load dump, when i_O suddenly increases from 0.1 to 1 mA, v_O falls to 0.95 V (CMP_M's lower threshold), prompting the system to enter HLM and source Li-Ion power (Fig. 17). Similarly, in response to a falling load dump from 1 to

0.1 mA, the converter sources more power than needed and v_O rises to 1.06 V, pushing the converter into LLM, where it draws FC power to both supply the load and charge the Li Ion. These single-cycle response times t_{LH} and t_{HL} (being only functions of i_O, C_O, and CMP_M's delay) are generally faster than those of PWM-based converters, which typically require several switching cycles to recover from severe load dumps [30]. CMP_M's asymmetrical delay, incidentally, accounts for the slight difference between CMP_M's measured (1.06 V) and expected upper threshold (1.05 V), which represents 1% of V_O. Overall, the system regulates v_O within 2.5% (±25 mV) of its target in steady state and within +6% and –5% (+60 and –50 mV) when subjected to load dumps. The results also show the prototype transitions between LLM and HLM automatically and seamlessly, indicating feedback control is reliable and stable.

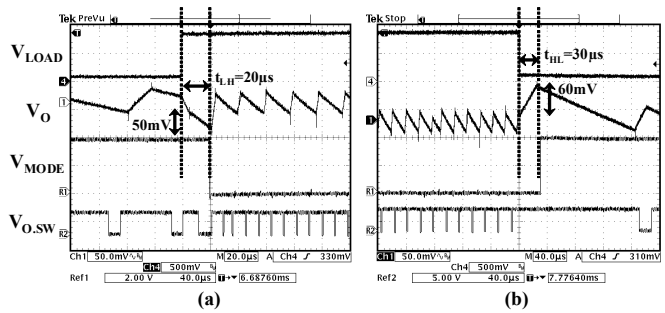


Fig. 17 Measured close-ups of the output when subjected to (a) rising and (b) falling load dumps

2. Efficiency

To understand and decouple the power losses in the system, a separate source (V_{DD}) supplied the controller (i.e., the IC) in these experiments. To this end, Fig. 18 shows the simulated input power that the battery and V_{DD} supply as P_{LI} and P_{DD} along with output power P_O and conduction losses P_C up to 10 mA, well above the target of 1 mA. (Fig. 18 shows simulation results because decoupling and measuring conduction losses are difficult in practice.) P_{DD}, which represents quiescent and switching gate-drive losses, is constant across the entire range and dominant below 3 mA because quiescent power and i_L's switching frequency f_{LSW} are independent of i_O (by design) and v_O's switching frequency in HLM is constant at 50 kHz. P_C's contribution and related voltage drops are negligible below 1 mA (because $P_C \propto i_O^2$), which means conduction power is less important than quiescent and switching losses in the targeted load range.

Fig. 19 shows the measured and simulated efficiency results of the converter in LLM (below 0.35 mA) and HLM (above 0.35 mA). While efficiency in LLM (η_{LLM}) is the ratio of the power that reaches v_O (P_O) and charges the battery (P_{CHG}) to the power the FC and V_{DD} deliver:

$$\eta_{LLM} = \frac{P_O + P_{CHG}}{P_{FC} + P_{DD}} = \frac{P_O + P_{CHG}}{I_{FC}V_{FC} + P_{DD}}, \tag{6}$$

HLM efficiency η_{HLM} is the ratio of P_O to the power the FC, the battery, and V_{DD} deliver on average as $r_{FC/LD.H}I_{FC}V_{FC}$, $(1 - r_{FC/LD.H})I_{LI}V_{LI}$, and P_{DD}, respectively:

$$\eta_{HLM} = \frac{P_O}{r_{FC/LD.H}I_{FC}V_{FC} + (1 - r_{FC/LD.H})I_{LI}V_{LI} + P_{DD}}. \tag{7}$$

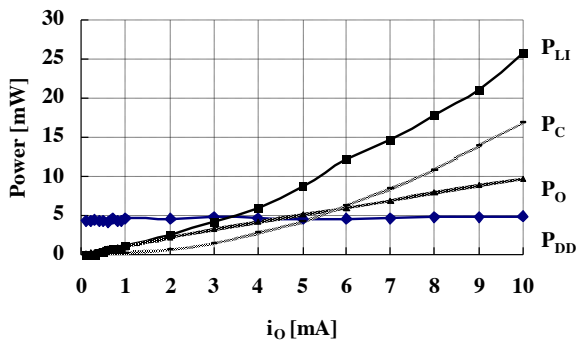


Fig. 18 Simulated Li Ion-, supply-, output- and conduction-power levels across load

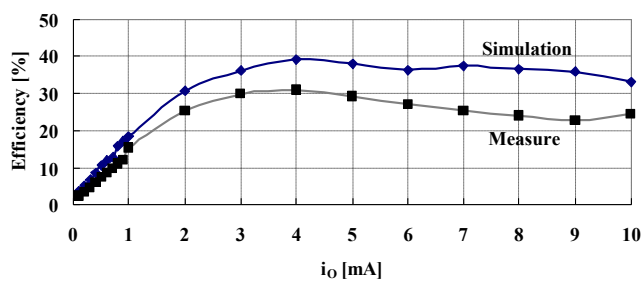


Fig. 19 Simulated and measured efficiency performance across load

Experimentally, power losses balance at 4 mA (in HLM), where efficiency peaks at 32%, and as i_O decreases to 0.35 mA, when the converter starts to recharge the battery, efficiency falls below 7%. Efficiency is relatively low because the effects of quiescent and switching losses (P_{DD}) in this region are profound. The design also favored flexibility and testability over converter efficiency to validate functionality (as proof of concept), choosing to operate in CCM for the sake of the FC and sense i_L with lossy sense resistors $R_{S.FC}$ and $R_{S.LI}$ (so P_{DD} exceeds P_{FC}). The efficiency simulated is generally higher than the one measured because the ringing currents observed in Fig. 15c dissipate additional power.

While $R_{S.FC}$ and $R_{S.LI}$ increase power losses by about 0.5% in LLM and 3.6% in HLM, the impact of current-sense amplifier A_I (which operates continuously) is worse at 3.5 mW (of the total 5 mW reported in Table 2). Replacing $R_{S.FC}$ and $R_{S.LI}$ with sample-and-hold sense FETs [31] would decrease conduction losses and, more importantly, eliminate the need for A_I, improving efficiency considerably, even if the sense FETs generate switching noise. Additionally, allowing L_E to conduct discontinuously (in DCM) reduces switching losses [17]–[18] and the time that the current-sensing network is operational, which combined should advantageously offset the conduction losses a higher peak current ($i_{L(PEAK)}$) would incur. Another benefit of DCM is that

L_E can be smaller, which is better for integration. Forcing DCM operation with multiple inputs and outputs is not straightforward, however, especially considering pseudo-DCM techniques are often inefficient [32] and FC peak power would have to increase.

3. Discussion

The significance of the results presented and the paper's main contribution is the functionality achieved with only one inductor. In other words, what is important is how the proposed MIMOSI switching converter optimally and automatically adjusts according to load level to draw and mix power to supply a 1-V load accurately [23] (within ±2.5%, under steady-state conditions) and respond quickly to fast load dumps [33] (within 20 – 30 μs) from the more appropriate of two complementary sources. Selecting the best source from which to draw energy in this way, albeit with a more efficient current-sensing method, would decrease the size requirements of portable devices further than the state of the art [19], [34], because 0.5 – 0.7-V FCs [15], for example, store more energy per unit volume than 2.7 – 4.2-V Li Ions and Li Ions supply more power per unit volume than FCs. Key to this achievement are the nested hysteretic loops, which regulate i_L and v_O and ensure the system transitions smoothly across operating modes with less than 60 mV of variation. Time-multiplexing L_E is an important feature because microsystems cannot co-package more power inductors, since on-chip inductors do not offer the inductance, ESR, and peak currents that their small off-chip counterparts can.

V. Conclusions

A single-inductor Fuel Cell-Li Ion charger-supply 0.5-μm CMOS IC with nested hysteretic loops was designed, fabricated, and tested. The prototype built regulates its output to 1 V within ±25 mV with 150 μH, 100 nF, and 1 μF of off-chip inductance and output and fuel-cell capacitance and responds to rising and falling load dumps of 0.1 – 1 mA without surpassing a +60/–50-mV window. Although the design favors testability over efficiency (peaking at 32%) to validate functionality, forcing the converter to operate in DCM and sensing the inductor current indirectly with sense FETs should reduce switching and quiescent power losses considerably, which are critical at these power levels. What is important to recognize is that the prototype's intelligent, load-dependent, and dynamically adaptive feedback control automatically selects the optimum source from which to derive power to supply a load, and when conditions permit, charge a Li Ion. Managing a miniaturized FC-Li Ion combination in this way appeals especially to microscale applications because the hybrid supply is able to complement the power-energy faults of its technologies to maximally extend the life of an otherwise easily exhaustible miniaturized source.

VI. Acknowledgment

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