A Compact 1–30µH, 1–350µF, 5–50mΩ ESR Compliant, 1.5% Accurate 0.6µm CMOS Differential ΣΔ Boost DC–DC Converter

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Abstract—Emerging high-end portable electronics demand on-chip integration of high-performance dc-dc power supplies not only to save pin count, printed circuit board (PCB) real estate, and the cost of off-chip components but also to better regulate the point of load (PoL). In the face of a widely variable LC filter, however, integrating the frequency-compensation circuit is difficult without sacrificing stability performance, which is why integrated controller ICs only cater to relatively narrow LC ranges. While ΣΔ control addresses this LC compliance issue in buck dc-dc converters with high equivalent series resistance (ESR) output capacitors, it is not clear how it applies to ΣΔ boost converters. To that end, this paper discusses, analyzes, and experimentally evaluates a prototyped 0.6µm CMOS differential ΣΔ boost converter. Experimental results verified the switching supply was stable across 1-30µH, 1-350µF, and 5-50mΩ of inductance, capacitance, and ESR while keeping output voltage variations in response to 0.1-0.8A load and 2.7-4.2V line changes to less than ±1.5%, peak efficiency at 95%, and switching frequency variation to less than 27%.

Index Terms—differential ΣΔ control, boost dc-dc converter

I. INTRODUCTION

INTEGRATING dc-dc power supplies on chip reduces pin count, printed circuit board (PCB) space, off-chip components, design complexity, and time to market, in other words, cost and form factor. The frequency-compensation circuit, however, is difficult to integrate without limiting the LC filter range for which the converter is stable [1]. This design constraint is severe in converters targeted for a wide application space where nominal off-chip LC values already span a substantial range without the widening effects of process tolerance and operating temperatures. Even in niche applications where the LC filter is on chip or in package, compact multiple input-output converters often change topology and LC filter combination dynamically to accommodate a diverse loading environment, changing the LC values for which the converter is to remain stable [2].

Buck dc-dc converters implementing ΣΔ control [3-6] often enjoy wide LC compliance but only when the output capacitor has sufficient equivalent series resistance (ESR) for its voltage to overwhelm that of the intrinsic capacitor. As a result, the ESR voltage mostly sets the terminal voltage of the capacitor, impressing the inductor ripple current information on the output voltage and achieving current-mode-like control. Reported literature on boost ΣΔ converters, the other hand, focuses on fixed LC filter applications [7-8], largely circumventing and therefore ignoring wide LC variations.

In addition to LC compliance, steady-state accuracy demands high-frequency operation [8], which in on-chip converters, translates to considerable noise content, especially when subjected to relatively high load currents. Despite the well-known advantages of differential-mode circuits in rejecting noise, the added circuit complexity, silicon real estate, and power demands over their single-ended counterparts often prohibit their effective use. As a result, ΣΔ controllers in literature are single-ended structures limited to lower switching frequencies or lower output power capabilities.

This paper discusses, intuitively analyzes, and experimentally evaluates the design of a 0.6µm CMOS differential ΣΔ boost switching supply aimed at extending LC filter compliance and increasing on-chip noise immunity. After a discussion on the operation of ΣΔ controllers and their system-level design implications in Section II, Section III introduces and discusses the system architecture and IC design details of the proposed strategy. Section IV then presents and evaluates the experimental results obtained and Section V draws relevant conclusions.

II. ΣΔ CONTROL IN BOOST CONVERTERS

A. Circuit

Unlike buck converters, the inductor current ripple in boost converters (Fig. 1) does not completely flow to the output capacitor. This is because during the on time of switch MN, the inductor is disconnected from the output by reverse-biased diode D. Because the output voltage does not reflect the behavior of the inductor current, as in buck converters with non-negligible ESRs, ΣΔ control in boost converters cannot rely on output voltage alone. Instead, the inductor current must also be sensed and mixed with the output voltage in the negative feedback loop to achieve current-mode-like control.
characteristics. A hysteretic comparator then modulates the frequency and duty cycle of switch MN based on how the scaled sum (V_{SUM}) of the ripples (scaled by \(g_{mi}R_s\) and \(g_{mv}R_s\)) compares against a user-defined hysteresis window. While the output voltage is compared to an independent dc reference, the inductor current, whose dc value changes with load, is self-referenced against its own average value.

The current loop is actually an inner loop for the voltage loop (Fig. 2(c)). As such, the current loop must first be stable and its closed-loop form used to determine the stability conditions of the voltage loop. One peculiarity of the boost converter is that the outer loop extracts two signals from the inner loop, as the diode current is the product of inductor current \(i_L\) and off duty cycle \(d_{m}'\), which is a signal-flow way of describing \(z_{RHP}\) and why Fig. 2(c) extracts two feed-forward closed-loop signals (e.g., \(i_{ldm_{cl}}\) and \(i_{ldc}\)) to output \(V_o\).

The gain across the current loop is the product of the gains across the low-pass filter (LPF) and accompanying \(R_{gmi}R_s\) combination, modulator gain \(M\), and switch-inductor MN-L combination. Under dc conditions, the sensed inductor current \(i_{R_i}\) equals its self-reference \(v_{\text{REF}}\), giving a zero at the origin because the difference between the two is zero, but the difference increases with frequency as the output \(v_{\text{REF}}\) of the LPF is shunted to ground. Beyond the filter pole \(p_{LPF}\), however, \(v_{\text{REF}}\) has negligible ac signals and the loop gain levels.

The small-signal gain across switch-inductor MN-L (\(G_i\)) is the ratio of small-signal inductor current \(i_L\) and duty cycle \(d_{m}\) which results from applying dc output voltage \(V_o\) (variations in \(V_o\) are negligible at high-frequency) across inductor impedance \(L_s\) during the fraction of time MN is off (off duty cycle \(d_{m}'\) or \(1-d_{m}\) or its small-signal equivalent -\(d_{m}\)):

\[
G_i \bigg|_{p_{LPF}} = \frac{i_L}{d_m} = \frac{V_{in} \cdot v_{ph}}{L_s d_m} = \frac{0 - (d_m V_o)}{L_s d_m} = \frac{V_o}{L_s},
\]

where the lower-case and capital subscripts indicate ac and dc quantities, respectively. Thus, the current loop gain \(|LG_i|\) at frequencies past LPF \(p_{LPF}\) and LC poles \(p_{LC}\) is:

\[
|LG_i|_{f>p_{LPF}} = \left| \frac{V_{SUM}}{i_{L}} \right| \left| \frac{d_{m}}{V_{SUM}} \right| = \left| R_{gmi}R_s \right| M \left| \frac{V_o}{L_s} \right|
\]

Hence, at high frequencies, \(G_i\) has a single pole response (Fig. 2(a)) and is therefore stable. Its unity-gain frequency \((f_{0\text{dB}})\) largely sets the switching frequency of MN at

\[
f_{0\text{dB}} = \frac{R_{gmi}R_s MV_o}{2nL_s}.
\]

The compensated loop gain of the voltage loop (\(|LG_v|\)) is the product (Fig. 2(c)) of the gains across transconductor \(g_{mv}\), the closed-loop current gain \(A_{1CL}\) of the current loop from \(i_{mv}\) to diode current \(i_d\), and the load impedance \(Z_o\). The latter is a parallel combination of output capacitive impedance \(1/sC_o\) and output resistance \(R_o\). Diode current \(i_d\) is the product of \(i_L\) and \(d_{m}'\) so its linearized small-signal counterpart varies with both \(i_L\) and \(d_{m}\):

\[
i_d = i_L \left( \frac{\partial i_L}{\partial i_L} \right) + d_{m}' \left( \frac{\partial i_L}{\partial d_{m}} \right) = i_L D_{M}' + d_d mL_L,
\]

where \(D_{M}'\) and \(L_L\) are the dc off duty cycle (1-D_{m}') and inductor current, respectively, the latter of which is equivalent to \(I_o/D_{M}'\) or \(I_o/(1-D_{m}')\). Note the feed-forward component is \(d_d mL_L\), which is out of phase with \(i_d\) (Fig. 2(c)).

Because two current-loop current components \(i_d D_{M}'\) and \(d_d mL_L\) are fed to \(Z_o\) (Fig. 2(c)), closed-loop current gain \(A_{1CL}\) (from \(i_{mv}\) to \(i_d\)) is comprised of the closed-loop gain to \(i_L\) and \(d_m\) and their translation to \(i_d\):

Fig. 1. Simplified schematic of current and voltage mixing in a \(\Sigma\Delta\) boost converter.

Fig. 2. High frequency Bode magnitude plots of the (a) current and (b) voltage loops in a \(\Sigma\Delta\) boost converter, and (c) equivalent control diagram highlighting the current loop, an inner closed-loop gain for the overall voltage loop.

B. Controller Design Requirements

1) Stability: The variation of the poles and zeros that depend on the output filter limits the \(R_{ESR}L_s\) space for which the \(\Sigma\Delta\) controller is stable. To be more specific, LC values in a boost converter produce (Uncompensated \(LG_v\) in Fig. 2(b)) a pair of complex-conjugate poles (\(p_{LC}\)) and a right half-plane (RHP) zero (\(z_{RHP}\)) and the capacitor and its ESR a left half-plane zero (\(z_{ESR}\)). The latter typically does not reside within frequencies of interest intentionally because larger ESR values increase the output ripple voltage [9]. While an increase in the on time of switch MN increases the energy stored in the inductor and subsequently the output voltage, disconnecting the output to do so allows the output voltage to droop, opposing the ultimate effect of increasing MN’s on time. This opposing effect amounts to an out-of-phase, feed-forward path in the voltage loop from the gate of switch MN to the output (\(Z_{RHP}\)).

The open-loop \(LG_v\) is uncompenated (Fig. 2(c)) and its frequency response is characterized by a single pole at the gain crossover frequency of \(f_{0\text{dB}}\).
the response of the system and degrades transient response [10].

2) Steady-State Error and Ripple: When including the effects
of switching and propagation delays, the sum (\(v_{SUM}\)) of
the current and voltage ripples extends beyond the limits
established by the hysteretic window of the comparator (Fig.
1). For switch duty-cycles away from the symmetrical 50% val-
ues, the asymmetry in the rising and falling slopes of \(v_{SUM}\)
results in unequal positive and negative excursions of \(v_{SUM}\)
beyond the hysteresis window. This inequality introduces an
error in the average value of \(v_{SUM}\) and therefore the output
voltage, depending upon the switching delay \(t_d\) and the
magnitude and asymmetry (duty-cycle) of the \(v_{SUM}\) ripple
slopes. Assuming that \(g_{mi}\) is significantly greater than \(g_{mv}\)
at the switching frequency, [11] shows that this steady-state error is

\[
v_{err} = V_{REF} - V_O = \left(\frac{g_{mi,fw}}{g_{mv,dc}}\right) \left(\frac{t_d}{2L}\right) (V_O - 2V_{IN}),
\]

where \(g_{mi,fw}\) and \(g_{mv,dc}\) are values of \(g_{mi}\) and \(g_{mv}\) at
the switching frequency and dc respectively. Equation (14)
suggests a small switching-frequency value of \(g_{mi}\) and a large
dc value of \(g_{mv}\) for low steady-state error. The error is the
worst at the smallest inductor value in a variable LC
environment. The switching ripple is inversely dependent
on the output capacitance and switching frequency, which, for
a well-designed converter, is approximately equal to \(f_{DBH}\).

3) Switching Frequency Variations: As stated earlier, the
switching frequency of the system \(f_{SW}\) is set by the unity-
gain frequency of the current loop \(f_{DBH}\), which is directly
proportional to \(V_O\) and gain constant \(R_{gmi}R_cM\), and inversely
proportional to \(L\). Other parameters remaining constant,
the switching frequency therefore depends on \(M\) showing a
parabolic variation that peaks when \(D_M\) and \(D_M'\) are equal at
50% duty-cycle. From a time-domain perspective, however,
the minimum propagation delay across comparator \(M\) and
other switching delays set the maximum switching frequency of
the system. As a result, arbitrarily increasing gain \(R_{Gmi}\) to
keep \(f_{DBH}\) below \(f_{RHP}\) and therefore increase LC compliance
frequencies \(f_{SW}\) \((f_{DBH}\) beyond the capabilities of \(M\). In terms of
proportionality (13), loops delays lead to excursions of the
regulated \(v_{SUM}\) ripple beyond the constraints set by the
comparator hysteresis, thus increasing the effective hysteresis
window, decreasing \(M\) and hence \(f_{DBH}\) (switching frequency).

### III. DESIGN

#### A. System Design

The main feature of the foregoing design is LC compliance
and key design parameters for stability, regulation, and
frequency performance are voltage and current gains \(g_{mv}\)
and \(R_{Gmi}\). The primary objectives of the proposed design are for
\(g_{mv}\) to exceed \(R_{Gmi}\) at low frequencies to reduce steady-state
dc errors in \(v_O\) and \(R_{Gmi}\) to exceed \(g_{mv}\) at moderate-to-high
frequencies to shift \(f_{DBH}\) \((f_{SW}\) above \(f_{DBH}\) and in the process
turn $i_l$ into a current source in the voltage loop masking the effects of the LC complex-conjugate pole pair and RHP zero. Another design goal is to make $g_{mi}$ inversely proportional to frequency below and near $f_{fmin}$ ($f_{sym}$) by means of pole $p_i$ (Fig. 3) to compensate partially for switching frequency variations, without resorting to additional frequency-regulating loops. The pole $p_i$ that constitutes a second pole in the current loop in addition to that in $G_i$, is compensated by the zero $z_i$. Fig. 3 illustrates the proposed frequency-dependent current and voltage gains $g_{mi}$ and $g_{mv}$. Table 1 describes the operating conditions and design parameters of the targeted 2.7-4.2V Li-Ion powered, 5V-0.8A output supply.

Since the feedback in the proposed $\Sigma\Delta$ controller includes high-bandwidth signals with harmonic components exceeding the switching frequency, the circuit must be tolerant to switching (supply and ground) noise, which is why a differential controller is proposed (Fig. 4). Inductor current, sensed through sense-resistor $R_i$, is amplified by amplifier $A_{DI}$ whose differential output is internally low-pass filtered through an RC filter to generate a second output, viz., self-referenced signal $V_{REF}$. The ripple in the sensed output voltage is amplified by $A_{DV}$, which also introduces pole $p_v$ in the voltage path. The outputs of amplifiers $A_{DI}$ and $A_{DV}$ are then mixed by summing amplifier $A_{DS}$ whose output is ultimately modulated into the duty-cycle of switches MN and MP by hysteretic comparator $C_D$. In this IC prototype, the switches and their gate drivers are off-chip, along with the LC filter elements.

**B. IC Design**

State-of-the-art $\Sigma\Delta$ controllers [3] employ high loop-gain, op-amp based, closed-loop amplifiers to accurately scale the gains of the sensed variables. Besides being susceptible to supply and ground noise, given their signals are single-ended, the switching frequency is limited by the speed of the controller, which is in turn set by the op amp's bandwidth. Current-mode processing based on current-conveyors [8] improves the bandwidth by reducing the number of high-impedance nodes and their associated voltage swings, but their vulnerability to noise, although somewhat improved, is still limited to the capabilities of single-ended processing schemes.

The presented controller implements a simple differential circuit where the feedback loop is closed around a single transistor and its source degenerating resistor, thereby allowing high bandwidth operation. In addition, the complexity associated an output common-mode feedback circuit is eliminated. The proposed system, designed in a 0.6μm double-poly, CMOS process with poly-poly capacitor (1fF/μm$^2$) and high-resistance poly (1kΩ/μm) options, also shows that the open-loop gain can be reduced to achieve high bandwidth without incurring a significant tradeoff in accuracy.

**1) Basic Amplifier Implementation**

The source-degenerated input transistor MNI produces an ac drain current $i_d$ that is folded through cascode PMOS transistor MPC to the output resistor $R_2$, generating the amplified output voltage $v_o$. The ac gain of this circuit is

$$A = \frac{v_o}{v_d} = \frac{R_2}{R_1} \left( \frac{g_m R_1}{1 + g_m R_1} \right) = \frac{R_2}{R_1} \left( K \right),$$

where $g_m$ is the transconductance of MNI. Since the ratio $R_2/R_1$ can be designed with very high accuracy ($< 0.5\%$) the net accuracy of $A$ across process and temperature variations is determined through the sensitivity of $K$ to small, and in the worst case, uncorrelated variations in the $g_m$ and $R_1$:

$$K + \Delta K = \left( g_m + \Delta g_m \right) \left( R_1 + \Delta R_1 \right) \left( 1 + g_m R_1 \right) + \frac{\Delta g_m R_1 + \Delta R_1}{\left( 1 + g_m R_1 \right)^2},$$

where $\Delta g_m$ and $\Delta R_1$ are small variations in $g_m$ and $R_1$ respectively, and second order terms are ignored. Therefore the relative sensitivity of $K$ is

$$\frac{\Delta K}{K} = \left. \frac{1}{1 + g_m R_1} \left( \frac{\Delta g_m}{g_m} + \frac{\Delta R_1}{R_1} \right) \right|_{K=1}.$$  

Equation (17) confirms that the term $g_m R_1$, which is the
open loop gain of the source-degenerating MNI-R₁ series feedback loop, suppresses the variations in \( i_{ds} \) from those in its determining terms \( g_m \) and \( R_1 \). As a result, by appropriately increasing the value of \( g_m R_1 \), a desired accuracy specification for gain \( A \) (e.g., \( \pm 10\% \)), can be met. In the limit, when the loop gain \( g_m R_1 \) is much greater than unity, \( K \) tends to a constant value of unity and \( A \approx R_2/R_1 \).

The MNI-R₁ loop that determines \( i_{ds} \), has high bandwidth limited only by the product of \( R_1 \) and the parasitic diffusion capacitance at the source of MNI. The pole at the other relatively high-resistance node i.e., the output node, is also at a high frequency because the cascode transistor MPC is designed with almost the minimum drawn length, keeping its drain capacitance small. Overall, a high-bandwidth amplifier can be achieved with a desired level of accuracy. The following sub-sections describe adaptations of the aforementioned circuit to the controller blocks shown in Fig. 4.

2) Current-Sense Amplifier (\( A_{DS} \))

The amplifier circuit (Fig. 6) implements a fully differential version of the basic cell in Fig. 5. Accordingly, the effective source-degenerated transconductor MNI+R₁ from Fig. 5 is replaced by a matched differential transconductor (\( G_{ds} \)) composed of MNI1-12+R₁1-12, where the common node \( v_C \) is ac-ground. The amplified differential voltage across the resistors \( R_{11-22} \) is buffered by the source-follower stages MP31-32, to give the primary differential output \( v_{IL} \). A differential RC filter yields the low-frequency component \( (v_{IL,REF}) \) of \( v_{IL} \) as the sensed current reference. In actuality, the capacitors in the RC filter are implemented using voltage-mode capacitor multipliers [12] to save area. The output common-mode level is naturally set by the DC current flowing through resistors \( R_{21-22} \), and the source-gate voltages of buffer transistors MP31-32, both component pairs being carefully laid out to minimize offsets. As for the other following blocks, the DC gain of current-sense amplifier is designed for an accuracy of \( \pm 10\% \) over worst-case PVT corners by appropriate choice of input devices MNI1-12 and resistors \( R_{11-12} \).

C. Voltage-Sense Amplifier (\( A_{DV} \))

One of the drawbacks of the circuit in Fig. 6 is that the input common-mode range (ICMR) is reduced by the additional DC voltage drop across the source-degenerating resistors \( R_{11-12} \). While this is not a concern for the current-sense amplifier whose input common-mode level is close to \( V_{DD} \), it poses a problem for the voltage-sense amplifier whose common-mode input is at the reference voltage (\( \sim 1.2 \) V). To improve the ICMR, the tail current is split into two sources \( I_{11-12} \) (Fig. 7) each half of the original value and the source-degenerating resistors are relocated so that they do not carry any DC current. The transistor DC biasing currents and the ac equivalent circuit are unchanged with node \( v_C \) being ac ground; hence, resistors \( R_{11-12} \) provide identical series feedback as described for Fig. 5 giving similar amplification.

The expected repercussion of splitting the tail current is an increased possibility of mismatch and therefore, a higher input-referred offset voltage; however, it can still be kept small by careful design and layout. Apart from this change in the input stage, the rest of the amplifier design is essentially the same as in Fig. 6, with changed polarities of the input and cascode transistors to meet input common-mode requirements. An RC filter at the amplifier output introduces the desired pole \( p_v \) (Fig. 3) in voltage path. As before, the physical filter capacitors are reduced in size by capacitor multipliers.

3) Summing Amplifier (\( A_{DV} \))

The summing amplifier is readily realized by combining the output currents of multiple differential transconductors (Fig. 8(a)) based on the circuit in Fig. 5. Consequently, in the circuit implementation (Fig. 8(b)) each summed input corresponds to a differential pair that feeds its output ac current to a common pair of cascode (common-gate) transistors MP21-22. The differential output voltage \( v_{SUM} \) across resistors \( R_{21-22} \), by superposition, is

\[
v_{SUM} = (v_1 + i_1 + i_2)Z_S = (G_{RV}v_1 + G_{RI}v_{11} + G_{RI}v_{12})Z_S, \quad (18)
\]

where the \( G_{RV,1} \) are the differential transconductances, \( v_1, i_1, i_2 \) and \( v_{11}, v_{12} \) are the input voltage and output current contributions from each input differential pair, and \( Z_S \) is the differential impedance looking into the output given by

\[
Z_S = 2R_{21} \left( \frac{2R_{23} + \frac{1}{C_2}}{2R_{23} + \frac{1}{C_2}} \right), \quad (19)
\]

ignoring the impedance looking into the drains of the cascode transistors MP21, 22. The gain from each input to the output is designed by choosing the appropriate source degenerating resistor value based on the earlier analysis for Fig. 5.

The inputs to each differential pair are chosen to have the same common-mode value under steady state conditions to reduce body-effect related mismatch. In the actual circuit, the summed output \( v_{SUM} \) is followed by source follower buffers, but these are omitted for simplicity from Fig. 8(b). The resistors \( R_{23-24} \) and capacitor \( C_2 \) at the output introduce the
pole-zero pair $p_1$-$z_1$ from Fig. 3.

D. Comparator ($C_D$)

The comparator design is standard with a preamplifier and latch for optimal propagation delay (<25ns) [13]. As such, the circuit is not included here for brevity. The interested reader is encouraged to consult literature for details [13], [14].

IV. EXPERIMENTAL RESULTS

In order to validate the functionality of the circuit blocks as well as the controller system, the prototype IC (in DIP40 package) is designed in two parts –

A. a set of circuit blocks that are not interconnected on-chip have all their I/O terminals accessible via package pins, and,

B. an additional set of identical circuit blocks are interconnected on-chip as in Fig. 4 with the only inputs of amplifiers $A_{DI}$-$A_{DV}$ and the output of comparator $C_D$ accessible off-chip via separate pins.

A. Performance of Amplifier Blocks

Because of high package parasitics, it is possible to measure accurately only the DC and low frequency characteristics of the pinned out blocks. To validate the accuracy of the controller IC over process variations, the above measurements are conducted for 39 parts in the production lot. The measured net DC gains $g_{mR}$ and $g_{mS}$ (Fig. 9(a)), accounting for the gains of amplifiers $A_{DI}$, $A_{DV}$, and $A_{DS}$, vary by less than 6% around their mean values of 7.4V/A and 37.2V/V respectively. The net offset voltage (Fig. 9(b)) referred to the input of amplifier $A_{DV}$ (including the effect of $A_{DS}$) is higher than that for $A_{DI}$ because of the additional mismatch in the tail currents biasing the input differential pair of $A_{DV}$. Nonetheless, the standard deviation (σ) for net input offset voltages of both $A_{DI}$ and $A_{DV}$ remains low (0.86mV and 2.01mV respectively). The simulated 3dB frequencies (due to parasitic poles) at the worst-case corners for amplifiers $A_{DI}$, $A_{DV}$, and $A_{DS}$ are 12MHz, 5MHz, and 13MHz respectively, with typical values roughly 40% higher.

B. Performance of $\Sigma\Delta$ Boost Converter

In assembling the system, the gate signal from the controller IC is buffered by an off-chip gate driver to drive the power switches. Various system performance parameters including stability, line/load regulation, power efficiency, and switching frequency variations are studied for a wide range of filter LC values. The results are discussed in the following text.

1) Steady-State: Steady-state inductor current and output voltage waveforms at $V_{IN}$=2.7V, $V_{O}$=5V, $L$=22μH, $C$=62μF, $I_{O}$=0.8A, (Fig. 10) show ripples in the output voltage (40mV pk-pk) and inductor current (190mA pk-pk), which are sensed by the $\Sigma\Delta$ controller through sensing ratios of 0.24V/V and ($A_{DI}R_l$) 0.4V/A respectively. The effective hysteresis window is roughly 650mVpk-pk and at the switching frequency of 330kHz, the value of $g_{mR}R_l$ (from Table 1) is approximately 3.8V/A, which corresponds to a current ripple of 170mA pk-
The slight discrepancy between the measured and hand-calculated values is attributed to additional switching delays.

2) Stability: The unity-gain frequency of the voltage loop approaches that of the current loop for increasing filter inductor and decreasing output capacitor values, destabilizing the $\Sigma\Delta$ operation, as seen from equation (10). In the evaluated circuit, the worst-case LC operation limits were determined in terms of the minimum capacitor value for a given inductor value at the maximum rated load (0.8A) and minimum supply voltage (2.7V) (equation (10)). Therefore, for a set value of the filter inductor, the capacitor value was gradually decreased (in steps of 0.5$\mu$F) and the converter subjected to a load step of 0.3 to 0.8 A for each capacitor value, until the circuit became unstable with the inductor current and the output voltage showing persistent oscillations (Fig. 11).

In the other direction, the highest capacitor value was restricted to 350$\mu$F as a practical limit in portable applications. A similar procedure was followed for $R_{ESR}$, which was limited to 50m$\Omega$ from ripple considerations in the output voltage. Given these constraints, the stable operating region of the $\Sigma\Delta$ controller can be represented as the enclosure of the $R_{ESR}$LC stability space (Fig. 12). As suggested by equation (10), the minimum capacitance for stable operation decreases – in this case from 15$\mu$F to 1$\mu$F as the inductor decreases from 30$\mu$H to 1$\mu$H. Resistance $R_{ESR}$ has little effect on the stability since the loop response near its unity-gain (switching) frequency is determined largely by the current loop (Fig. 2). The robustness of the controller design against process variations is confirmed by the nearly overlapping stability volumes measured for 10 samples from the production lot.

3) Switching Frequency Variations:

As explained in section II(B)(3), switching frequency with a constant gain $g_mR_S$ would be ideally expected to decrease significantly as the input voltage changed from 2.7V to 4.2V, even including the effects of a constant switching delay and line regulation. This is illustrated in the constant $g_mR_S$ curve for 5$\mu$H and 0.5A (Fig. 13), which shows a net switching frequency variation of 43%. In comparison, the measured curve has improved performance with the switching frequency variations restricted to 25% at 0.5A because of the inverse frequency dependence of gain $g_mZ_S$ (Figs. 3 and 8). Fig. 13 also shows that as the load increases, the resulting droop in output voltage increases the switching frequency further reducing its line variation at high loads.
4) Line and Load Regulation: Switching delays in the converter and finite loop-gain result in a variation of the DC output voltage from its desired value with changes in the supply voltage and load current. As the input voltage changes from 2.7V to 4.2V making the duty-cycle more asymmetrical, experimental results show that the error in the regulated output voltage becomes more negative, validating equation (14). Therefore, with the output voltage centered at a 3.3V input, the error voltage changes polarity as the input voltage transitions between its extreme values (Fig. 14). The increase in the error voltage magnitude with decreasing filter inductance expressly shows the effects of loop delays on the regulation performance. In the prototype IC, higher package parasitics (DIP40 package) and off-chip gate-drivers lead to a rise in switching delays whose effects were most evident at the lowest inductance value of 1µH (voltage error ≈ +1%, -2%). The steady-state error remains below ±1% at higher inductors that suppress the effects of switching delays. A package with lower parasitics would further improve the performance.

Since the loop response near and at the switching frequency is dominated by the current loop, load variations do not affect the output voltage (Fig. 15) as significantly as line voltage variations. The effect of varying filter inductance remains the same as before with worst-case error (+0.2%, -0.9%) at 1µH.

5) Efficiency: Power efficiency in a variable filter, self-oscillating ΣΔ converter is subjected to several loss mechanisms and the dominance of one over the others is determined by not only line voltage and load, but also by filter inductance. Measured efficiency curves at a V_{IN} of 3.3V (Fig. 16) show that at high inductor values the efficiencies are higher at load currents (91% at 0.1A, 29µH, 120kHz) because of low switching frequencies and consequently low switching losses. However, at increased loads, higher inductors, which have a higher equivalent series resistance (ESR_{L}) due more coil turns, suffer from greater conduction losses leading to a reduced system efficiency (83% at 0.8A, 29µH). This trend is reversed as the inductor value decreases because an increase in the switching frequency degrades low load efficiency (88% at 0.1A, 12.5µH, 250kHz) and a reduced ESR_{L} increases high load efficiency (86.5% at 0.8A, 29µH). However, as the inductance decreases further, increase in the switching frequency is limited not by the comparator hysteresis but by the switching delays due to package parasitics.

\begin{align*}
\text{Efficiency} & = \frac{P_{OUT}}{P_{IN}} \\
\text{Input Voltage} & = V_{IN} \\
\text{Output Power} & = P_{OUT} \\
\text{Error} & = \frac{V_{OUT} - V_{REF}}{V_{REF}}
\end{align*}
parasitics. Therefore, the inductor-current ripple sharply increases (from 0.75A pk-pk at 5µH to 2.2A pk-pk at 1µH) making the RMS ripple current related conduction losses dominant. As a result, the overall efficiency reduces both at high and low loads (67% at 0.1A, 1µH, 550kHz; 82% at 0.8A, 1µH).

At higher input voltages, the efficiencies increase primarily because of reduced inductor and switch currents. Nevertheless, the trend remains as before (Fig. 17) with the lowest efficiencies at 1µH. The peak system efficiency approaches 94% at 0.3A, 29µH, and 4.2V supply voltage.

5) Load Transient Response: As mentioned earlier, a ΣΔ controller designed for a variable LC system is expected to suffer from a non-optimal transient response, and the proposed design is no exception. Nevertheless, by appropriately sizing the output capacitor, the desired transient response can be achieved. The measured 0.3-0.8A load transient response of the system (at L=5µH, C=200µF, and V_in=4.2V) is included (Fig. 18) for completeness.

V. CONCLUSION

A ΣΔ controller optimized for filter LC variations was presented, analyzed, and implemented (in a 0.6µm CMOS process) using simple low-gain, high-bandwidth, differential circuit blocks consisting essentially of source-degenerated input transconductance stages. Stable converter operation for orders of magnitude variations in filter LC and capacitor ESR values (1-30µH, 1-350µF, 5-50mΩ) was verified through experimental results. In designing the high speed ΣΔ controller, the use of low-gain blocks was validated by the open-loop DC gain accuracy (+6% over process and line variations) and overall converter accuracy (+1.5% over process, line, load, and filter variations). Although the system performance was somewhat degraded at low inductance values because of higher package parasitics, switching delays, and the consequent limitations on switching frequency, other performance metrics - efficiency (up to 95%) and switching frequency variations (improvement of 20%), were also well within specifications; a low-parasitic package would improve performance throughout the inductance range. Overall, with regard to the problem that an integrated boost dc-dc controller may be exposed to widely varying off-chip filter LC parameters jeopardizing stability and performance, the presented ΣΔ boost dc-dc controller gives a flexible, simple, and user-friendly solution.

<table>
<thead>
<tr>
<th>VDD</th>
<th>2.7V - 4.2V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ibias</td>
<td>0.6mA</td>
</tr>
<tr>
<td>Area</td>
<td>0.9mm²</td>
</tr>
<tr>
<td>Peak converter efficiency</td>
<td>95%</td>
</tr>
<tr>
<td>R_eq-LC space</td>
<td>5-50mΩ</td>
</tr>
<tr>
<td>Feature size</td>
<td>0.62mm</td>
</tr>
</tbody>
</table>

Fig. 18. 0.3A to 0.8A load step response at 5µH, 200µF, and V_in = 4.2V

Fig. 19. Die photograph and key specifications of the fabricated ΣΔ controller IC.

REFERENCES


