A High-Efficiency, Dual-Mode, Dynamic, Buck–Boost Power Supply IC for Portable Applications

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***Abstract*—Integrated power supplies are critical building blocks in state-of-the-art portable applications, where they efficiently and accurately transform a battery supply into various regulated voltages, as required by their loads. This paper presents a novel low voltage, dual-mode, buck-boost converter IC targeted for dynamic supplies of linear RF power amplifiers (PAs) in wireless handsets. Maintaining high efficiency of the converter over a wide loading range is critical for improving battery life in such systems. The use of a novel supply voltage using adaptive on time control for pulse-frequency-modulation (PFM) mode achieves an accurate output ripple voltage, not to mention higher efficiency under light loads, which is important in portable applications. In the high-power mode, the converter is operated in a modified pulse-width-modulated (PWM) control, where its operation is changed adaptively between the buck, buck-boost, and boost regions, thereby saving unnecessary switching losses. Appropriate circuit topologies are developed and designed to overcome the challenges of a low supply voltage environment requiring a wide dynamic range converter. The converter is designed and simulated using a 0.5-µm n-well CMOS process for a supply voltage range of 1.4-4.2 V, which is compatible with state-of-the-art Li-ion batteries (2.7–4.2 V), and alternate power sources, e.g., NiCd and NiMH batteries. Simulation results show that the converter generates an output voltage of 0.5–5 V while delivering up to 0.5 A of load current with a maximum ripple voltage of 40 mV. The converter exhibits efficiency of 60–90% in PWM mode and 80% in PFM mode. A 0.9–1 V transient control-step response in PWM mode, which refers to a change in output voltage of 4.5–5 V, from an input supply of 1.4 V, is less than 200 µsec.**

***Index Terms*—Buck-boost converter IC, integrated power management, dual-mode converter**

I. Introduction

The widespread use of portable devices with multiple functionalities (e.g., voice, data, imaging, and multimedia) has resulted in the requirement of efficient power saving solutions to prolong battery life. State-of-the-art power management systems are used to generate constant or variable supplies from battery sources having a wide terminal voltage variation (e.g., NiCd/NiMH: 1.8–0.9 V, Li-ion: 4.2–2.7 V). At any given time, the required voltage can be higher or lower than the battery voltage, depending on the application, thereby requiring a buck-boost (step-up and -down) regulator. For example, in the 3.3 V I/O [1] and USB applications [2] a buck-boost converter is required to allow the Li-ion battery to be drained to its lowest level. A comparative evaluation of various circuit topologies suitable for buck-boost conversion in portable applications is found in [3]. The single-inductor buck-boost converter, in spite of its complexity, is preferred in portable applications because of its suitability of realizing a cost-effective, integrated solution with fewer external inductors and capacitors.

This paper presents an integrated circuit (IC) design and implementation of a dual-mode, buck-boost converter to achieve high efficiency over wide loading conditions. The converter is designed as a dynamically adaptive supply for a code-division-multiple-access (CDMA) RF power amplifier (PA)[4]. Fig. 1 shows the supply voltage profile of the PA, which reveals that the converter output voltage varies in two regions. In region "A" the PA supply voltage is adjusted from a maximum (V_{MAX}) to a minimum (V_{MIN}) as its output power changes from the maximum output power (P_{MAX}) to a power level (P_{TH}, corresponding to V_{MIN}) and "B" where the supply voltage is kept constant at V_{MIN} in spite of its output power decreasing below P_{TH}.

Fixed-frequency PWM converters suffer from lower efficiency during light loads, where switching losses dominant the total power loss. The novelty of this work relies on the use of novel pulse-frequency modulation (PFM) control with adaptive on-time control in region B of operation of the converter, where the switching frequency is lower resulting in higher efficiency. Unlike state-of-the-art PFM converters with constant on-time control, the converter's on time is adaptively adjusted with the supply voltage to achieve an accurate ripple voltage. Furthermore, the simplicity of the PFM controller with a lower quiescent current consumption offers a better standby performance compared to the converter operating in PWM mode. Appropriate low voltage circuit topologies are developed to enable the converter's operation with a minimum supply voltage of 1.4 V having PMOS and NMOS threshold voltages of 0.95 and 0.75 V, respectively. In addition, the challenges of designing and implementing the PWM control scheme in a low supply voltage environment to dynamically transition between buck, buck-boost, and boost region depending on the input and output voltage are addressed in this paper.

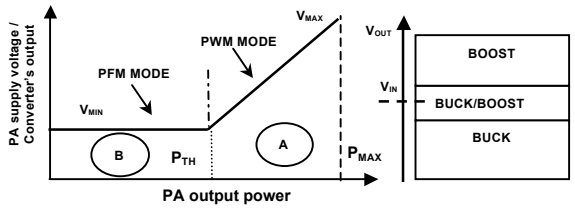

Fig. 1. Converter's output voltage profile.

Section II of the paper introduces the dual-mode converter and its operation. In Section III, IC design of the converter's building blocks is presented while offering insightful design considerations. Representative full chip circuit-level simulation results of the converter and its layout are presented in Section IV. Finally, conclusions are drawn in Section V.

II. The Dual-Mode Converter

A simplified schematic of the proposed buck-boost voltage regulator with dual-mode control is shown in Fig. 2. The two controllers, voltage-mode PWM and PFM are selected by an external signal (MODE), and at any given time, only one remains active.

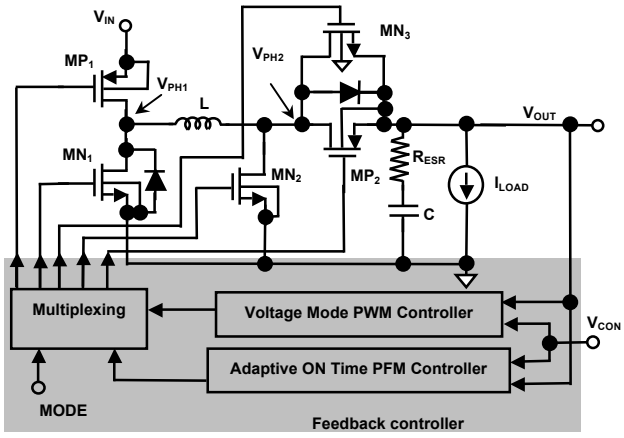

Fig. 2. Schematic of the dual-mode, buck-boost voltage regulator.

PWM Mode: The basic noninverting synchronous buck-boost converter operates with four switches (MP_1, MN_1, MP_2 and MN_2) turning on and off

to generate the output voltage [3]. Intuitively, any output voltage can be generated using either a buck or a boost converter, which requires only two switches to be operational. In the buck (step-down) mode, switch MN_2 is open while MP_2 and MN_3 are closed. Similarly, for boost operation, MN_1 is open while MP_1 is closed. Fig. 3 shows a modified control scheme [5], [6], to realize the functionality just mentioned earlier. To adaptively control the transition between buck and boost regions, the error amplifier's output voltage, V_{EAO}, is level-shifted by V_{LS} for comparison with the triangular wave signal (V_{TW}) to control the buck switches MP_1 and MN_1. The error amplifier's output voltage, V_{EAO}, is directly compared with V_{TW} to control the boost switches MN_2, MN_3 and MP_2. If the shift voltage, V_{LS}, is exactly equal to the triangular wave generator's peak-to-peak voltage, the converter operates either in buck or in boost region. However, designing the shift voltage to be exactly equal to the triangular wave generator's peak-to-peak voltage is not practical in an IC environment because of the process variation and tolerance. Furthermore, the input offset voltage inherent associated with the comparators add to the inaccuracies even if the shift voltage (V_{LS}) is trimmed to be equal to the triangular wave generators peak-to-peak output signal. Therefore, an overlap between buck and boost mode is deliberately established to account for any instability that might arise in a situation where the output voltage cannot be generated either in buck or boost mode.

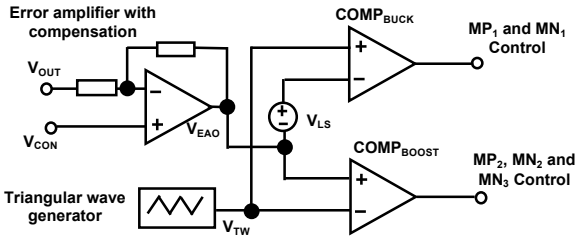

Fig. 3. Control scheme for separate buck, buck-boost and boost region of operation in PWM mode.

PFM Mode: For the PA application considered in this work, the converter's output voltage is kept at 0.5 V from an input supply of 1.4 – 4.2 V during low loading conditions. Therefore, the converter operates in only buck-mode with PFM.. During the on time, transistor MP_1 is turned-on resulting in a inductor current rise up to I_{L_PEAK}, and therefore stores energy in the inductor's magnetic field and charges the output capacitor while providing load current. In the second interval, the inductor current freewheels through switch MN_1. Finally, when the inductor current starts to flow in the negative direction, MN_1 is switched off resulting in a discontinuous conduction mode (DCM) operation. During the third interval, no switching action happens and the load current is provided by the output capacitor, thereby discharging it. When the output voltage drops below the control voltage, MP_1 is turned on and the cycle of event repeats.

MP_1's on time can be controlled by detecting the inductor's peak-current [7], which requires additional current sensing circuitry and results in additional power losses and lower efficiency, especially during heavy loading conditions, not to mention increased complexity. A predefined constant on-time control can be used to eliminate the peak-current sensing requirement. However, for a given output voltage, a constant on time designed for the high-end of the input supply (4.2 V) results in a lower peak-current and thereby lower stored energy in the inductor when operated with lower-limit of the supply (1.4 V) during a given switching interval. A lower energy transfer to the output in one cycle essentially results in a higher switching frequency to maintain voltage regulation, which defeats the advantage of using a PFM control. Conversely, an on time designed for the lower supply voltage yields a higher peak current when operated at the highest supply voltage, thereby resulting in a larger output voltage ripple. These limitations are overcome by dynamically adjusting the PMOS on time with the supply voltage variation. Fig. 4 shows the simplified schematic of the PFM mode controller.

As the output capacitor voltage is discharged below the required voltage as set by the control signal, the output voltage sensing comparator's output goes from 0 to 1, which sets the RS latch (RS_1). After a certain delay, the latch is reset, thereby producing an on time for the switch MP_1. After MP_1 is turned off, the transistor MN_1 is turned on by setting RS_2 until the inductor current direction changes from a positive to a negative value resetting RS_2. The inductor current transition is detected indirectly by sensing the node voltage V_{PH1}, which changes from a negative (when inductor current is positive) to a positive value (when inductor current is negative).

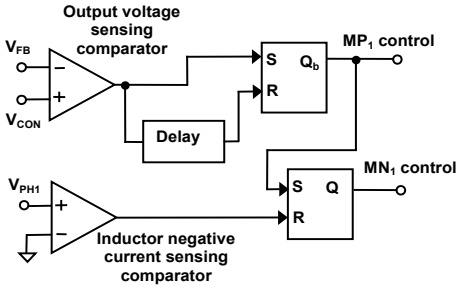

Fig. 4. Simplified schematic of the PFM controller.

Mode Transition: The transition from PWM mode to PFM mode and vice versa offers unique design challenges to provide uninterrupted power for the load accurately. During this period a lower converter's output voltage than the required PA supply would result in unnecessary signal clipping and subsequent degradation in the transmitter's signal quality. One way to avoid such a scenario is to generate a higher voltage before mode transition such that even during the transition period the converter's voltage does not fall below the PA's required voltage level.

III. Integrated System Design

The schematic of the system is shown in Fig. 5. The converter is designed for an output voltage of 0.5 – 5 V up to a 0.5 A load with 1.4 – 5 V supply, and a switching frequency of 1 MHz. The targeted peak-to-peak ripple is less than 50 mV (at 5 V output and 500 mA load current), with less than 250 μsec worst-case control-signal transient response. The converter's output voltage is always 1-dB higher than the supply voltage required for the PA, to meet the transient requirement of 1dB in 666 μsec. All the control circuits are designed for a 1.4 V minimum supply in a 0.5 -μm n-well CMOS process with NMOS and PMOS threshold voltages of 0.7 V and 0.95, respectively. The minimum supply voltage requirement (1.4 V) is equal to sum of a threshold voltage (0.95 V) and three times (3×0.15 V = 0.45 V) the saturation voltage of a transistor.

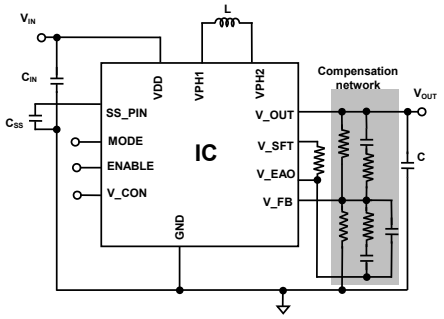

Fig. 5. Schematic of converter IC and external components.

1. Output filter inductor and capacitor selection: In a boost converter, the value of output inductor is chosen to optimize the ripple current for a given switching frequency and push the right-half plane (RHP) zero to a higher frequency by using a smaller inductor. For the minimum input supply of 1.4 V (V_{IN_MIN}) and maximum output voltage of 5 V (V_{OUT_MAX}) with load current 0.5 A (I_{LOAD}), the maximum duty cycle (D_{MAX}) of the converter in boost mode is 77 % , where V_{SW} is the voltage drop due to the switches' on resistances (assumed to be 100 mV). Assuming a peak-to-peak inductor

current ripple of 1 A (ΔI_L), the minimum value of inductor is estimated to be 0.97 µH using the expression in [3]. A total ripple voltage of 50 mV is divided across the ESR component (30 mV) and the output capacitor ripple (20 mV) using the equation given in [3] to yield an output capacitor of 20 µF with an estimated ESR of 10 mΩ. Similarly, an input capacitor of 47 µF with an ESR of 5 mΩ is chosen to limit the input supply ripple within 50 mV.

2. Compensation Network: The time-averaged small-signal model of the boost converter [8] is used for designing the compensation network. For the converter to be stable across supply and loading conditions, it is compensated for the worst-case conditions. In a boost converter, the loop is compensated to achieve an open-loop unity gain frequency before the RHP zero location. Since the RHP zero caused by the inductor is at the lowest frequency when the maximum output voltage is generated from the minimum input (maximum duty cycle) with maximum load current, the converter is compensated for this condition. For a maximum duty cycle of 80 % and triangular wave generator's peak-to-peak signal of 300 mV, the uncompensated feedback loop has an open-loop gain of 16.77 dB with a pair of complex-conjugate filter poles at 7.2 kHz and a RHP zero at 64 kHz. A 2-zero and 3-pole, type III network (shown in Fig. 7) with zeros at the filter pole frequency, one pole at the origin and two other poles just around the switching frequency of the converter is used to compensate the PWM control loop yielding a unity-gain frequency of 35 kHz and phase margin of 30 degrees.

3. Power Switches: Design of the power switches for the integrated buck-boost converter is driven by efficiency and functional considerations, especially in a low-supply voltage environment. The W/L values in µm of MP_1, MN_1, MP_2, MN_2, MN_3 used for this design are 360000/0.6, 60000/0.6, 180000/ 0.6, 120000/0.6, 80000/ 0.6, respectively.

4. Error Amplifier: To generate an output voltage of 0.5 to 5 V, the control signal for the dynamic converter is chosen to vary from 0.1 to 1 V with a closed-loop gain of 5, considering the minimum supply voltage of 1.4 V. The error amplifier's input offset voltage is a critical parameter since it appears as the steady-state output voltage error amplified by the converter's closed-loop gain. Subsequently, a lower range of control signal results in a larger converter closed-loop gain, which means a higher output voltage error is contributed by the op-amp's input offset voltage. Realization of a low-offset op-amp, especially in a CMOS process requires complex offset cancellation schemes. Designing large input common-mode range (ICMR) op-amp with high threshold voltages of transistors is quite challenging. A supply voltage tracking common-mode feedforward technique using the principle offered in [9], the schematic of which is shown in Fig. 6, is used to achieve the desired ICMR over the entire supply voltage range.

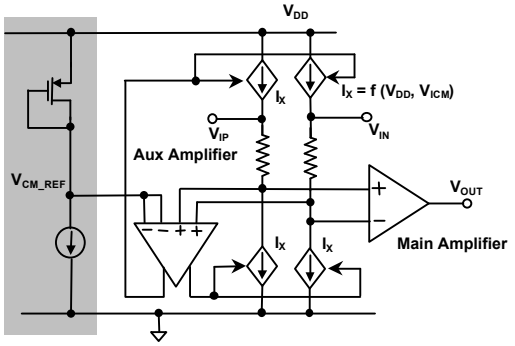

Fig. 6. Simplified schematic of the error amplifier.

The circuit essentially consists of a main amplifier whose input common mode signal is adjusted to a reference signal (V_{CM_REF}) using an auxiliary amplifier in a negative feedback configuration, while the differential input signal remains unaltered. The reference signal V_{CM_REF} is generated with respect to the supply voltage and PMOS input pairs are used in the amplifiers for this design. For a given reference signal, a larger common-mode value of the input signal results in a higher voltage drop across the resistors, thereby the actual signal applied to the input of the main amplifier is within its ICMR. The amplifier's simulated open-loop gain is greater than 70 dB over process, temperature, supply voltage, and common-mode variations with 65 µA of maximum bias current.

5. Triangular wave generator: The frequency of the triangular wave signal in PWM voltage mode control is same as the converter's switching frequency. Fig. 9 represents a conceptual representation of the circuit. Essentially, a pair of current source/sink are switched on and off to charge/discharge a capacitor to generate the triangular signal. The comparators control the switching action when the triangular wave signal crosses either the high (V_{HIGH}) or low value (V_{LOW}). For a minimum supply of 1.4 V, error amplifier's maximum output voltage being (V_{DD} – V_{DS_SAT}) 1.25 V, and the lower ICMR value of an NMOS input stage (V_{TN} + $2V_{DS\_SAT}$) 0.95 V, and the triangular wave generator is designed for a peak-to-peak signal of 300 mV (0.95 – 1.25 V).

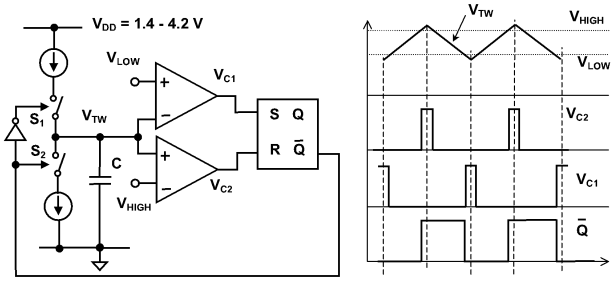

Fig. 7. Simplified schematic of the triangular-wave generator.

6. Adaptive on time for PFM: The PMOS (MP_1 in Fig. 2) on time in PFM control is determined from the relationship between on-time (T_{PMOS}), input and output voltage and peak inductor current (I_{L_EAK}). A larger on time results in a higher peak inductor current, which subsequently produces a larger ripple at the output capacitor. Since the inductor (L) and capacitor (C) values are already selected to meet the PWM control requirements, to meet the output ripple voltage (ΔV) specifications, the peak inductor current to a certain value given by the expression

$$I_{L\_PEAK} \le \frac{2C\Delta V_{OUT}}{L}\left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right), \quad (1)$$

which ultimately determines the on time of the converter. Fig. 8 presents conceptual representation of the circuit used to generate on time for PFM control. The circuit uses a current (I_{VAR}) dependent on V_{IN} and V_{OUT} to charge a capacitor whose voltage is compared with a constant voltage to generate the desired delay. For a given output voltage, a higher supply results in a larger current consequently charging the capacitor faster and subsequently resulting in a smaller delay.

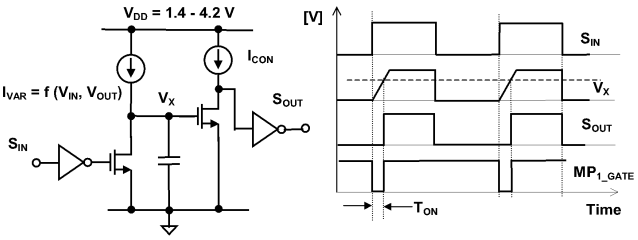

Fig. 8. Adaptive on-time circuit for the PFM controller.

The PWM comparators in the voltage mode controller (Fig. 3) and triangular wave generator (Fig. 7) use a two-stage architecture with NMOS differential input stages [10] designed for a minimum ICMR of 0.95 – 1.25 V. The comparator's propagation delay is less than 100 nsec to minimize the control loop's phase margin degradation due to the feedback path delay. The PFM comparators use a standard two-stage architecture [11] with PMOS input pairs and are designed for an ICMR of – 50 mV to 150 mV, which satisfies the requirement of zero voltage detection and sensing

a feedback signal of 100 mV corresponding the output voltage of 500 mV in PFM mode. Also, a bandgap reference circuit is designed to generate the reference voltages (V_{LOW} and V_{HIGH}) for the triangular wave generators and also provide a current reference that is used to bias various analog building blocks throughout the chip. For brevity, the details of deign and implementation is not presented here and can be found in [10].

V. Simulation Results and Discussion

The converter circuit is simulated using Cadence Spectre simulation environment. Fig. 9(a) shows a representative plot of simulation results with key waveforms, e.g., inductor current, output voltage illustrating the converter's functionality in PWM mode. The output ripple voltage is within 18 mV when a 5 V steady-state output voltage is generated from a 1.5 V input supply with a load resistance of 15 Ω. Fig. 9(b) depicts the worst-case control step response, which is simulated with a 0.9 – 1 V step signal at the control input of the converter while monitoring its output voltage and inductor current. The transient response plot illustrates the converter's stability under the extreme duty cycle environment for which the compensation circuitry is designed. The converter's output voltage changes from 4.5 to 5 V within 200 μsec with an input supply of 1.5 V.

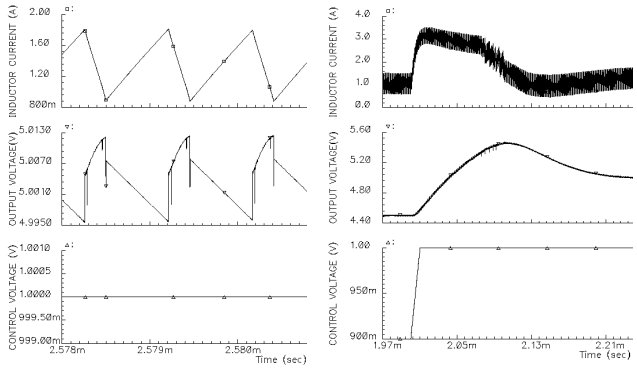

Fig. 10. Full chip PWM mode simulation results: (a) Steady-state waveforms (V_{IN}= 1.5 V, V_{OUT} = 5 V), (b) Control-step response.

Fig. 11 shows the representative steady-state waveform illustrating the functionality of the converter operating in PFM control with an output voltage of 0.5 V having a peak-to-peak ripple of 13 mV generated from an input supply of 3.0 V. The output ripple voltage in PFM mode is critical to minimize signal distortion, especially when the transmitted power is low. A summary of the converter's performance is offered in Table I, which verifies that the simulation results are within the targeted values. The converter's efficiency, which is of interest in battery-life improvement, has seen an improvement from 60 % in PWM mode to 80 % in PFM mode operation for an output voltage of 500 mV. The converter IC is currently under fabrication.

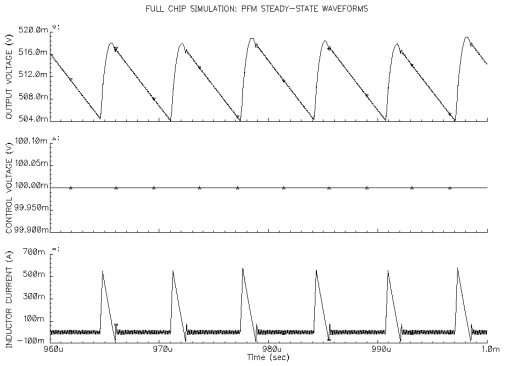

Fig. 11. Full chip simulation results: PFM steady-state waveforms.

VI. Conclusions

A novel dual-mode, noninverting synchronous buck-boost power supply IC with an output voltage range of 0.5 – 5 V and an input supply of 1.4 – 4.2 V is presented. With the use of adaptive on-time based PFM control in DCM, the converter exhibits an efficiency of 80 % compared to the 60 % achieved in PWM mode during light loading conditions (500 mV of output voltage and a 50 mA load current). The converter efficiency in PWM mode was from 60 – 93 % with a resistive load of 10 Ω over the entire output voltage range. In PFM mode, the converter's standby performance is improved by reducing its quiescent current dissipation, i.g., use a simple control circuit. The low voltage design and implementation of the converter circuit blocks provides a basis for designing converters for versatile portable power source applications, e.g., rechargeable nickel- and lithium-based batteries.

Although the minimum supply voltage of the converter is limited to 1.4 V because of technological constraints (PMOS threshold voltages of 0.95 V), the concepts developed can be extended to other processes. For a process with a threshold voltage of 0.5 V, for instance, the circuit can be designed for a minimum supply voltage of 0.95 V, which is compatible with low-cost, single-cell batteries. With power management of battery-powered devices becoming a critical issue, the dual-mode buck-boost supply proposed, with its ability to operate efficiently over wide loading conditions and under a variable supply environment, plays an important role in portable systems.

Table I. Integrated converter's simulation results summary.

Parameters	Target	Sim. Result
PWM Control		
Supply voltage	1.4 – 4.2 V	1.4 – 4.2 V
Output voltage	0.5 – 5 V	0.5 – 5 V
Load current	50 – 500 mA	50 – 500 mA
Output ripple	≤ 50 mV	10 – 40 mV
Worst-case control-step response	≤ 250 μs	200 μs
Efficiency (peak load)	> 90 %	60 – 93 %
PFM Control		
Output voltage	0.5	0.51
Load current	50 mA	50 mA
Efficiency	> 80 %	78 – 85 %

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