Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications

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ABSTRACT
Linear regulators are critical analog blocks that shield a system from fluctuations in supply rails and the importance of determining their Power Supply Rejection (PSR) performance is magnified in SoC systems, given their inherently noisy environments. In this work, a simple, intuitive, voltage divider model is introduced to analyze the PSR of linear regulators, from which design guidelines for obtaining high PSR performance are derived. The PSR of regulators that use PMOS output stages for low drop-out (LDO), crucial for modern low-voltage systems, is enhanced by error amplifiers which present a supply-correlated ripple at the gate of the PMOS pass device. On the other hand, amplifiers that suppress the supply ripple at their output are optimal for NMOS output stages since the source is now free from output ripple. A better PSR bandwidth, at the cost of dc PSR, can be obtained by interchanging the amplifiers in the two cases. It has also been proved that the dc PSR, its dominant frequency breakpoint (where performance starts to degrade), and three subsequent breakpoints are determined by the dc open-loop gain, error amplifier bandwidth, unity-gain frequency (UGF) of the system, output pole, and ESR zero, respectively. These results were verified with SPICE simulations using BSIM3 models for the TSMC 0.35 µm CMOS process from MOSIS.

I. INTRODUCTION
The close proximity of analog and digital circuits in SoC environments can cause them to be overwhelmed by spurious switching noise signals propagated through supply lines, interface nodes, and substrate injection [1], [2]. In these VLSI and ULSI circuits, voltage regulators form an indispensable component of the power management system. They generate stable voltages while supplying a wide range of currents to a variety of circuits. They also filter the fluctuations in the power supply, thereby shielding their load circuits from supply ripple. Thus, in circuits like DRAMs [3], PLLs [4], [5], and EPROMs [6], where power supply noise directly translates to degradation in system performance, power supply rejection is a key figure of merit for a voltage regulator. It is therefore imperative to analyze the PSR of linear regulators over a large frequency range with the aim of establishing design guidelines and principles for high PSR performance. Further, as systems aggressively advance towards integration, these state-of-the-art regulators rely increasingly on on-chip capacitors (10-200 pF) for frequency compensation [3]-[7]. These capacitors do not consume expensive board-space and are not associated with a significant equivalent series resistance (ESR). Since the regulators do not use an external capacitor to establish the dominant low-frequency pole, they are termed “internally compensated regulators”. It must be noted, however, that the effects of ESR still warrant discussion, since they become important when the connectivity to the plates of the capacitor is limited by the dense routing requirements of the chip.

II. PSR OF A TYPICAL LINEAR REGULATOR

Fig. 1 depicts the block diagram of a typical linear regulator (pass device may be PMOS or NMOS).

Fig. 1. Block diagram of typical linear regulator (pass device may be PMOS or NMOS).

In its simplest form, the PSR transfer function (a ratio of the output to the supply ripple) can be viewed as the effect of a voltage divider caused by an impedance between the supply and the regulator output, and an impedance between the output and ground. An intuitive and insightful model for analyzing the PSR of a typical linear regulator is presented in Fig. 2. This model consists of an impedance ladder comprising of the channel resistance of the pass device ($r_{ds}$), and a parallel combination of the open-loop output resistance to ground ($z_0$), and the shunting effect of the feedback loop ($z_{o-reg}$). Hence, referring to Fig. 1 and Fig. 2, we can see that

$$z_o = \left( z_{Oout} + R_{ESR} \right) / (R_1 + R_2),$$

and,
The model is presented in Fig. 2. Thus, by simplifying the model in Fig. 1 to the one in Fig. 2, the PSR can be seen to be

\[
\text{PSR} = \frac{v_{\text{out}}}{v_{\text{id}}} = \frac{z_0}{r_{\text{ds}}} + \frac{z_{\text{reg}}}{(z'_0 \parallel z_{\text{reg}})} \beta.
\]

The presence of a PSR pole (p_1) at the unity-gain frequency, as predicted by (5), can be easily understood when we note that the deterioration of the PSR due to increasing closed-loop output resistance ceases at the UGF. At this stage, the shunting effect of the feedback loop no longer exists and the PSR is determined simply by the frequency-independent resistive divider between the channel resistance of the pass device (r_{ds}) and bias resistors (R_1+R_2). The PSR is given by

\[
\text{PSR}_{\text{UGF}} = \frac{z_0}{z_0 + r_{\text{ds}}} = \frac{R_1 + R_2}{R_1 + R_2 + r_{\text{ds}}} = 1.
\]

At these frequencies, the PSR of the system is the weakest since the closed loop output resistance is not decreased by the feedback loop and the output capacitor cannot shunt the output ripple to ground.

3) High Frequencies

When the output capacitor starts shunting (R_1+R_2) to ground, a smaller ripple appears at the output, thereby causing an improvement in the PSR (since z_0 decreases with increasing frequency) and the second PSR pole (p_2). Thus,

\[
\text{PSR}_{\text{UGF}} = \frac{z_0}{z_0 + r_{\text{ds}}} = \frac{R_1 \parallel R_2}{R_1 + R_2 + r_{\text{ds}}} C_{\text{out}}.
\]

The effectiveness of the output capacitor is, however, restricted by its ESR. At very high frequencies, since this capacitor is an “ac short”, \( z_0 \) is determined by the ESR, which limits PSR to

\[
\text{PSR}_{\text{UGF}} = \frac{z_0}{z_0 + r_{\text{ds}}} = \frac{1}{2\pi R_{\text{ESR}} C_{\text{out}}}
\]

thereby leading to the formation of an effective PSR zero at \( z_2 = 1/2\pi R_{\text{ESR}} C_{\text{out}} \). Fig. 3 shows a sketch of the poles and zeros of a typical PSR curve predicted by this model.

Though the simple model depicted in Fig. 2 provides an intuitive understanding of the relationship between PSR and the open-loop gain of the regulator, it does not take into account the effect of the conduction of the supply ripple through the amplifier itself. This ripple feedthrough has significant implications for high PSR design and is critical for determining the optimal amplifier topology for a particular type of output stage.

III. DESIGNING FOR HIGH PSR

A. Series Pass Device

In applications where low drop-out is not a primary concern, the output stage of the regulator is often an NMOS device. Despite the relatively large voltage headroom required to drive
the gate due to its gate-source voltage drop, the NMOS device, acting as a source follower, offers an inherently low output impedance, making the compensation of the regulator easier than its low drop-out counterpart [6], [7]. It is evident that in this follower configuration, the NMOS device will conduct the ripple present at its gate directly to its output, the source. Hence, to keep the ripple at the output node low, it is crucial to design the preceding error amplifier such that the ripple at the gate of the NMOS device is as small as possible.

In most low voltage applications today, however, a PFET transistor is used as the output series pass device [8]-[10] because of the driving requirements of its gate. In this configuration, the gain from the source of the device (connected to \( V_{dd} \)) to its drain, has the same magnitude as the gain from its gate to its drain, i.e., \( g_mR_{ds} \). However, the two gain paths are out of phase. Hence, in order to cancel the feedthrough of the power supply ripple from the source, the preceding amplifier should provide a correlated ripple at the gate of the PMOS device (\( V_{Si} = V_S - V_G = \delta_{Vdd} - \delta_{Vdd} = 0 \)). In other words, the supply ripple should appear as a common-mode signal at the gate and the source.

B. PSR of the Error Amplifier

Most error amplifiers that have a single-ended output use a current-mirror load to perform double-to-single-ended conversion and add the ac signals obtained from the input differential pair to a single-ended signal. This mirror may be implemented in the form of PMOS devices connected to the supply or NMOS devices connected to ground [11]. Let us classify the former PMOS-mirror topologies as Type-A topologies, and the latter as Type-B. In the following analysis, it will become apparent that the implementation of the current-mirror is critical in determining the PSR of the error amplifier, and therefore the regulator. In this analysis, \( V_{dd} \) and \( V_{out-A} \) are the ac ripples at the supply and the output of the amplifier, respectively. The internal capacitances of the amplifiers have been ignored for simplicity and since they are negligible when compared to the high device capacitances of the large output power device. The analysis also assumes that transconductance of all the devices (\( g_m \)) is much greater than their channel conductance (\( g_{ds} \)), which is typical in analog IC design (channel lengths are larger than the minimum).

1) Type-A Topologies

Consider a typical example of the Type-A architecture, namely, the conventional error amplifier as shown in Fig. 4(b), which consists of an NMOS input differential pair and a PMOS current-mirror load connected to the supply. The small signal PSR model of this circuit is presented in Fig. 4(a). The model is obtained by grounding the two inputs to the amplifier and applying a small signal source at the input supply (\( v_{ss} \)). \( R_1 \) and \( R_2 \) represent the channel resistances of the PMOS and NMOS devices, respectively. The current-dependent current source \( i_{R2} \), which reflects the current flowing through resistor \( R_2 \) into the output, models the effect of the current mirror. Assuming the \( 1/g_m \) resistance (of the diode-connected PMOS device) is much smaller when compared against \( R_2 \), which is typically the case, the supply ripple is entirely reflected at the output,

\[
V_{out-A} = V_{dd} \left( \frac{R_2}{R_1 + R_2} \right) + i_{R2} \left( \frac{R_1}{R_2} \right)
\]

A similar result is reported in [2], where it was found that, for this amplifier topology, the entire supply ripple was transferred to the output over a wide frequency range.

![Fig. 4. (a) Small signal model for PSR of Type A error amplifiers, (b), (c), and (d) Examples of Type A error amplifiers.](image-url)
the model presented in Fig. 5(a). Hence, from Fig. 5 and (10), it can be seen that their small signal PSR model corresponds to (c) and (d) Examples of Type A error amplifiers.

Figs. 5(c) and (5d) depict two other examples of the Type-B topology of the folded type using NMOS current-mirror loads. As in Type-A topologies, on observing that the signals at \( v_c \) and \( v_i \) are common mode with respect to the input differential pair, it can be seen that their small signal PSR model corresponds to the model presented in Fig. 5(a). Hence, from Fig. 5 and (10), it is evident that Type-B topologies shield their respective outputs from ripples in the supply.

C. General Design Guidelines for High PSR

Most LDO topologies use a PMOS pass device at the output because it exhibits a low forward drop (and consequently a low power loss across the device). Type-A error amplifiers, as it turns out, conduct nearly the entire ripple at the supply to their output. Having the ripples at the gate and source equal in magnitude and phase makes the supply ripple common-mode, thereby canceling any feedthrough. Type-B amplifiers in source follower type power devices shield the gate and therefore the source and output from any supply ripple.

IV. RESULTS FROM SAMPLE DESIGN

The design principles from Sections II and III were used to design a monolithic low-drop out regulator having the specifications presented in Table 2. The process technology is 0.35\( \mu \)m TSMC CMOS. The output voltage of 1.2V is typical of many low-voltage applications. Many of these applications, like EPROMs and DRAMs, do not require large currents and hence a typical value for the maximum output current of 20mA has been chosen. Since a completely integrated design is required, the value of the required capacitance should lend itself easily to fabrication. Towards this aim, the value of the maximum allowable total capacitance of 150 pF has been chosen.

### TABLE 2. CIRCUIT AND PROCESS PARAMETERS FOR A LOW DROP-OUT REGULATOR DESIGN.

<table>
<thead>
<tr>
<th>Circuit Parameter</th>
<th>Value</th>
<th>Process Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>3.3 V</td>
<td>( K_p' )</td>
<td>65 ( \mu )A/V(^2)</td>
</tr>
<tr>
<td>( V_{out} )</td>
<td>1.2 V</td>
<td>( K_p' )</td>
<td>185 ( \mu )A/V(^2)</td>
</tr>
<tr>
<td>PSR @ dc</td>
<td>-70 dB</td>
<td>(</td>
<td>V_{in}</td>
</tr>
<tr>
<td>PSR @ 1MHz</td>
<td>-20 dB</td>
<td>( V_{in} )</td>
<td>0.61 V</td>
</tr>
<tr>
<td>Dropout @ I_{out} = 20mA</td>
<td>300 mV</td>
<td>( C_{out} )</td>
<td>4 fF/( \mu )m(^2)</td>
</tr>
<tr>
<td>( C_{out} )</td>
<td>&lt; 150 pF</td>
<td>( \lambda_n = \lambda_p )</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Fig. 5. (a) Small signal model for PSR of Type A error amplifiers, (b), (c), and (d) Examples of Type A error amplifiers.

The low drop-out voltage specifications necessitated the use of a PMOS output stage, and hence a Type-A amplifier. For the sake of simplicity, the conventional amplifier of Fig. 4(b) was chosen. The schematic of the LDO design is presented in Fig. 6.

The small signal equivalent of the circuit was then analyzed for PSR, in a manner similar to [11]. Only the large device capacitances of the output device were considered in the analysis. If \( A_{dc-A} \) and \( G_{m-A} \) are the dc gain and output conductance of the amplifier, respectively, and \( C_{g} \) is the total gate-drain capacitance, including compensating Miller capacitor \( C_m \), the PSR transfer function is given by (11). The dc gain, zero, and poles of this transfer function are

\[
PSR = \frac{V_{out-A}}{V_{in}} = \frac{s(g_{m-A} + G_{m-A})C_{g}}{s^2 C_{out} C_{g} + s(G_{m-A} C_{out} + C_{g}) + (g_{ds} + g_{m} - G_{m-A})C_{g}} + G_{m-A} g_{m} + G_{m-A} g_{ds}
\]

The assumptions made in the analysis above are that \( g_{m} \) is much
greater than $g_{ds}$ for all devices, $g_{ds}$ is much greater than $G_{o-A}$, and $g_{ds}C_{gd}$ is much greater than $g_{ds}C_{gs}$, $G_{o-A}C_{out}$ (due the large size of he series pass device). These assumptions are reasonable for a typical low-power regulator using a large series pass device and large compensating capacitors relative to device capacitances.

Fig. 7 illustrates both the simulated and the analytical PSR, along with the simulated open-loop gain of the regulator. The SPICE simulations, which used BSIM3 models, show a strong correlation between the open-loop gain and the PSR of the regulator and agree very well with the analytical results, which were obtained through MATLAB. Fig. 7 also shows the simulated PSR in the absence of $C_{out}$ – the degradation in the PSR at high frequencies can easily be noted through the absence of the second PSR pole, $p_2$.

Table 3 compares the results of the analysis performed in the previous section to the results of a similar analysis performed for regulators consisting of a PMOS output stage with a Type B Error amplifier and an NMOS output stage with Type A and Type B amplifiers. It is evident that Type-A (Type-B) amplifiers provide much higher dc PSRR than their Type-B (Type-A) counterparts for PMOS (NMOS) devices. Another way to view this result is as follows: the Type-A amplifier can meet the dc PSRR specifications of an LDO regulator with a lower gain than a Type-B topology. This would make the Type-A amplifier a preferred choice in many CMOS applications, where low voltage headroom makes the design of high-gain amplifiers a challenge [8]-[10]. It must be noted, however, that in applications where a high PSRR bandwidth is required at the expense of dc PSRR, the Type-B amplifier is a more suitable choice since its dominant PSRR breakpoint (zero) lies at a higher frequency ($z_1 = p_{o-A}g_{ms}g_{ds}$) than for the conventional error amplifier case ($z_1 = p_{o-A}$).

V. CONCLUSIONS

A simple, intuitive voltage divider model for the PSR of a typical linear regulator is used to accurately describe the PSR performance of linear regulators. The PSR at low frequencies, the dominant PSR breakpoint where performance starts to degrade, and three subsequent breakpoints are determined by the dc open-loop gain, the error amplifier bandwidth, the unity-gain frequency, the output pole of the regulator, and the ESR zero, respectively. A closer examination of the PSR of a regulator reveals that amplifiers that employ mirrors connected to supply to produce a supply-correlated ripple at the gate of the PMOS output device (thereby making the ripple common-mode) are best suited for LDO applications with high PSR performance, while amplifiers that use mirrors connected to ground to attenuate the supply ripple at their output are optimal for driving an NMOS output device (since the gate, and hence, source, is now free from output ripple). A better PSR bandwidth, at the cost of dc PSR, can be obtained by interchanging the amplifiers in the two cases. A strong relationship between the PSR and open-loop gain of a linear regulator has been established from which design principles critical to obtaining high PSR performance have been proposed.

REFERENCES