Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications

Vishal Gupta [1], Student Member, IEEE, Gabriel A. Rincón-Mora [1], Senior Member, IEEE, and Prasun Raha [2], Member, IEEE

Email: vishalg@ece.gatech.edu

[1] Georgia Tech Analog and Power IC Design Lab, Georgia Institute of Technology, [2] Texas Instruments Inc.

ABSTRACT

Linear regulators are critical analog blocks that shield a system from fluctuations in supply rails and the importance of determining their Power Supply Rejection (PSR) performance is magnified in SoC systems, given their inherently noisy environments. In this work, a simple, intuitive, voltage divider model is introduced to analyze the PSR of linear regulators, from which design guidelines for obtaining high PSR performance are derived. The PSR of regulators that use PMOS output stages for low drop-out (LDO), crucial for modern low-voltage systems, is enhanced by error amplifiers which present a supply-correlated ripple at the gate of the PMOS pass device. On the other hand, amplifiers that suppress the supply ripple at their output are optimal for NMOS output stages since the source is now free from output ripple. A better PSR bandwidth, at the cost of dc PSR, can be obtained by interchanging the amplifiers in the two cases. It has also been proved that the dc PSR, its dominant frequency breakpoint (where performance starts to degrade), and three subsequent breakpoints are determined by the dc open-loop gain, error amplifier bandwidth, unity-gain frequency (UGF) of the system, output pole, and ESR zero, respectively. These results were verified with SPICE simulations using BSIM3 models for the TSMC 0.35 µm CMOS process from MOSIS.

I. INTRODUCTION

The close proximity of analog and digital circuits in SoC environments can cause them to be overwhelmed by spurious switching noise signals propagated through supply lines, interface nodes, and substrate injection [1], [2]. In these VLSI and ULSI circuits, voltage regulators form an indispensable component of the power management system. They generate stable voltages while supplying a wide range of currents to a variety of circuits. They also filter the fluctuations in the power supply, thereby shielding their load circuits from supply ripple. Thus, in circuits like DRAMs [3], PLLs [4], [5], and EPROMs [6], where power supply noise directly translates to degradation in system performance, power supply rejection is a key figure of merit for a voltage regulator. It is therefore imperative to analyze the PSR of linear regulators over a large frequency range with the aim of establishing design guidelines and principles for high PSR performance. Further, as systems aggressively advance towards integration, these state-of-the-art regulators rely increasingly on on-chip capacitors (10-200 pF) for frequency compensation [3]-[7]. These capacitors do not consume expensive board-space and are not associated with a significant equivalent series resistance (ESR). Since the regulators do not use an external capacitor to establish the dominant low-frequency pole, they are termed "internally compensated regulators". It must be noted, however, that the effects of ESR still warrant discussion, since they become important when the connectivity to the plates of the capacitor is limited by the dense routing requirements of the chip.

II. PSR OF A TYPICAL LINEAR REGULATOR

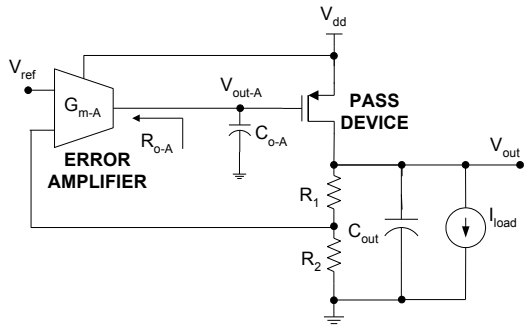

Fig. 1. Block diagram of typical linear regulator (pass device may be PMOS or NMOS).

Fig. 1 depicts the block diagram of a typical regulator consisting of an error amplifier, a pass device and an output capacitor, C_{out} [3]-[10]. The regulator supplies a variable current to the load circuit through the pass device while maintaining a constant output voltage due to a feedback loop formed by the potential divider created by resistors R_1 and R_2 ($\beta = R_2/(R_1+R_2)$) and the amplifier. The amplifier is characterized by its transconductance G_{m-A}, high output resistance, R_{o-A} ($R_{o-A} \equiv 1/G_{o-A}$), and corresponding pole, p_{o-A} ($f_{p-oA} \equiv 1/2\pi R_{o-A}C_{o-A}$). The large series pass device (NMOS or PMOS) has a transconductance g_m and low drain-source resistance r_{ds} ($r_{ds} \equiv 1/g_{ds}$). Bias resistors, R_1 and R_2, that form the feedback network through a potential divider, are typically very large ($R_1+R_2 >> r_{ds} = 1/I_{load}\lambda$) for low quiescent power consumption. Though this model is a very accurate representation of a linear regulator, it does not offer an intuitive picture into the origin of the PSR frequency response – a measure of the supply ripple transferred to the output.

A. Simple Model for PSR of Linear Regulators

In its simplest form, the PSR transfer function (a ratio of the output to the supply ripple) can be viewed as the effect of a voltage divider caused by an impedance between the supply and the regulator output and an impedance between the output and ground. An intuitive and insightful model for analyzing the PSR of a typical linear regulator is presented in Fig. 2. This model consists of an impedance ladder comprising of the channel resistance of the pass device (r_{ds}), and a parallel combination of the open-loop output resistance to ground (z_o) and the shunting effect of the feedback loop (z_{o-reg}). Hence, referring to Fig. 1 and Fig. 2, we can see that

$$z_o = \left(z_{Cout} + R_{ESR}\right) \| \left(R_1 + R_2\right), \tag{1}$$

and,

$$z_{o-reg} = \frac{z_o \,||\, r_{ds}}{A_{ol}\beta}. \quad (2)$$

The model is presented in Fig. 2. Thus, by simplifying the model in Fig. 1 to the one in Fig. 2, the PSR can be seen to be

$$PSR = \frac{v_{out}}{v_{dd}} = \frac{(z_o \,||\, z_{o-reg})}{r_{ds} + (z_o \,||\, z_{o-reg})}. \quad (3)$$

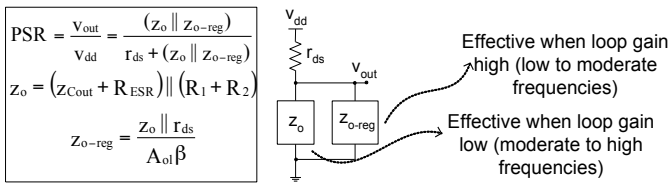

Fig. 2. Intuitive model for PSR in action at various frequencies.

B. Model in Action over Wide Frequency Range

Fig. 3 depicts the sketch of a typical PSR curve and how the intuitive model allows us to determine the PSR performance of a linear regulator over a large range of frequencies, simply by accounting for the frequency dependence of z_o and z_{o-reg}.

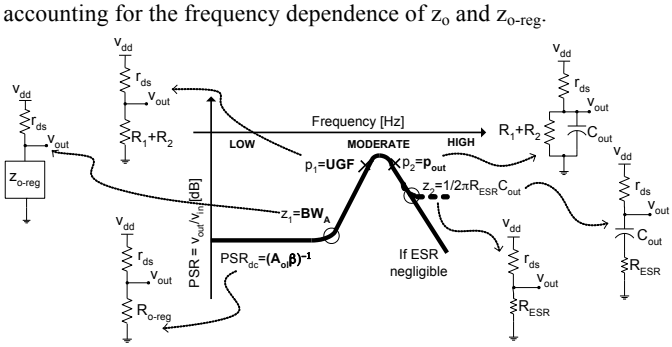

Fig. 3. Simple model in action over wide frequency range.

1) DC and Low Frequencies

At low frequencies, the high loop gain ($A_{ol-dc}\beta$) allows z_{o-reg} to shunt z_o, and since r_{ds} is, for the most part, significantly lower than R_1+R_2, the following simplification can be derived:

$$PSR_{dc} \approx \frac{R_{o-reg}}{r_{ds} + R_{o-reg}} = \frac{\dfrac{r_{ds} \,||\, (R_1 + R_2)}{A_{ol-dc}\beta}}{r_{ds} + \dfrac{r_{ds} \,||\, (R_1 + R_2)}{A_{ol-dc}\beta}} \approx \frac{\dfrac{r_{ds}}{A_{ol-dc}\beta}}{r_{ds} + \dfrac{r_{ds}}{A_{ol-dc}\beta}} \approx \frac{1}{A_{ol-dc}\beta}. \quad (4)$$

Consequently, the PSR of the regulator is intimately related to the open-loop gain of the system.

2) Moderate Frequencies

The shunting effect of the feedback loop, however, deteriorates at frequencies beyond the bandwidth of the amplifier, BW_A (or dominant pole, p_{o-A}), thereby causing an increase in the regulated output impedance, z_{o-reg}. This leads to a rise in the output ripple and, consequently, the dominant PSR breakpoint in the form of a PSR zero (z_1). The resultant degradation in the PSR can been obtained by replacing A_{ol-dc} in (4) with the bandwidth-limited response of the loop at frequencies where A_{ol-dc} is greater than one i.e. between dc and the unity-gain frequency (UGF) of the system. This leads to

$$PSR|_{f \le UGF} \approx \frac{z_{o-reg}}{r_{ds} + z_{o-reg}} = \frac{r_{ds}}{(A_{ol}\beta)\, r_{ds} + r_{ds}} = \frac{r_{ds}}{1 + \dfrac{A_{ol-dc}}{BW_A s}\beta\, r_{ds} + r_{ds}}$$
$$= \frac{p_{o-A}}{(1 + A_{ol-dc}\beta)\left[1 + \dfrac{s}{(1 + A_{ol-dc}\beta)\, p_{o-A}}\right]} \approx \frac{r_{ds}}{(A_{ol-dc}\beta)\left(1 + \dfrac{s}{UGF}\right)}. \quad (5)$$

The presence of a PSR pole (p_1) at the unity-gain frequency, as predicted by (5), can be easily understood when we note that the deterioration of the PSR due to increasing closed-loop output resistance ceases at the UGF. At this stage, the shunting effect of the feedback loop no longer exists and the PSR is determined simply by the frequency-independent resistive divider between the channel resistance of the pass device (r_{ds}) and bias resistors (R_1+R_2). The PSR is given by

$$PSR|_{f=UGF} \approx \frac{z_o}{z_o + r_{ds}} = \frac{R_1 + R_2}{R_1 + R_2 + r_{ds}} \approx 1. \quad (6)$$

At these frequencies, the PSR of the system is the weakest since the closed loop output resistance is not decreased by the feedback loop and the output capacitor cannot shunt the output ripple to ground.

3) High Frequencies

When the output capacitor starts shunting (R_1+R_2) to ground, a smaller ripple appears at the output, thereby causing an improvement in the PSR (since z_o decreases with increasing frequency) and the second PSR pole (p_2). Thus,

$$PSR|_{f>UGF} \approx \frac{z_o}{z_o + r_{ds}} = \frac{z_{Cout}}{z_{Cout} + r_{ds}}. \quad (7)$$

The effectiveness of the output capacitor is, however, restricted by its ESR. At very high frequencies, since this capacitor is an "ac short", z_o is determined by the ESR, which limits PSR to

$$PSR|_{f>>UGF} \approx \frac{z_o}{z_o + r_{ds}} \approx \frac{R_{ESR}}{R_{ESR} + r_{ds}}, \quad (8)$$

thereby leading to the formation of an effective PSR zero at z_2 = $1/2\pi R_{ESR}C_{out}$. Fig. 3 shows a sketch of the poles and zeros of a typical PSR curve predicted by this model.

Though the simple model depicted in Fig. 2 provides an intuitive understanding of the relationship between PSR and the open-loop gain of the regulator, it does not take into account the effect of the conduction of the supply ripple through the amplifier itself. This ripple feedthrough has significant implications for high PSR design and is critical for determining the optimal amplifier topology for a particular type of output stage. Before analyzing the PSR of the error amplifier, let us discuss the mechanism of ripple conduction through the output stage, or series pass device of the regulator. Then, the design of the amplifier will be considered.

III. Designing for High PSR

A. Series Pass Device

In applications where low drop-out is not a primary concern, the output stage of the regulator is often an NMOS device. Despite the relatively large voltage headroom required to drive

the gate due to its gate-source voltage drop, the NMOS device, acting as a source follower, offers an inherently low output impedance, making the compensation of the regulator easier than its low drop-out counterpart [6], [7]. It is evident that in this follower configuration, the NMOS device will conduct the ripple present at its gate directly to its output, the source. Hence, to keep the ripple at the output node low, it is crucial to design the preceding error amplifier such that the ripple at the gate of the NMOS device is as small as possible.

In most low voltage applications today, however, a PFET transistor is used as the output series pass device [8]-[10] because of the driving requirements of its gate. In this configuration, the gain from the source of the device (connected to V_{dd}) to its drain, has the same magnitude as the gain from its gate to its drain, i.e., $g_m r_{ds}$. However, the two gain paths are out of phase. Hence, in order to cancel the feedthrough of the power supply ripple from the source, the preceding amplifier should provide a correlated ripple at the gate of the PMOS device ($V_{SG} = V_S - V_G = \delta_{Vdd} - \delta_{Vdd} = 0$). In other words, the supply ripple should appear as a common-mode signal at the gate and the source.

B. PSR of the Error Amplifier

Most error amplifiers that have a single-ended output use a current-mirror load to perform double-to-single-ended conversion and add the ac signals obtained from the input differential pair to a single-ended signal. This mirror may be implemented in the form of PMOS devices connected to the supply or NMOS devices connected to ground [11]. Let us classify the former PMOS-mirror topologies as Type-A topologies, and the latter as Type-B. In the following analysis, it will become apparent that the implementation of the current-mirror is critical in determining the PSR of the error amplifier, and therefore the regulator. In this analysis, v_{dd} and $v_{out\text{-}A}$ are the ac ripples at the supply and the output of the amplifier, respectively. The internal capacitances of the amplifiers have been ignored for simplicity and since they are negligible when compared to the high device capacitances of the large output power device. The analysis also assumes that transconductance of all the devices (g_m) is much greater than their channel conductance (g_{ds}), which is typical in analog IC design (channel lengths are larger than the minimum).

1) Type-A Topologies

Consider a typical example of the Type-A architecture, namely, the conventional error amplifier as shown in Fig. 4(b), which consists of an NMOS input differential pair and a PMOS current-mirror load connected to the supply. The small signal PSR model of this circuit is presented in Fig. 4(a). The model is obtained by grounding the two inputs to the amplifier and applying a small signal source at the input supply (v_{dd}). R_1 and R_2 represent the channel resistances of the PMOS and NMOS devices, respectively. The current-dependent current source (i_{R2}), which reflects the current flowing through resistor R_2 into the output, models the effect of the current mirror. Assuming the $1/g_m$ resistance (of the diode-connected PMOS device) is much smaller when compared against R_2, which is typically the case, the supply ripple is entirely reflected at the output,

$$v_{out-A} = v_{dd}\left(\frac{R_2}{R_1+R_2}\right) + i_{R2}\left(R_1 \parallel R_2\right)$$
$$\approx v_{dd}\left(\frac{R_2}{R_1+R_2}\right) + \frac{v_{dd}}{R_2}\left(\frac{R_1 R_2}{R_1+R_2}\right) = v_{dd}. \quad (9)$$

A similar result is reported in [2], where it was found that, for this amplifier topology, the entire supply ripple was transferred to the output over a wide frequency range.

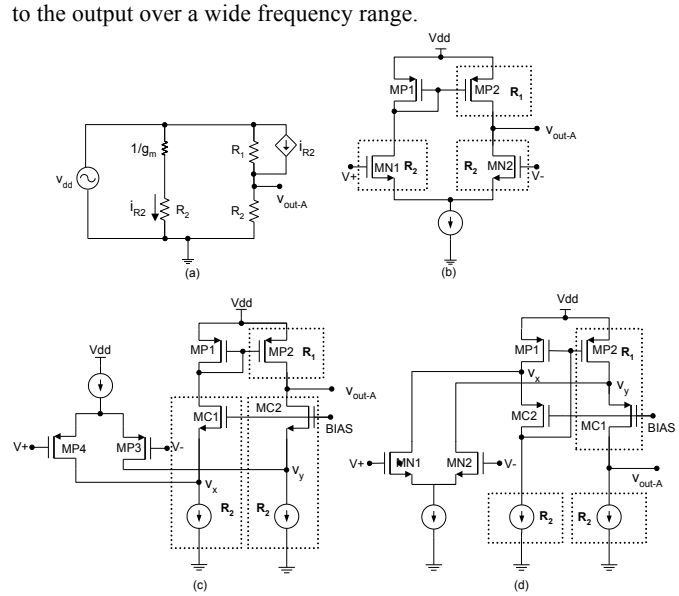

Fig. 4. (a) Small signal model for PSR of Type A error amplifiers, (b), (c), and (d) Examples of Type A error amplifiers.

Figs. 4(c) and 4(d) present two other examples of Type-A structures of the folded type with PMOS current-mirror loads. Noting that the signals at v_x and v_y are both common-mode with respect to the differential pair, they "cancel out" and the effect of the input differential pair is therefore nullified. Hence, the small signal PSR models of these error amplifiers corresponds to the same model presented in Fig. 4(a), which was analyzed earlier and described with (9). The devices represented by resistors R_1 and R_2 are depicted in dashed boxes in Figs. 4(b)-(d). Thus, from Fig. 4 and (9), it can be established that the supply ripple appears at the output unattenuated for Type-A topologies.

2) Type-B Topologies

Fig. 5(b) illustrates a conventional error amplifier consisting of a PMOS differential input pair and an NMOS current-mirror load connected to ground. This is a typical example of a Type-B topology. As in the model for Type-A topologies discussed earlier, the small signal PSR model of this circuit can be constructed by grounding the inputs, neglecting the ($1/g_m$) resistance of the diode-connected NMOS device (when compared against the channel resistance of the PMOS device), and modeling the current-mirror as a current-dependent current source connected between the output and ground. This model is presented in Fig. 5(a). The derivation of the transfer-function $v_{out\text{-}A}/v_{dd}$ reveals that no ac ripple appears at the output, theoretically isolating the output from the input supply ripple,

$$v_{out-A} = v_{dd}\left(\frac{R_2}{R_1+R_2}\right) - i_{R1}\left(R_1 \| R_2\right)$$

$$= v_{dd}\left(\frac{R_2}{R_1+R_2}\right) - \frac{v_{dd}}{R_1}\left(\frac{R_1 R_2}{R_1+R_2}\right) = 0. \quad (10)$$

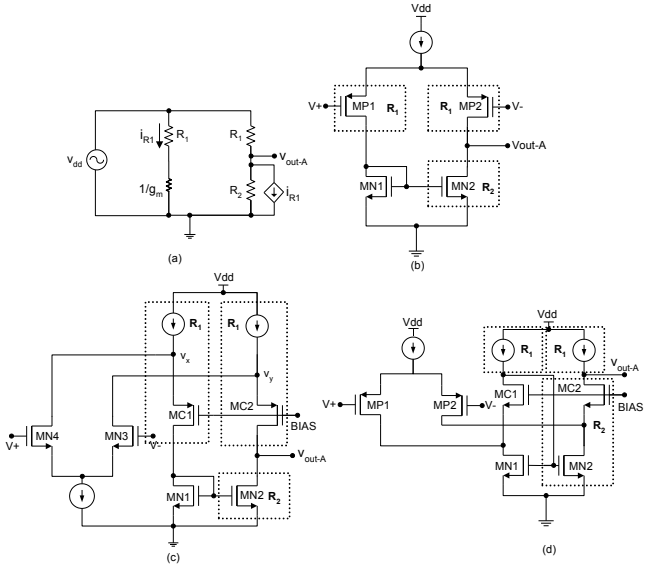

Fig. 5. (a) Small signal model for PSR of Type A error amplifiers, (b), (c), and (d) Examples of Type A error amplifiers.

Figs. 5(c) and 5(d) depict two other examples of the Type-B topology of the folded type using NMOS current-mirror loads. As in Type-A topologies, on observing that the signals at v_x and v_y are common mode with respect to the input differential pair, it can be seen that their small signal PSR model corresponds to the model presented in Fig. 5(a). Hence, from Fig. 5 and (10), it is evident that Type-B topologies shield their respective outputs from ripples in the supply.

C. General Design Guidelines for High PSR

Most LDO topologies use a PMOS pass device at the output because it exhibits a low forward drop (and consequently a low power loss across the device). Type-A error amplifiers, as it turns out, conduct nearly the entire ripple at the supply to their output. Having the ripples at the gate and source equal in magnitude and phase makes the supply ripple common-mode, thereby canceling any feedthrough. Type-B amplifiers in source follower type power devices shield the gate and therefore the source and output from any supply ripple.

IV. Results from Sample Design

The design principles from Sections II and III were used to design a monolithic low drop-out regulator having the specifications presented in Table 2. The process technology is 0.35μm TSMC CMOS. The output voltage of 1.2V is typical of many low-voltage applications. Many of these applications, like EPROMs and DRAMs, do not require large currents and hence a typical value for the maximum output current of 20mA has been chosen. Since a completely integrated design is required, the value of the required capacitance should lend itself easily to fabrication. Towards this aim, the value of the maximum allowable total capacitance of 150 pF has been chosen.

TABLE 2. Circuit and process parameters for a low drop-out regulator design.

Circuit Parameter	Value	Process Parameter	Value
VDD	3.3 V	K_p'	65 μA/V^2
V_{out}	1.2 V	K_n'	185 μA/V^2
PSR @ dc	-70 dB	$\|V_{tp}\|$	0.74 V
PSR @ 1MHz	-20 dB	V_{tn}	0.61 V
Dropout @ I_{load} = 20mA	300 mV	C_{ox}	4 fF/μm^2
C_{out}	< 150 pF	$\lambda_n = \lambda_p$	0.1

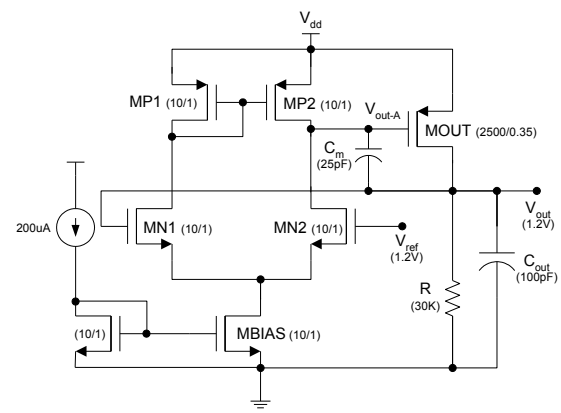

Fig. 6. Schematic of LDO using PMOS output device and conventional OTA.

The low drop-out voltage specifications necessitated the use of a PMOS output stage, and hence a Type-A amplifier. For the sake of simplicity, the conventional amplifier of Fig. 4(b) was chosen. The schematic of the LDO design is presented in Fig. 6. The small signal equivalent of the circuit was then analyzed for PSR, in a manner similar to [11]. Only the large device capacitances of the output device were considered in the analysis. If A_{dc-A} and G_{o-A} are the dc gain and output conductance of the amplifier, respectively, and C'_{gd} is the total gate-drain capacitance, including compensating Miller capacitor C_m, the PSR transfer function is given by (11). The dc gain, zero, and poles of this transfer function are

$$PSR_{dc} \approx \frac{G_{o-A}}{G_{m-A}}\frac{g_{ds}}{g_m} = \frac{g_{ds}}{g_m}\frac{1}{A_{dc-A}} = \frac{1}{g_m r_{ds}}\frac{1}{A_{dc-A}} = \frac{1}{A_{ol-dc}}, \quad (12)$$

$$z_1 \approx -\frac{G_{o-A}\, g_{ds}}{g_m C'_{gd}} = -\frac{1}{R_{o-A}(g_m r_{ds} C'_{gd})} = p_{o-A} = BW_A, \quad (13)$$

$$p_1 \approx -\frac{G_{m-A} g_m + G_{o-A} g_{ds}}{G_{o-A}(C_{out} + C'_{gd}) + (g_{ds} + g_m - G_{m-A}) C'_{gd}} \approx -\frac{G_{m-A}}{C'_{gd}} = UGF, \quad (14)$$

and

$$p_2 \approx -\frac{G_{o-A}(C_{out} + C'_{gd}) + (g_{ds} + g_m - G_{m-A}) C'_{gd}}{C_{out} C'_{gd}} \approx \frac{g_m}{C_{out}} = p_{out}, \quad (15)$$

The assumptions made in the analysis above are that g_m is much

$$PSR = \frac{v_{out}}{v_{dd}} \approx \frac{s(g_m + G_{o-A}) C'_{gd} + G_{o-A}\, g_{ds}}{s^2 C_{out} C'_{gd} + s(G_{o-A}(C_{out} + C'_{gd}) + (g_{ds} + g_m - G_{m-A}) C'_{gd}) + G_{m-A}\, g_m + G_{o-A}\, g_{ds}} \quad (11)$$

greater than g_{ds} for all devices, g_{ds} is much greater than $G_{o\text{-}A}$, and $g_m C'_{gd}$ is much greater than $g_{ds}C_{gs}$, $G_{o\text{-}A}C_{out}$ (due the large size of he series pass device). These assumptions are reasonable for a typical low-power regulator using a large series pass device and large compensating capacitors relative to device capacitances.

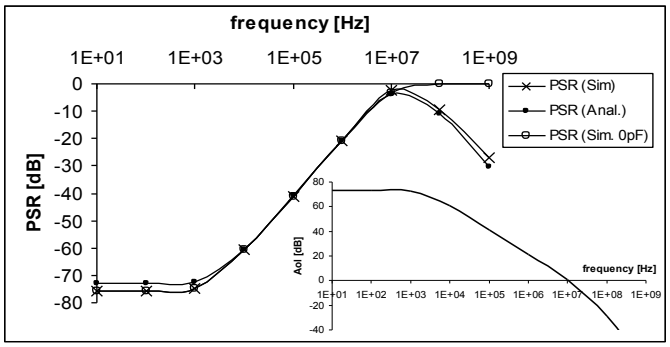

Fig. 7. PSR performance comparison of simulated and analytical results for PSR for regulator using PMOS pass device (inset shows open loop gain).

Fig. 7 illustrates both the simulated and the analytical PSR, along with the simulated open-loop gain of the regulator. The SPICE simulations, which used BSIM3 models, show a strong correlation between the open-loop gain and the PSR of the regulator and agree very well with the analytical results, which were obtained through MATLAB. Fig. 7 also shows the simulated PSR in the absence of C_{out} – the degradation in the PSR at high frequencies can easily be noted through the absence of the second PSR pole, p_2, the output pole.

TABLE 3. ANALYTICAL EXPRESSIONS FOR POLES AND ZEROS OF THE PSR OF TYPICAL REGULATOR TOPOLOGIES IN TERMS OF THEIR OPEN LOOP CHARACTERISTICS (p_1=UGF AND p_2=p_{OUT} FOR ALL TOPOLOGIES)

Pass Device	Error amplifier	$\lvert PSR \rvert_{dc}$	z_1	High dc PSR	High PSR BW
PMOS	Type-A	$G_{m-A} R_{o-A} g_m r_{ds}$	$p_{o\text{-}A}$	√	
	Type-B	$G_{m-A} R_{o-A}$	$g_m r_{ds} p_{o-A}$		√
NMOS	Type-A	$G_{m-A} R_{o-A}$	$g_m r_{ds} p_{o-A}$		√
	Type-B	$G_{m-A} R_{o-A} g_m r_{ds}$	$p_{o\text{-}A}$	√	

Table 3 compares the results of the analysis performed in the previous section to the results of a similar analysis performed for regulators consisting of a PMOS output stage with a Type B Error amplifier and an NMOS output stage with Type A and Type B amplifiers. It is evident that Type-A (Type-B) amplifiers provide much higher dc PSRR than their Type-B (Type-A) counterparts for PMOS (NMOS) devices. Another way to view this result is as follows: the Type-A amplifier can meet the dc PSRR specifications of an LDO regulator with a lower gain than a Type-B topology. This would make the Type-A amplifier a preferred choice in many CMOS applications, where low voltage headroom makes the design of high-gain amplifiers a challenge [8]-[10]. It must be noted, however, that in applications where a high PSRR bandwidth is required at the expense of dc PSRR, the Type-B amplifier is a more suitable choice since its dominant PSRR breakpoint (zero) lies at a higher frequency ($z_1 = p_{o\text{-}A} g_m r_{ds}$) than for the conventional error amplifier case ($z_1 = p_{o\text{-}A}$).

V. CONCLUSIONS

A simple, intuitive voltage divider model for the PSR of a typical linear regulator is used to accurately describe the PSR performance of linear regulators. The PSR at low frequencies, the dominant PSR breakpoint where performance starts to degrade, and three subsequent breakpoints are determined by the dc open-loop gain, the error amplifier bandwidth, the unity-gain frequency, the output pole of the regulator, and the ESR zero, respectively. A closer examination of the PSR of a regulator reveals that amplifiers that employ mirrors connected to supply to produce a supply-correlated ripple at the gate of the PMOS output device (thereby making the ripple common-mode) are best suited for LDO applications with high PSR performance, while amplifiers that use mirrors connected to ground to attenuate the supply ripple at their output are optimal for driving an NMOS output stage (since the gate, and hence, source, is now free from output ripple). A better PSR bandwidth, at the cost of dc PSR, can be obtained by interchanging the amplifiers in the two cases. A strong relationship between the PSR and open-loop gain of a linear regulator has been established from which design principles critical to obtaining high PSR performance have been proposed.

REFERENCES

[1] M. S. J, Steyaert, W. M. C. Sansen, "Power supply rejection ratio in operational transconductance amplifiers," IEEE Trans. Circuits Sys., vol. 37, pp. 1077-1084, Sept. 1990.

[2] E. Säckinger, J. Goette, W. Guggenbűl, "A general relationship between amplifier parameters, and its application to PSRR improvement," IEEE Trans. Circuits Sys., vol. 38, pp. 1173-1181, Oct. 1991.

[3] H. Tanaka, M. Aoki, T. Sakata, S.Kimura, N. Sakashita, H. Hidaka, T. Tachibana, and K. Kimura, "A precise on-chip voltage generator for a gigascale DRAM with a negative word-line scheme," IEEE Jour. of Solid-State Circuits, vol. 34, pp. 1084-1090, Aug. 1999.

[4] V.R. von Kaenel, "A high-speed, low-power clock generator for a microprocessor application," IEEE Jour. of Solid-State Circuits, vol. 33, pp.1634-1639, Nov. 1998.

[5] C.Lee, K. McClellan, and J. Choma Jr., "A supply-noise-insensitive CMOS PLL with a voltage regulator using dc-dc capacitive converter," IEEE Jour. of Solid-State Circuits, vol. 36, pp. 1453-1463, Oct. 2001.

[6] J. Shor, Y. Sofer, Y. Polansky, and E. Maayan, "Low power voltage regulator for EPROM applications," in Proc. IEEE Intl. Symp. Circuits and Sys., 2002, pp. 56-579.

[7] G.W. den Besten and B. Nauta, "Embedded 5V-to-3.3V voltage regulator for supplying digital IC's in 3.3V CMOS technology," IEEE Jour. of Solid-State Circuits, vol. 33, pp. 956-962, July 1998.

[8] V. Balan, "A low-voltage regulator circuit with self-bias to improve accuracy," IEEE Jour. Solid State Circuits, vol. 38, pp. 365-368, Feb. 2003.

[9] S. Yuan, and B. C. Kim, "Low dropout voltage regulator for wireless applications," in 33rd IEEE PESC, 2002, pp. 421-424.

[10] H. Shin, S. Reynolds, K. Wrenner, T. Rajeevakumar, and S. Gowda, "Low-dropout on-chip voltage regulator for low-power circuits," in IEEE Symp. Low Power Electronics, 1994, pp. 76-77.

[11] P.E. Allen and D.R. Holberg, CMOS Analog Circuit Design. New York, NY: Oxford University Press, 2002.