Nested Hysteretic Current-mode Single-inductor Multiple-output (SIMO) Boosting Buck Converter

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***Abstract*—Portable microsystems, which typically incorporate transceivers, analog/digital converters, microprocessors, and others, require several fast on-chip supplies to both function and save energy. Linear regulators are fast and compact, but also lossy, and although switched inductors are efficient, power inductors are bulky, which is why supplying several functions with one inductor is often an optimal compromise. Responding quickly to individual disruptions, however, is challenging when sharing one inductor with other loads, and bucking and boosting the battery voltage normally require more power switches. The 1.25-MHz single-inductor multiple-output (SIMO) converter presented here employs a buck stage to buck and boost 3.6 V to 0.8, 1.2, and 4.5 V and uses nested hysteretic current-mode control to respond within 1 µs to 20-mA load dumps across 0.8 and 1.2 V and 2 µs to 5-mA load dumps across 4.5 V. Simulations show that efficiency peaks at 91% with a combined load of 45 mA.**

***Index Terms*—Single inductor, multiple output, hysteretic, current mode, dc–dc switching converter, cross regulation**

I. Powering Microsystems

Wireless microsensors and other portable electronics can add performance-enhancing and energy-saving intelligence to large infrastructures, like the power grid, and inaccessible places, like the human body [1]. However, powering the transmitter, sensor interface, processor, and other functions shown in Fig. 1 requires several efficient supplies that can source µW to mW at voltages above and below the battery. Since disabling components and scaling voltages save energy [2] and reduce latency [3], the supplies must also sustain load-power transitions that are both vast and fast.

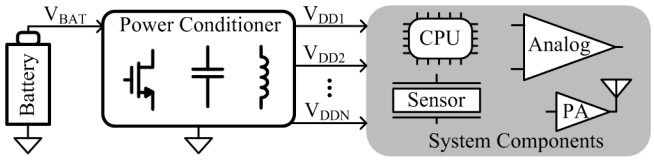

Fig. 1. Typical wireless microsensor.

Whereas linear regulators are fast, compact, low noise, and lossy, switched inductors are slow, bulky, noisy, and efficient, which is why dedicating linear regulators to sensitive subsystems and supplying them from one common switching converter is a popular compromise. However, because linear circuits cannot boost, having one master rail means many milliamp linear regulators drop considerable voltages. Even across 100 – 200 mV, they often consume more power than switched inductors. Therefore, the aim of this research is to eliminate linear regulators by accelerating the response time of a switched inductor that supplies several bucked and boosted outputs. For this, the single-inductor multiple-output (SIMO) supply presented in Section III employs a nested hysteretic current-mode control strategy that energizes and de-energizes the inductor in the manner described in Section II with the performance demonstrated in Section IV, from which Section V draws final conclusions.

II. SIMO Switching Sequence

A. Dedicated Energy Packets

One way of transferring input energy to all loads is to send dedicated energy packets to each output, as Fig. 2a shows. Each subsystem therefore receives power from, essentially, a conventional single-output converter [4]. This way, if all outputs draw sufficient power, current i_L can flow continuously through the inductor: in continuous-conduction mode (CCM). If load power drops below a threshold, the inductor can de-energize fully after every packet in discontinuous-conduction mode (DCM). Because LC complex-conjugate poles reduce to one left-half-plane pole in DCM, some researchers emulate DCM operation when load power is high by momentarily short-circuiting the inductor after each packet. Under these pseudo-DCM (PDCM) conditions [5], i_L flattens momentarily at dc offset I_{OS}, as i_L would at 0 A in DCM. The drawback to PDCM is the power lost across the switch that shorts the inductor is substantial.

B. Shared Energy Packet

Another way of using one inductor to supply several outputs is by drawing all the energy necessary to supply all outputs once and delivering fractions of the packet to each output. In other words, the converter directs i_L to one output at a time, switching to the next output in the sequence after fully satisfying the first. As with dedicated packets, the total power drawn determines whether the inductor conducts continuously in CCM, discontinuously in DCM, or continuously in PDCM, as Fig. 2b illustrates.

C. Comparison

Of these two schemes, sharing one energy packet amongst all outputs suffers more cross-regulation effects because drawing more energy from one output necessarily diminishes what subsequent loads can receive. In fact, many implementations of this technique rely on this dependence to determine when to stop supplying power to a particular load. Energizing the inductor only once, however, means energizing switches lose gate-drive energy only once per

cycle, or if sending smaller packets more frequently, then each output receives energy more often, which means each output can respond to load dumps more quickly.

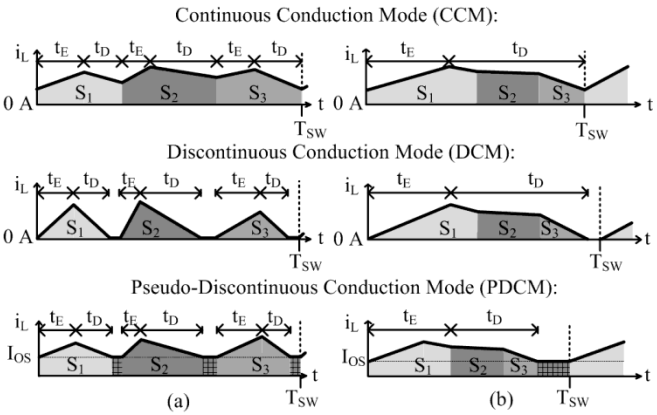

Fig. 2. Delivering (a) dedicated and (b) shared energy packets.

What is less obvious is that sharing one packet allows buck-derived SIMOs to boost and boost SIMOs to buck [6]. Recall that conventional one-output bucks cannot boost because the input must energize the inductor to a lower voltage. In the case of the buck-conceived SIMO in Fig. 3, however, inductor L_O energizes to bucked output v_{O1}, and if insufficient, L_O further energizes to bucked output v_{O2}. As long as L_O draws enough energy while connected to v_{O1} and v_{O2} across energizing time t_{EN} of the switching period T_{SW}:

$$t_{EN} < t_{O1} + t_{O2} \equiv \sum t_{O(BUCK)}\,, \tag{1}$$

L_O can later drain to a boosted output like v_{O3} because, when switching node v_{SW} connects to 0 V, a boosted output, like a bucking one, reverses L_O's polarity. In fact, because L_O's average voltage $v_{L(AVG)}$ is zero, $v_{SW(AVG)}$ equals $v_{SW.O(AVG)}$:

$$v_{SW(AVG)} = V_{IN}D_{EN} = v_{SW.O(AVG)} = v_{O1}D_1 + v_{O2}D_2 + v_{O3}D_3\,, \tag{2}$$

so v_{O3} can be higher than V_{IN} if $v_{O3}t_{O3}/T_{SW}$ or $v_{O3}D_3$ are a fraction of $V_{IN}t_{EN}/T_{SW}$ or $V_{IN}D_{EN}$.

Ultimately, L_O must draw sufficient energy from the bucked outputs to supply the boosted counterpart. Thankfully, boosting an output that draws less power than all bucked outputs is often all a system requires. For this reason, and because refreshing all outputs more often amounts to higher bandwidth, bucked and boosted outputs in the foregoing design share every energy packet.

III. Current-mode Feedback Control

The ultimate aim of a supply is to regulate its output voltages to prescribed targets across load levels. As in one-output bucks, however, the inductor (e.g., L_O in Fig. 3) and output capacitors in the feedback loops of multiple-output converters introduce a pair of complex poles. Regulating L_O's i_L so its bandwidth surpasses the system's unity-gain frequency f_{0dB} ensures the loops perceive L_O to be a current source (with a constant gain) below f_{0dB}. As such, the pole pair reduces to one pole and the system is stable because its loop gain reaches f_{0dB} after only one pole: at –20 dB/dec.

A. Current Loop

As in typical bucks, regulating i_L's peak or average by pulse-width modulating (PWM) the connectivity of L_O [7–9] is possible. The drawback is that the loop requires several clock cycles to respond to disruptions. In other words, i_L's bandwidth $f_{I.0dB}$ is below switching frequency f_{SW} and the system's bandwidth f_{0dB} is even lower. Regulating i_L with a hysteretic loop is faster because, if a disruption pushes i_L past its window limits, the loop reacts at once [10], which means switching period T_{SW} shortens and $f_{I.0dB}$ nears f_{SW}.

The system in [11] employs a hysteretic loop to control i_L, except a phased-locked loop (PLL) fixes T_{SW}, which means i_L must wait until the end of T_{SW} to react. Instead, comparator CP_I in the proposed converter of Fig. 3 responds almost immediately to disruptions in i_L via the voltage i_L sets across R_S. Because the voltage loops regulate v_{O1}, v_{O2}, and v_{O3} to their respective targets V_{R1}, V_{R2}, and V_{R3} and their loop gains are negligible at $f_{I.0dB}$, the outputs equal their targets near $f_{I.0dB}$: $\Sigma v_O - \Sigma V_R$ nears zero. So, since R_F and C_F average $i_L R_S$ to $i_{L(AVG)}R_S$, CP_I reacts to instantaneous variations in $i_L R_S$ relative to $V_{IL(AVG)}$.

B. Voltage Loops

Employing PWM to regulate the output voltages of a multiple-output system at a fixed f_{SW} is possible [7–8, 12], except again, each loop requires multiple cycles to respond to load disruptions. Instead, in the proposed converter of Fig. 3, CP_I discerns errors to start energizing L_O asynchronously with v_{START} by connecting L_O only to v_{O1}. Then, comparator CP_{O1} waits until i_L charges C_{O1} to its target V_{R1}, so if the load pulls v_{O1} below V_{R1} in midstream, CP_{O1} extends how long L_O connects to v_{O1} (i.e., t_{O1}). After satisfying v_{O1}, CP_{O1} resets flip-flop FF_1 to disconnect L_O from v_{O1} (via S_1) and

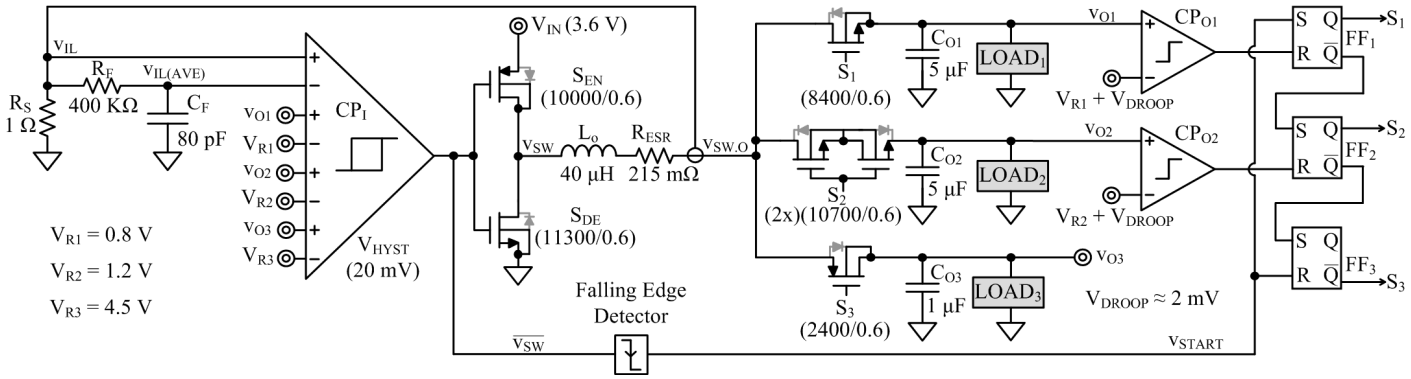

Fig. 3. Proposed nested hysteretic current-mode buck-derived single-inductor multiple-output dc–dc converter with bucked and boosted outputs.

subsequently connect L_O to v_{O2} (with S_2). Similarly, comparator CP_{O2} directs i_L to output capacitor C_{O2} until v_{O2} reaches target V_{R2}, after which CP_{O2} prompts S_2 and S_3 to disconnect L_O from v_{O2} and connect L_O to v_{O3}. Since i_L at low frequency is $i_{L(AVG)}$ (i.e., $i_L R_S$ equals $i_{L(AVG)} R_S$) and CP_{O1} and CP_{O2} regulate v_{O1} and v_{O2} to V_{R1} and V_{R2}, CP_I, whose feedback effect is to reduce the sum of its inputs to zero, regulates v_{O3} to V_{R3}:

$$\left(i_L R_S - i_{L(AVG)} R_S + \sum v_O - \sum V_R\right)\Big|_{\text{Low Frequency}} \approx v_{O3} - V_{R3} \to 0 . \quad (3)$$

C. Load-dump Droop Compensation

Because CP_{O1} redirects i_L to the next output when v_{O1} reaches V_{R1}, v_{O1} droops until the next cycle, when L_O reconnects to v_{O1}, as Fig. 4 shows. In other words, load i_O pulls v_O below V_R when S_1 is open (across t_{OFF} or $D_1'T_{SW}$) to establish what amounts to a load-regulation offset V_{OS}:

$$V_{OS} = \Delta v_O = \frac{i_C t_{OFF}}{C_O} = \frac{i_O D_1' T_{SW}}{C_O} = \frac{i_O (1 - D_1) T_{SW}}{C_O} . \quad (4)$$

Rather than a defect, this offset, which is also present in v_{O2}, as is in [15], can reduce the error that load dumps cause in v_O. For example, raising V_R above v_O's actual target by 2% for load dumps that produce 4% variations induces v_O to fall 4% from $1.02V_R$ to $0.98V_R$ and rise 4% from $0.98V_R$ to $1.02V_R$, as Fig. 4 demonstrates. As a result, v_O remains within ±2% of its actual target instead of the ±4% that rising and falling load dumps would have induced when V_{OS} is 0 V.

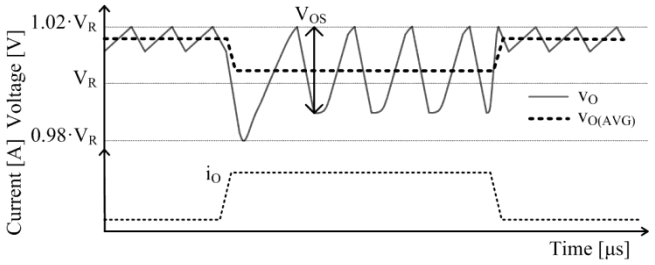

Fig. 4. Reducing load-dump errors with droop compensation.

V_{DROOP} in the proposed converter of Fig. 3 implements droop compensation for v_{O1} and v_{O2}. Here, V_{DROOP} raises v_{O1}'s and v_{O2}'s respective references V_{R1} and V_{R2} so v_{O1} and v_{O2} rise above V_{R1} and V_{R2} by 2 mV, which corresponds to half their load-dump variations. This way, the system keeps v_{O1} and v_{O2} within ±2 mV of V_{R1} and V_{R2}. In general, adjusting V_{DROOP} to half the load-dump effect keeps output variations to half their load-dump counterparts.

IV. Performance

A. Steady State

Fig. 5 displays the steady-state waveforms of i_L, v_{O1}, v_{O2}, and v_{O3} from the 0.6-µm CMOS implementation of Fig. 3 when loaded with 40, 20, and 10 mA, respectively, supplied from V_{IN} at 3.6 V, and configured to buck and boost 0.8, 1.2, and 4.5 V. Note the state of the art from Table I could either buck or boost, but not both. These operating conditions caused the system to switch at 1.25 MHz and produce 3-, 2-, and 7-mV ripples at v_{O1}, v_{O2}, and v_{O3}, respectively. For this, L_O connected to v_{O1} for 0.46 µs, v_{O2} for 0.21 µs, and v_{O3} for 0.13 µs of the 0.8-µs period. L_O's connectivity to v_{O1} is longer than the others because v_{O1}'s load is the heaviest at 40 mA.

B. Load-dump Response

When v_{O1}'s load i_{O1} suddenly rises from 20 to 40 mA, v_{O1} slews below V_{R1} before v_{O1} recovers in 0.3 µs and settles in 3 µs, as Fig. 6 shows, which is 27 µs faster than [9] in Table I, which is a comparable system. Because i_{O1} is higher after the rising load dump, v_{O1}'s steady-state ripple Δv_{O1} rises accordingly from 1.6 to 3 mV. Similarly, because Δv_{O1} drops when i_O decreases, the falling load dump causes v_{O1}'s ripple to diminish about V_{R1}, reaching steady state in 3 µs. Since v_{O3} does not have a dedicated comparator with which to implement droop compensation, v_{O3} in Fig. 7 falls 8 mV and rises 6 mV before v_{O3} recovers within 3 µs from rising and falling 5-mA load dumps and completely settles in 50 µs.

Table I: Operating Performance

Parameters	This SIMO	[7]	[9]
f_{SW}	1.25 MHz	1 MHz	1 MHz
V_{IN}	2.7 – 4.2 V	2.7 – 4.5 V	2.7 – 3.6 V
V_O	0.8, 1.2, 4.5 V	4.58, –6.24 V	1.8, 1.2 V
Ripple	3, 2, 7 mV	15, 5 mV	< 16 mV
Response Time	Buck: 3 µs (20 mA) Boost: 50 µs (5 mA)	60 µs (40 mA)	30 µs
Peak Efficiency	91%	82%	91%

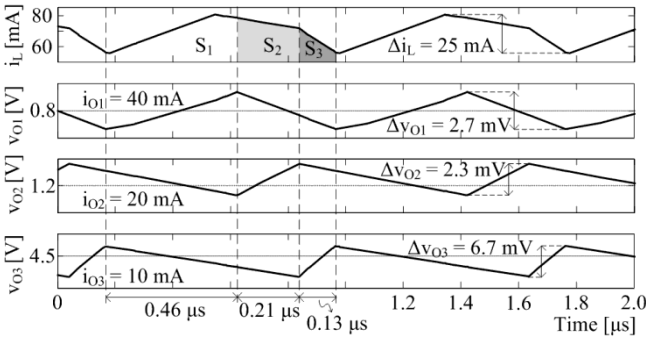

Fig. 5. Steady-state waveforms when loaded with 40, 20, and 10 mA.

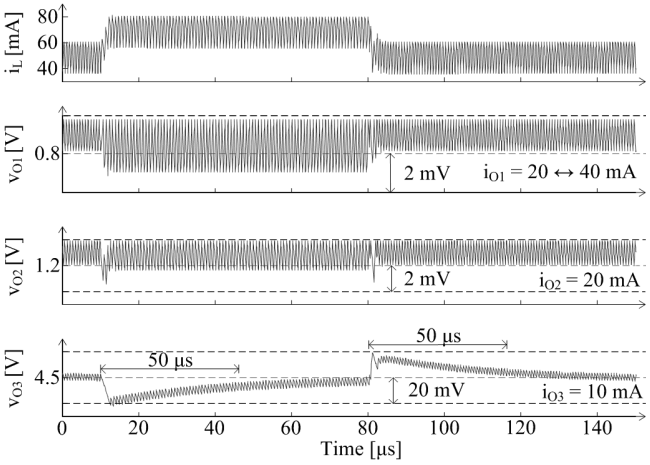

Fig. 6. v_{O1}'s load-dump response and v_{O2} and v_{O3}'s cross-regulation effects.

C. Cross Regulation

In waiting for v_{O1} to rise to V_{R1} and v_{O2} to rise to V_{R2} before re-connecting L_O, the system cross-regulates the outputs. As such, load dumps have forward rippling effects. A rising load dump at v_{O1}, for example, extends v_{O1}'s connection to L_O, so v_{O2} and v_{O3} droop longer, as Fig. 6 corroborates, and settle to their steady-state conditions in 3 and 50 µs, respectively. A falling load dump at v_{O1}, however, does not affect v_{O2} because CP_{O2} disconnects L_O as soon as v_{O2} reaches V_{R2}. Because v_{O1}'s load suddenly falls, though, L_O carries more energy than v_{O3} requires, so v_{O3} rises 20 mV above V_{R3} and settles in 50 µs.

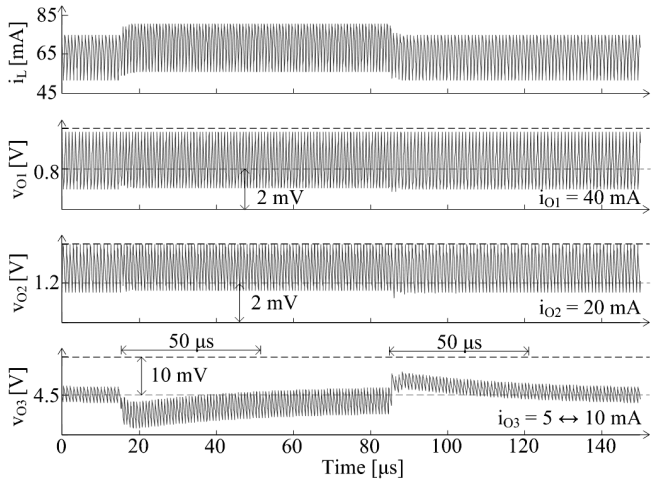

Fig. 7. v_{O3}'s load-dump response and v_{O1} and v_{O2}'s cross-regulation effects.

Again, because v_{O3} waits for v_{O2} and v_{O2} for v_{O1}, load-dump effects do not ripple in reverse. A load dump at v_{O3}, for example, has minimal impact on v_{O1} and v_{O2} in Fig. 7 because L_O satisfies v_{O1} and v_{O2} before suffering the effects of i_{O3}. Similarly, a load dump at v_{O2} ripples only to v_{O3}. This also means v_{O1} and v_{O2} respond faster to load dumps than v_{O3} because the system favors v_{O1} and v_{O2} over v_{O3}.

D. Efficiency

Since power switches in Fig. 3 consume conduction power P_C and V_{IN} supplies gate-drive power P_{GD} to charge their gates, the power stage's power-conversion efficiency η is

$$\eta \equiv \frac{P_O}{P_{IN}} = \frac{P_O}{P_O + P_C + P_{GD}} = \frac{\Sigma v_O i_O}{\Sigma v_O i_O + P_C + P_{GD}}. \quad (5)$$

P_C balances P_{GD} when combined load current Σi_O is 45 mA, so η in Fig. 8 peaks at 91%. η falls when Σi_O rises above 45 mA because P_C increases with Σi_O. η also falls when Σi_O drops below 45 mA because P_O drops below P_{GD} and P_{GD}, which is now the dominant loss, does not scale with Σi_O when the converter is in CCM with a near constant f_{SW}.

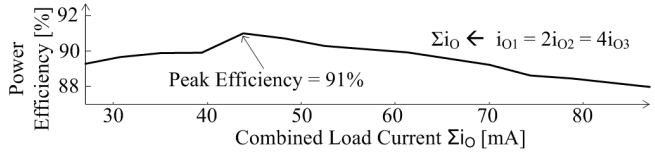

Fig. 8. Power efficiency across combined load current Σi_O.

V. Conclusions

The 90-mA buck-derived single-inductor multiple-output (SIMO) supply shown bucks and boosts 3.6 V to 0.8, 1.2, and 4.5 V with 3-, 2-, and 7-mV ripples, respectively, and 91% peak power efficiency. The converter can both buck and boost as long as the inductor energizes only to bucked outputs, so buck power must surpass boost power. Boosting with a buck stage is important because buck- and boost-only systems require fewer switches than buck–boost stages, so efficiency is higher. Plus, since this system uses hysteretic loops to control the inductor current and all outputs, the supplies respond to load dumps in 1 – 3 µs. This response time is notable because sharing one inductor inherently slows the system. This system, in fact, further reduces the accuracy error that response time produces with droop compensation.

Acknowledgement

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