Maximum DC–DC Conversion in Switched-Inductor Power Supplies

Qiwei Chen, *Graduate Student Member*, *IEEE*, and Gabriel A. Rincón-Mora, *Fellow*, *IEEE*
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, U.S.A.
aren_chen@gatech.edu and rincon-mora@gatech.edu

***Abstract*—High DC–DC voltage conversion is crucial in many emerging fields. However, the maximum achievable voltage conversion of switched-inductor power supplies (SLPS) has been a lingering question. This paper first establishes the inversely proportional relationship between minimum duty cycle and maximum conversion ratio in ideal SLPS. Then, how propagation delays limit the minimum duty cycle is found. The difference between actual and ideal duty cycle, caused by losses in the power stage, is analyzed. By translating delay-limited minimum duty cycle and loss-induced duty cycle shift into ideal SLPS's duty cycle, the maximum conversion of any actual SLPS can be determined. The paper also discusses the dominant loss for duty cycle shift at different operating conditions and the loading effect of losses. For validation, a buck and a boost example are simulated with SPICE. In summary, this paper presents expressions and insights to analyze and understand maximum DC–DC conversion of SLPS.**

Keywords—Propagation delay, power losses, maximum voltage gain, voltage translation, buck–boost, extreme duty ratio.

I. DC–DC Conversion in Power-Supply Systems

Power supplies are essential for all systems that require external electrical power to operate. DC–DC power supplies are designed to sustain a constant voltage or current from a constant input voltage, examples of which are shown in Fig. 1.

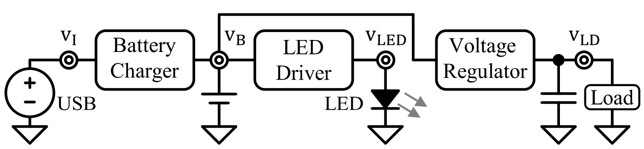

Fig. 1. Types of power DC–DC power supplies.

Many emerging fields, such as USB power delivery, electric vehicle, and computation center, require power supplies to step-up or step-down voltages by high ratios. Most literatures on high DC–DC conversion power supplies utilized cascaded power stages, such as multiple switched-inductors [1]–[3], or switched-inductor/capacitor hybrid [4]–[12]. They all need additional components and usually more complex control schemes compared to standalone switched-inductor power supplies (SLPS) [13]–[19]. However, these costs for high DC–DC conversion applications remain unjustified unless the conversion exceeds the capability of SLPS. Past discussions have touched upon some factors' impact on voltage conversion of certain SLPS [4], [20]–[24]. But the general conversion limit of SLPS is largely unexplored in the state-of-the-art.

In this paper, theory to find maximum DC–DC conversion ratio of SLPS is developed and validated with simulation. Section II introduces the operation and maximum conversion ratio of ideal SLPS, while Section III and IV explain how propagation delay and power losses impose limitation on real systems. Section V reveals the approach to find realistic maximum DC–DC conversion ratio and provides simulation validation of the theory, and Section VI concludes the paper.

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II. Switched-Inductor DC–DC Conversion

A. Operation

In SLPS, the switched-inductor L_X serves as an energy storage device that receives and delivers energy in alternating energize and drain phases, as shown in Fig. 2. Across energize time t_E, inductor voltage v_L includes input voltage v_I, and in drain time t_D, it includes output voltage v_O to supply the load from source.

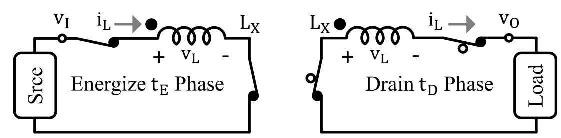

Fig. 2. Phases of switched-inductor.

As Fig. 3 shows, in steady state, across conduction time t_C, v_L switches between ideal energize voltage v_E' during t_E and ideal drain voltage v_D' during t_D, keeping an average v_L of 0 V. Meanwhile, inductor current i_L rises and falls by the same ripple current Δi_L that can be calculated with:

$$\Delta i_L = t_E\left(\frac{di_L}{dt_E}\right) = t_E\left(\frac{v_E'}{L_X}\right) = t_D\left(\frac{v_D'}{L_X}\right). \tag{1}$$

The ideal energize duty cycle d_E', the t_E fraction of t_C, can also be represented by v_E' and v_D', and it sums to 1 with the ideal drain duty cycle d_D':

$$d_E' \equiv \frac{t_E}{t_C} = \frac{t_E}{t_D+t_E} = \frac{v_D'}{v_E'+v_D'} \equiv 1 - d_D'. \tag{2}$$

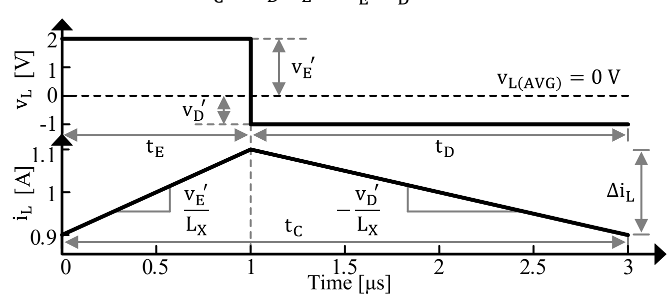

Fig. 3. Simulated switched-inductor waveforms.

B. Conversion Ratio

As (2) shows, v_D' exceeds v_E' when d_E' is above 50 % and *vice versa*. An ideal buck-boost converter, shown in Fig. 4(a), can convert-up or convert-down v_E' to v_D', which are v_I and v_O, as shown in Table I. Buck or boost converter in Fig. 4(b) or (c) are variations of buck-boost, with the absence of output or input switches. Their v_O's can only be lower or higher than v_I.

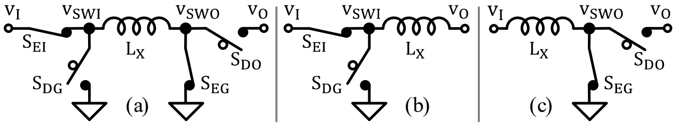

Fig. 4. Ideal (a) buck–boost, (b) buck, and (c) boost converters.

TABLE I. IDEAL VOLTAGES AND DUTY RATIOS

	v_E'	v_D'	d_I'	d_O'
Buck–Boost	v_I	v_O	d_E'	d_D'
Buck	$v_I - v_O$	v_O	d_E'	1
Boost	v_I	$v_O - v_I$	1	d_D'

The up or downward conversion ratio $K_{V(\downarrow/\uparrow)}$ from v_I to v_O is always larger than 1 V/V. The input and output switching node voltages (v_{SWI} and v_{SWO}) are duty-cycle fractions of v_I and v_O. Since $v_{L(AVG)}$ is 0 V, v_{SWI} and v_{SWO} have the same average value. $K_{V(\downarrow/\uparrow)}$ is then the ratio between d_I' and d_O', the duty cycles of L_X connecting to v_I and v_O respectively:

$$K_{V(\downarrow/\uparrow)} \equiv \frac{v_{I/O}}{v_{O/I}} = \left(\frac{v_{SWI/O(AVG)}}{d_{I/O}'}\right)\left(\frac{d_{O/I}'}{v_{SWO/I(AVG)}}\right) = \frac{d_{O/I}'}{d_{I/O}'}. \quad (3)$$

C. Conversion Limit

The maximum conversion ratio $K_{V(\downarrow/\uparrow)}^{MAX}$ would then be the ratio between maximum and minimum d_I' or d_O'. By variable substitution, it can be expressed with only minimum $d_{E/D}'$, or d_{MIN}' in short, for buck–boost (BB), buck (BK), and boost (BS):

$$K_{V(\downarrow/\uparrow)}^{MAX} = \frac{d_{O/I(MAX)}'}{d_{I/O(MIN)}'} = \underbrace{\frac{1-d_{E/D(MIN)}'}{d_{E/D(MIN)}'}}_{K_{V(BB)}^{MAX}} \approx \underbrace{\frac{1}{d_{E/D(MIN)}'}}_{K_{V(BK/BS)}^{MAX}} \equiv \frac{1}{d_{MIN}'}. \quad (4)$$

III. DELAY LIMIT

It is now established that d_{MIN}' is the limiting factor for $K_{V(\downarrow/\uparrow)}^{MAX}$. Ideally, d_{MIN}' can approach 0 % and $K_{V(\downarrow/\uparrow)}^{MAX}$ can approach ∞. However, in an actual system, there is a minimum energize or drain duty cycle provided to the switches, d_{MIN}.

A. Control Loop

Fig. 5 shows a simplified control loop diagram of SLPS, where the properties to be controlled, such as v_O or i_O, are sensed and fed to the circuits that process the information into a control signal v_{EO}. The duty cycler then translates v_{EO} into an alternating duty cycle command v_G' that the driver uses to turn the switches on and off. In steady state, the feedback signal and v_{EO} are constant, while the duty cycler and the driver operate switches at $d_{E/D}$, with d_{MIN} possible.

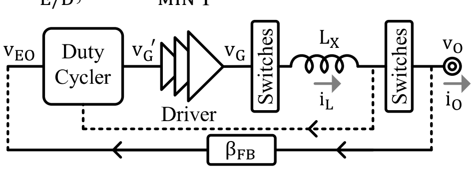

Fig. 5. Typical feedback loop in SL power supplies.

B. Discontinuous-Conduction Mode

In Discontinuous-Conduction Mode (DCM), t_C is a fraction of the switching period t_{SW}. After the drain phase, i_L remains at 0 until the next t_{SW} begins. As Fig. 6 shows, even with minimum energize time $t_{E(MIN)}$, d_E can still decrease with t_C extending into the zero-current period. The same applies to decreasing d_D.

So, d_{MIN} limit is not reached until t_C approaches t_{SW}, and the operation is hastened to Continuous-Conduction Mode (CCM).

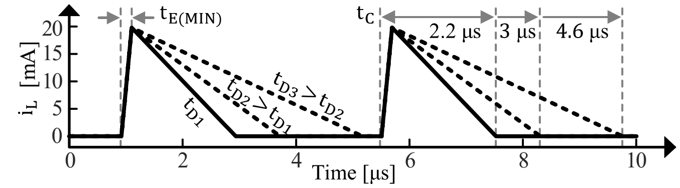

Fig. 6. Simulated conduction times.

C. Continuous-Conduction Mode

In CCM, t_C equals t_{SW}, and d_{MIN} is dependent on $t_{SW(MAX)}$ and $t_{E/D(MIN)}$. For a component with propagation delay t_P, it can only reproduce inputs no shorter than t_P, as Fig. 7 shows.

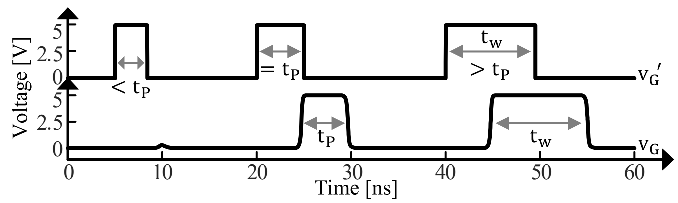

Fig. 7. Simulated pulse widths.

In order to provide a valid signal at the switches, v_{EO} should contain information of $t_{E/D}$ longer than any individual propagation delay $t_{P(x)}$ between v_{EO} and the switches. However, the rising and falling propagation delay of a component, t_P^+ and t_P^-, may vary from each other by:

$$t_{P\Delta} \equiv t_P^+ - t_P^-. \quad (5)$$

Fig. 8 shows waveforms of two drivers that have $t_{P\Delta}$ of opposite signs. A negative or a positive $t_{P\Delta}$ extends or shortens the active-high energize signal, subtracting itself from the pulse width. Similarly, $t_{P\Delta}$ adds itself to an active-low drain pulse.

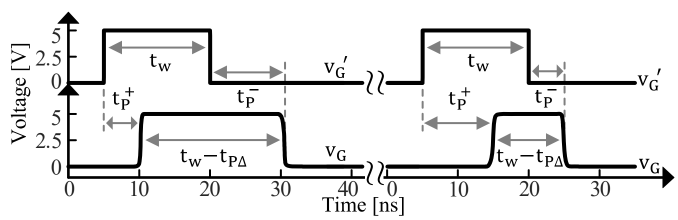

Fig. 8. Simulated asymmetric delays.

Therefore, the longest $t_{P(x)}$, or $t_{P(MAX)}$, and the sum of all the subsequent $t_{P\Delta}$, or $t_{P\Sigma\Delta}$, determine $t_{E/D(MIN)}$. So d_{MIN} is:

$$d_{MIN} = \frac{t_{E/D(MIN)}}{t_{SW(MAX)}} = \frac{\mathrm{Max}\{t_{P(x)}\} \mp \Sigma_{j>x} t_{P\Delta(j)}}{t_{SW(MAX)}} \equiv \frac{t_{P(MAX)} \mp t_{P\Sigma\Delta}}{t_{SW(MAX)}}, \quad (6)$$

assuming $t_{P\Sigma\Delta}$ is subtracted from active-high t_E and added to active-low t_D. However, different control methods of SLPS could impose some variations on (6).

PWM Loop: In Pulse-Width Modulation (PWM) control, the duty cycler has a fixed t_{SW}. In this scheme, d_{MIN} is determined solely by $t_{E/D(MIN)}$, or the delays. The expression for d_{MIN} would be (6) with a constant denominator t_{SW}.

Valley/Peak Loop: t_E or t_D can be designed to be constant in valley or peak loop. Such, $d_{E(MIN)}$ in valley loop and $d_{D(MIN)}$ in peak loop are limited by $t_{SW(MAX)}$, or the lowest switching frequency f_{SW} allowed before the control loop's response time and stability is impacted by f_{SW} approaching the unity gain frequency. In this case, the numerator in (6) should be constant $t_{E/D}$. In the alternative case that variable t_D or t_E is very short and t_{SW} is close to the preset t_E or t_D, (6) shows approximate expression of d_{MIN} when the denominator is constant $t_{E/D}$.

Hysteretic Loop: The power supplies can also be controlled by limiting i_L within a window. Since the enegize or drain actions are administered whenever i_L reaches the boundaries, there is no preset $t_{E/D}$ or t_{SW}. Hence, (6) is accurate.

IV. Power-Loss Duty Cycle Shift

Though $\mathrm{d_{MIN}}$ can be found with delays, (4) cannot be directly applied to a real, lossy system in which $\mathrm{v_L}$ is altered. This section analyzes the effects of power losses on a synchronous buck–boost shown in Fig. 9. Since buck and boost are buck–boost without certain components, their losses are naturally included in this analysis. Output capacitor $\mathrm{C_O}$ and its series resistance $\mathrm{R_C}$ may not always be present in all SLPS.

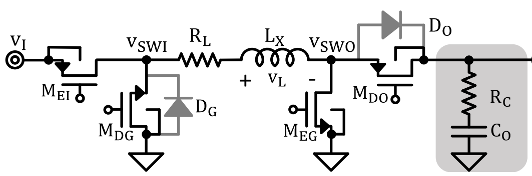

Fig. 9. Power stage of buck–boost converter.

A. Conduction-Path Losses

Across $\mathrm{t_E}$, current flows in the direction of $\mathrm{v_E}'$. Losses along the conduction path reduces $\mathrm{v_E}'$ into $\mathrm{v_E}$, the actual $\mathrm{v_L}$ during $\mathrm{t_E}$:

$$\mathrm{v_E} \approx \mathrm{v_E}' - \mathrm{i_{L(AVG)}}\mathrm{R_E} - \mathrm{v_{IV(E)}}, \tag{7}$$

where $\mathrm{R_E}$ is the resistance in energize path and $\mathrm{v_{IV(E)}}$ is the average energize voltage reduced by switches' current-voltage (IV) overlap transient. As left of Fig. 10 shows, when $\mathrm{v_{GS}}$ rises to $\mathrm{v_{TH}}$, $\mathrm{M_{EG}}$'s $\mathrm{v_{DS}}$ falls about linearly as the switch closes. Across interval $\mathrm{t_{V(E)}}$, $\mathrm{v_E}$ is reduced by the average voltage $\mathrm{v_{DS}}$ traverses, $0.5(\mathrm{v_O} + \mathrm{v_{DO}})$. Similarly, $\mathrm{v_{DS}}$ of $\mathrm{M_{EI}}$ traversing through $\mathrm{v_I} + \mathrm{v_{DG}}$ contribute to a lower $\mathrm{v_E}$. We can then derive:

$$\mathrm{v_{IV(E/D)}} \approx \left(\frac{\mathrm{t_{V,EI(E/D)}}}{\mathrm{t_{E/D}}}\right)\left(\frac{\mathrm{v_I}+\mathrm{v_{DG}}}{2}\right) + \left(\frac{\mathrm{t_{V,EG(E/D)}}}{\mathrm{t_{E/D}}}\right)\left(\frac{\mathrm{v_O}+\mathrm{v_{DO}}}{2}\right), \tag{8}$$

where $\mathrm{v_{DG}}$ and $\mathrm{v_{DO}}$ are diode voltages of $\mathrm{D_G}$ and $\mathrm{D_O}$, which can have different values for Silicon, Schottky, or MOS diode. The IV overlap effects of $\mathrm{M_{DG}}$ and $\mathrm{M_{DO}}$ are negligible as their $\mathrm{v_{DS}}$'s traverse only $\mathrm{v_{DG}}$ and $\mathrm{v_{DO}}$ across short $\mathrm{t_V}$'s.

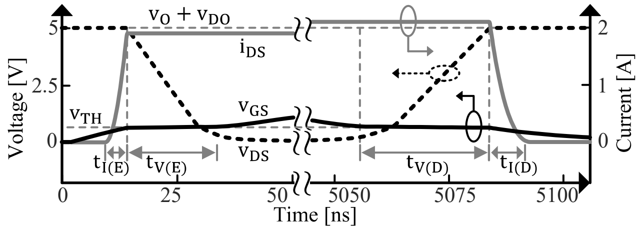

Fig. 10. Simulted transitions of $\mathrm{M_{EG}}$.

Across $\mathrm{t_D}$, current flows in the reverse direction of $\mathrm{v_D}'$. The effects of drain path resistance $\mathrm{R_D}$, additional diode voltages during dead time $\mathrm{t_{DT}}$, and IV overlap transients raises $\mathrm{v_D}'$ to $\mathrm{v_D}$:

$$\mathrm{v_D} \approx \mathrm{v_D}' + \mathrm{i_{L(AVG)}}\mathrm{R_D} + \mathrm{v_{DT(D)}} - \mathrm{v_{IV(D)}}. \tag{9}$$

$\mathrm{v_{DT(D)}}$ in (10) shows the average effect of diode drops on $\mathrm{v_D}$ during $\mathrm{t_{DT}}$. In the case of an asynchronous system, $\mathrm{R_D}$ contains no resistance of $\mathrm{M_{DG}}$ and $\mathrm{M_{DO}}$, and $2\mathrm{t_{DT}}$ equals $\mathrm{t_D}$ in:

$$\mathrm{v_{DT(D/SW)}} = \left(\frac{2\mathrm{t_{DT}}}{\mathrm{t_{D/SW}}}\right)(\mathrm{v_{DG}} + \mathrm{v_{DO}}). \tag{10}$$

As right of Fig. 10 shows, after $\mathrm{M_{EG}}$'s $\mathrm{v_{GS}}$ drops to $\mathrm{v_{TH}}$, $\mathrm{v_{DS}}$ does not rise instantaneously but linearly across $\mathrm{t_{V(D)}}$, reducing $\mathrm{v_D}$. This effect of $\mathrm{M_{EG}}$ and $\mathrm{M_{EI}}$'s IV overlap is $\mathrm{v_{IV(D)}}$ in (8).

B. Energize Duty-Cycle Shift

The energize duty cycle in a lossy system can then be expressed in terms of the actual $\mathrm{v_E}$ and $\mathrm{v_D}$ applied on $\mathrm{L_X}$:

$$\mathrm{d_E} = \frac{\mathrm{v_D}}{\mathrm{v_E}+\mathrm{v_D}} \approx \frac{\mathrm{v_D}'+\mathrm{i_{L(AVG)}}\mathrm{R_D}+\mathrm{v_{DT(D)}}-\mathrm{v_{IV(D)}}}{\mathrm{v_E}'+\mathrm{v_D}'+\mathrm{i_{L(AVG)}}(\mathrm{R_D}-\mathrm{R_E})+\mathrm{v_{DT(D)}}-\mathrm{v_{IV(D)}}-\mathrm{v_{IV(E)}}}, \tag{11}$$

and the shift in energize duty cycle between lossy and lossless system, under identical $\mathrm{v_E}'$ and $\mathrm{v_D}'$, would be:

$$\Delta\mathrm{d_E} = \mathrm{d_E} - \mathrm{d_E}' = \frac{\mathrm{i_{L(AVG)}}\mathrm{R_{EQ}}+\mathrm{v_{DT(SW)}}+\mathrm{v_{IV(SW)}}}{\mathrm{v_E}'+\mathrm{v_D}'}, \tag{12}$$

where $\mathrm{R_{EQ}}$ is the weighted average of $\mathrm{R_E}$ and $\mathrm{R_D}$ based on their respective duty cycles, and is approximately the sum of $\mathrm{R_L}$, MOSFET resistance in a conduction path $\mathrm{R_M}$, and a fraction of $\mathrm{R_C}$ that conducts $(1 - \mathrm{d_O})$ inductor current for $\mathrm{d_O}$ period:

$$\mathrm{R_{EQ}} = \mathrm{d_E}\mathrm{R_E} + (1 - \mathrm{d_E})\mathrm{R_D} \approx \mathrm{R_L} + \mathrm{R_M} + \mathrm{d_O}(1 - \mathrm{d_O})\mathrm{R_C}. \tag{13}$$

The effect of dead time across $\mathrm{t_{SW}}$ would be $\mathrm{v_{DT(SW)}}$ shown in (11), and IV overlap's combined effect simplifies to:

$$\mathrm{v_{IV(SW)}} = \left(\frac{\mathrm{t_{V\Delta,EI}}}{\mathrm{t_{SW}}}\right)\left(\frac{\mathrm{v_I}+\mathrm{v_{DG}}}{2}\right) + \left(\frac{\mathrm{t_{V\Delta,EG}}}{\mathrm{t_{SW}}}\right)\left(\frac{\mathrm{v_O}+\mathrm{v_{DO}}}{2}\right), \tag{14}$$

where $\mathrm{t_{V\Delta,EI/EG}}$ is $\mathrm{t_{V,EI/EG(E)}} - \mathrm{t_{V,EI/EG(D)}}$. As combined effect of all three components, $\Delta\mathrm{d_E}$ represents the amount by which $\mathrm{d_E}$ must increase in a lossy power stage compared to an ideal power stage energized and drained by the same $\mathrm{v_I}$ and $\mathrm{v_O}$.

Inspecting (12), we find that only the $\mathrm{R_{EQ}}$ factor increases linear with $\mathrm{i_{L(AVG)}}$, inferring that resistance is the dominant $\Delta\mathrm{d_E}$ contributor in high-current systems. However, the insignificant, natural-logarithmically increasing (respect to $\mathrm{i_{L(AVG)}}$) $\mathrm{v_{DT(SW)}}$, becomes more pronounce in high-$\mathrm{f_{SW}}$ system, as $\mathrm{t_{DT}}$ takes up a larger fraction of $\mathrm{t_{SW}}$. Although $\mathrm{t_{V\Delta}}$'s are much shorter than $\mathrm{t_{DT}}$, $\mathrm{v_{IV(SW)}}$ can overwhelm $\Delta\mathrm{d_E}$ in high-voltage systems, as it contains $\mathrm{v_I}$ and $\mathrm{v_O}$ while the others are divided by $\mathrm{v_E}' + \mathrm{v_D}'$.

C. Loading Effect

Previous subsections only considered the losses that alter $\mathrm{v_L}$. Some losses do not change $\mathrm{v_L}$, but effectively diverge current away from the output node or the load:

$$\mathrm{i_{LD(EFF)}} = \mathrm{i_{LOSS}} + \mathrm{i_{LD}} = \mathrm{i_Q} + \mathrm{i_G} + \mathrm{i_{d_O}} + \mathrm{i_{DT}} + \mathrm{i_{IV}} + \mathrm{i_{LD}}. \tag{15}$$

$\mathrm{i_Q}$ is the quiescent current drawn from $\mathrm{v_O}$, and $\mathrm{i_G}$ denotes the gate-drive current, or the amount of charge transferred to gate capacitance $\mathrm{C_G}$ by $\mathrm{v_O}$ over each $\mathrm{t_{SW}}$:

$$\mathrm{i_G} = \frac{\mathrm{P_G}}{\mathrm{v_O}} = \frac{\mathrm{C_G}\mathrm{v_O}}{\mathrm{t_{SW}}}. \tag{16}$$

For boost and buck–boost, whose $\mathrm{i_O}$ is a $1 - \mathrm{d_E}$ fraction of $\mathrm{i_{L(AVG)}}$, a higher $\mathrm{d_E}$ would result in a decrease in available $\mathrm{i_{LD}}$:

$$i_{d_O} = i_{L(AVG)}(d_O' - d_O) = \Delta d_E i_{L(AVG)}\big|_{BS,BB}. \quad (17)$$

Additionally, in each t_{DT}, some forward recovery charge q_{FR}, which is proportional to forward transit time τ_F, is trapped in D_O that could have been supplied to the load:

$$i_{DT} = \frac{2q_{FR}}{t_{SW}}\bigg|_{BS,BB} \approx \frac{2\tau_F i_{L(AVG)}}{t_{SW}}\bigg|_{BS,BB}. \quad (18)$$

Referring to Fig. 11, it can also be seen that M_{EG} starts steering current away from the output $t_{I(E)}$ before it closes and starts feeding the output $t_{V(D)} + t_{I(D)}$ later than it is supposed to. Across t_I's, i_{DS} rises or falls roughly quadratically. The output current taken away during IV overlap is then:

$$i_{IV} = \frac{q_{EG(IV)}}{t_{SW}} \approx \left(t_{V,EG(D)} + \frac{t_{I,EG(D)}}{3} + \frac{t_{I,EG(E)}}{3}\right)\left(\frac{i_{L(AVG)}}{t_{SW}}\right). \quad (19)$$

Fig. 11 shows the trend of individual contribution and the total loading current i_{LOSS} across $i_{L(AVG)}$. Both i_{DT} and i_{IV} increase linearly with $i_{L(AVG)}$, while i_{d_O} has both linear and quadratic components since Δd_E also increases with $i_{L(AVG)}$.

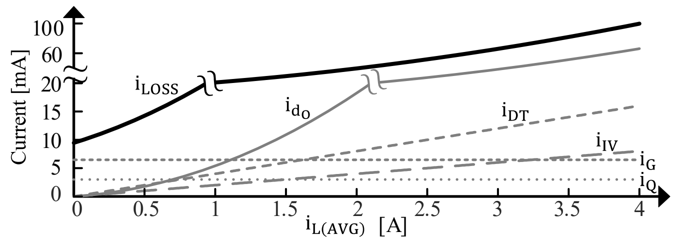

Fig. 11. Calculated loading effects.

V. MAXIMUM DC–DC CONVERSION

As discussed, d_E' is a relationship between v_E' and v_D', and can be derived from d_E and Δd_E. In other words, a lossy SLPS operating at d_E can be reflected into an ideal SLPS operating at d_E' with the same v_E' and v_D', or v_I and v_O as Table I shows. When the actual system operates at its delay-limited d_{MIN}, the imaginary ideal system has:

$$d_{MIN}' = d_{E/D(MIN)} - \Delta d_{E/D} = d_{MIN} \mp \Delta d_E. \quad (20)$$

From (4), $K_{V(\downarrow/\uparrow)}^{MAX}$ can be found and it is also the maximum conversion ratio of the actual, lossy system between identical v_I and v_O as the equivalent ideal system. It is worth noting that higher delay-limited d_{MIN} always lowers $K_{V(\downarrow/\uparrow)}^{MAX}$. Fig.12 shows the trend of decreasing $K_{V(\downarrow/\uparrow)}^{MAX}$ with higher $t_{P(MAX)}$ and d_{MIN}.

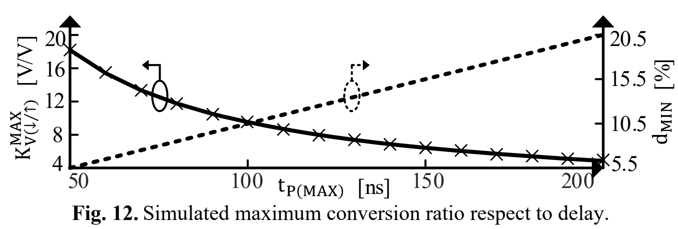

Fig. 12. Simulated maximum conversion ratio respect to delay.

Loss-induced Δd_E, however, extends $K_{V(\downarrow)}^{MAX}$ and reduces $K_{V(\uparrow)}^{MAX}$ as (20) and (4) show. It aligns with the intuition that losses reduce voltage along the direction of current flow, favoring voltage step-down applications and countering step-up applications. Fig. 13 shows $K_{V(\downarrow/\uparrow)}^{MAX}$ of a buck and a boost converter and their losses contributing to Δd_E across $i_{L(AVG)}$.

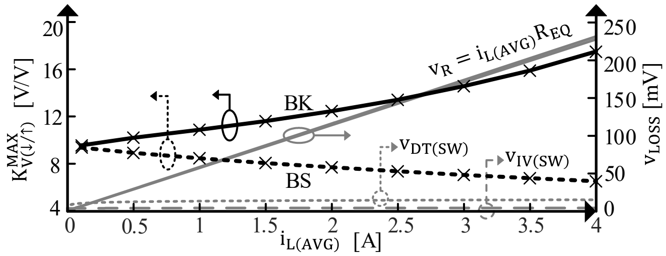

Fig. 13. Simulated buck and boost maximum conversion ratio.

A. Buck Example

The buck converter example in Fig.14 is supplied by a USB and operates at a f_{SW} of 1 MHz with a 10 ns t_{DT}. Its duty cycler has t_P^+ of 100 ns and t_P^- of 110 ns, while the drivers have a $t_{P\Delta}$ of 5 ns. At conversion limit, $d_{E(MIN)}$ is 10.5 %, and R_{EQ} exhibited is 56.7 mΩ. Simulated with SPICE, $K_{V(BK)}^{MAX}$ rises from 9.6 to 17.5 V/V across 0.1 – 4 A of $i_{L(AVG)}$ as Fig.13 shows. When the power stage is replaced with lossless components and duty cycler's t_P varies, Fig.12 shows simulated $K_{V(BK)}^{MAX}$.

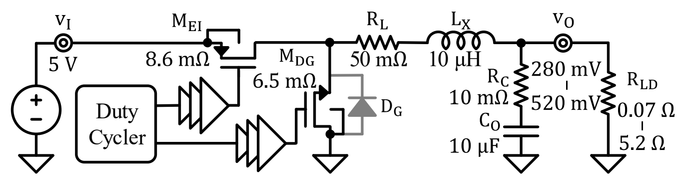

Fig. 14. Implementation of a buck example.

B. Boost Example

The boost example in Fig.15 supplies a USB load and operates with the same f_{SW}, t_{DT}, and delays. At conversion limit, $d_{D(MIN)}$ is 10.5 % and R_{EQ} is 57.7 mΩ. $K_{V(BS)}^{MAX}$ falls from 9.4 to 6.5 V/V across $i_{L(AVG)}$ as Fig.13 shows. Fig.12 shows $K_{V(BS)}^{MAX}$ when the power stage is lossless and duty cycler's t_P varies.

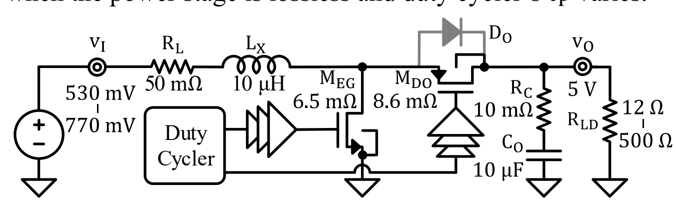

Fig. 15. Implementation of a boost example.

VI. CONCLUSIONS

This paper comprehensively analyzes the factors affecting the maximum DC–DC conversion in SLPS. By lumping the impact of losses into a shift from delay-limited minimum duty cycle, an actual system can be reflected into an ideal equivalence, where the maximum conversion can be easily determined. The minimum duty cycle is largely set by the longest single-component delay, higher of which lowers achievable conversion ratio. Resistance, dead time, and IV overlap cause the duty cycle shift, which extends the maximum conversion in voltage step-down applications but reduces it in step-up. With the derivations and insights presented, designers can now assess the feasibility of using SLPS in high conversion applications.

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