Salvaging Gate-Drive Power in Switched Power Supplies

Guillaume Guérin, *Graduate Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Fellow, IEEE*
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, U.S.A.
gguerin3@gatech.edu and rincon-mora@gatech.edu

***Abstract*— Due to the increasing use of electronic devices in our everyday lives, ranging from automotive to home automation and portable devices, the demand for effective power management systems has become more pressing. Switched-mode power supplies are highly popular because they offer high power efficiency over a wide load range. However, these power supplies lose gate charge energy due to parasitic gate capacitances. Therefore, recovering this energy could lead to higher power efficiency. This paper explores two methods of salvaging part of the gate energy by using an additional on-chip bond wire inductor and discusses their impact. The simulated results demonstrate that salvaging up to 50% of the energy stored in gate capacitances is possible, which translates to a loss saving of up to 50% of the total loss occurring in a power supply.**

Keywords*— *Switched-mode power supplies, DC–DC, bond wire inductor, gate charge loss, loss recycling

I. Gate-Drive Losses in Switched Power Supplies

From automotive applications to personal consumer electronics, IoT devices, home automation, etc. Electronic devices are increasingly important in our daily lives. Low-loss systems are always desirable, and since power supplies are the first source of losses in electronic systems, designing efficient power supplies is critical [1]. This is particularly true for portable applications, where devices are powered by a battery.

Switched-mode power supplies are popular among power supplies because of their high efficiency across a wide load range. A typical electronic system can consist of a charger and a voltage regulator that supply a load, as Fig. 1 shows. The charger and/or regulator can be implemented as switched-mode power supplies. Switched-mode power supplies switch (at a switching frequency, f_{SW}) between two or more states using switches that periodically connect and disconnect parts of the system.

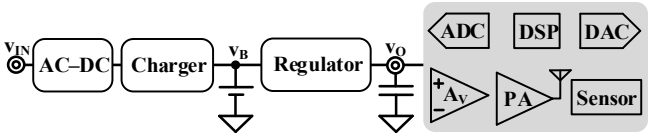

Fig. 1. Electronic system with charger, voltage regulator, and load.

Fig. 2 illustrates a CMOS switch implementation, which can be either an NMOS or a PMOS that a driver drives. The switches can carry high currents, causing MOS devices to be relatively large and result in a significant parasitic capacitance, C_G, at their gate. Whenever a switch turns on (or off), the supply must charge its gate capacitance to v_{DD} [2]. Only half of the total power that the driver burns, E_D, goes toward charging C_G. The gate charge q_G stored in C_G is then usually discharged to ground, resulting in a net loss E_D. Thus, recovering, at least partially, this gate energy, E_G, would result in an overall reduction in power loss.

$$E_D = q_G v_{DD} = 2E_G. \quad (1)$$

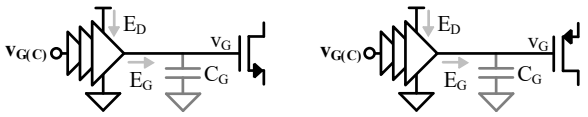

Fig. 2. CMOS switches: NMOS (left), PMOS (right).

The vast of majority of designers simply accept this loss. The State of the Art have partially implemented techniques to salvage gate energy. [3] implements an on-chip synchronous salvaging technique, but they drain C_G into a temporary tank capacitance by the mean of switches, which always burn half of E_G. This yields to a maximum salvaging rate of 25% of E_G. Similarly, [4] implements a synchronous RC transfer to the output capacitor to salvage up to 25% of E_D.

On the other hand, [5–14] implement a resonant gate driver, achieving to salvage up to 73% of E_D [5]. However, they use an external discrete inductor, and the resonant process requires precise timing, adding extra complexity on the driver control. [15] performs a resonant LC transfer by the mean of an on-chip inductor. However, they require an extra storage capacitor, and the synchronous transfer must be precisely timed.

This paper offers 2 ways of salvaging gate energy with an on-chip bond wire inductance and an asynchronous transfer, avoiding any difficult timing control. Section II presents the salvaging circuit. Section III describes the 2 techniques in detail. Section IV discuss the 2 techniques and their limitations, and Section V concludes this paper.

II. Salvaging Circuit

A. Operations

In contrast to RC transfer, LC energy transfer is lossless. Fig. 3 below shows the salvaging circuit. It relies on a bond wire inductor to salvage the energy contained in the gate C_G of a switch. The pull-up and pull-down transistor on the left are part of the driver. The gate of a switch connects to the node v_G.

The closure of the switch S_{SW} initiates the draining of C_G. D_{SW} prevents any current from flowing back to C_G. The current flows to a capacitor C_{SO} connected at the output, v_{SO}, of the salvaging circuit. Section III gives more details about the nature of C_{SO}. If C_G drains completely before L_{BW} finishes de-energizing, D_{DG} allows the current to flow.

Initially, C_G has been charged to v_{DD} by the pull-up transistor (corresponding to an NMOS switch being on or a PMOS switch being off), therefore carrying an initial amount of energy, E_I:

This work is supported by Texas Instruments.

$$E_I = \frac{1}{2} v_{DD} q_G = \frac{1}{2} C_G {v_{DD}}^2. \quad (2)$$

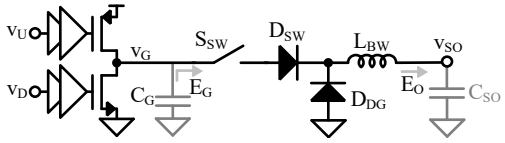

Fig. 3. Salvaging circuit.

If S_{SW} and $D_{SW/DG}$ allow the system to be asynchronous, they unfortunately contribute to degrading the efficiency of the transfer. The amount of energy E_{SO} transferred to C_{SO} is E_I minus what the switch and the diodes have burned, $E_{LOSS(TR)}$:

$$E_{SO} = E_I - E_{LOSS(TR)}. \quad (3)$$

Equation (4) defines the savings efficiency, S_E, of the transfer:

$$S_E = \frac{E_{SO}}{E_I}. \quad (4)$$

B. CMOS Implementation

Fig. 4 below depicts the CMOS implementation of the salvaging circuit. The switch is implemented with a transmission gate (PMOS and NMOS in parallel), where the 2 FETs are sized to balance their ohmic loss due to their channel resistance with their own gate drive loss. D_{DG} is implemented with a regular PN junction. D_{SW} is implemented with a MOSFET, M_{DSW}. Its gate is connected to v_G, allowing for a larger overdrive to reduce the voltage dropped across it thanks to R_G that slows down its fall.

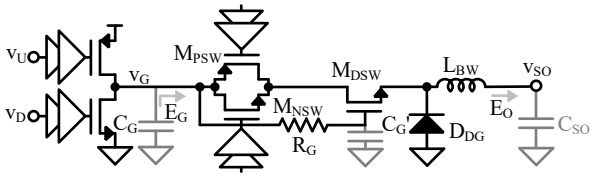

Fig. 4. Resistive gate diode.

The switch T_{SW} offers some resistance, R_{SW}, to current, and diodes (M_{DSW} or D_{DG}) drop a voltage when conducting current. The parasitic resistance of L_{BW} is negligible compared to the switch resistance. Those elements are responsible for the 2 losses degrading transfer efficiency, E_{SW} and E_D:

$$E_{LOSS(TR)} = E_{SW} + E_D = E_{SW} + v_D Q_D. \quad (5)$$

The loss occurring in a diode is simply the product of the diode voltage, v_D, and the charge, Q_D, flowing through it. The current flowing from C_G to C_{SO} through L_{BW} is a LC sinusoidal transfer. It peaks when all the initial amount of energy available in the equivalent capacitance, C_{EQ}, (the sum in series of C_G and C_{SO}), is transferred to L_{BW}. The current then reaches $i_{L(PK)}$. The initial energizing voltage applied across L_{BW} is v_{DD} minus v_{SO}:

$$E_{SW} \approx R_{SW} {i_{RMS}}^2 \left(\frac{t_{LC}}{2}\right) = R_{SW} \left(\frac{i_{L(PK)}}{\sqrt{2}}\right)^2 \left(\frac{2\pi\sqrt{L_{BW}C_{EQ}}}{2}\right)$$
$$\approx R_{SW} \left[\frac{(v_{DD} - v_{SO})}{\sqrt{2}} \sqrt{\frac{C_{EQ}}{L_{BW}}}\right]^2 \pi\sqrt{L_{BW}C_{EQ}}. \quad (6)$$

It takes about half the LC period, t_{LC}, for the energy to transfer from C_G to C_{SO}.

For the system to be integrated, an on-chip inductor needs to be used. On-chip inductors come in 2 main types: bond wires, and monolithic metal traces, and are in the nano Henries range, up to 10 nano Henries usually [16–22]. For this application, a lead frame bond wire inductor was chosen due to the low inductance required and insensitivity to inductance variation [18]. Simulations are performed with a 5 nano Henries inductor.

Fig. 5 depicts how such an inductor can be implemented using 4 bond wires to benefit from coupling. The 2 upper wires are close from each other and see a current flowing in the same direction. They therefore see a positive mutual coefficient that reinforce the inductance, noted M+ in Fig. 5. The same principle applies to the 2 lower bond wires. Separating the two sets of wires helps to reduce the negative coupling coefficient, noted M-, as discussed in literature [23–27].

Any parasitic capacitance, such as pad capacitance, will negatively impact S_E, as they will steal energy away from C_{SO}. However, if they are small enough in front of C_G, their effect can be neglected.

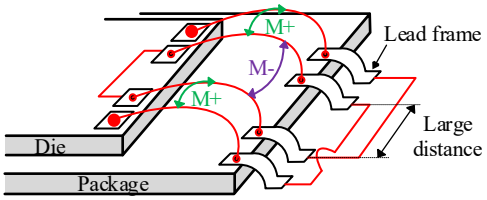

Fig. 5. Bond wire inductor design.

III. Salvaging Strategies

A. Recover Gate Energy

This section introduces the first technique for salvaging gate-drive energy: recovery. As depicted in Fig. 6, the salvaging circuit connects to the output of the power supply. C_{SO} is therefore the output capacitance, C_O, of a switched-mode power supply. Therefore, each switch in the power supply can have its own recovery circuit implemented.

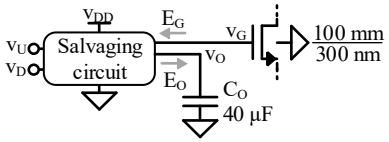

Fig. 6. Salvaging circuit connects to the output capacitor of the power supply.

In order to present an insightful analysis of the design and limitation of this system, the only loss considered in the theory is a diode loss. In this configuration, the initial voltage across C_O is the output voltage v_O of the power supply. Because C_O is significantly larger than C_G, v_O is considered constant. For C_G to drain completely, the initial energizing voltage across the inductor should be larger than half the initial voltage across C_G. This condition gives an upper limit value for v_O:

$$v_O + v_D \leq \frac{v_{DD}}{2}. \quad (7)$$

If (7) is not met, C_G will not drain fully, and when the transfer is over, voltage across C_G is $v_{G(\infty)}$. Equation (8) expresses the conservation of energy during the transfer. On the total amount of energy transferred from C_G, some has been burned in D_{SW}, and the remaining has reached v_O:

$$\frac{[{v_{DD}}^2 - {v_{G(\infty)}}^2]}{2} = v_D(v_{DD} - v_{G(\infty)}) + v_O(v_{DD} - v_{G(\infty)}). \quad (8)$$

Solving (8) for $v_{G(\infty)}$ reveals the amount of energy, E_{O1}, recovered in C_O:

$$E_{O1} = C_G v_O[2v_{DD} - 2(v_O + v_D)], \quad (9)$$

And the optimal output voltage, v_O', that yields the highest E_{O1}:

$$v_O' = \frac{v_{DD} - v_D}{2}. \quad (10)$$

A lower v_O results to in less energy recovered because energy held in a capacitor scales quadratically with the voltage across it. Equation (11) consequently expresses the savings efficiency, S_E, which simplifies to (12) in the ideal case of a zero v_D:

$$S_E = 4\left(\frac{v_O}{{v_{DD}}^2}\right)[v_{DD} - (v_O + v_D)]. \quad (11)$$

$$S_E = 4\left(\frac{v_O}{v_{DD}}\right)\left(1 - \frac{v_O}{v_{DD}}\right). \quad (12)$$

If (7) is met, C_G drains fully. When v_G reaches 0, L_{BW} remains energized and holds $E_{L(0)}^{RECO}$. $E_{L(0)}^{RECO}$ is E_G minus what has been recovered by v_O until v_G reaches 0 (E_O^L), minus what has been lost in D_{SW} (E_D). Part of $E_{L(0)}^{RECO}$ will reach v_O, and the remaining will be lost in D_{DG} ($E_{D(DG)}$). Equation (13) thus expresses the amount of energy recovered in C_O, E_{O2}:

$$\begin{aligned} E_{O2} &= E_O^L + E_{L(0)}^{RECO} - E_{D(DG)} \\ &= v_O q_G + \left(\frac{C_G}{2}{v_{DD}}^2 - v_D q_G - v_O q_G\right) - v_D C_G\left(\frac{v_{DD}}{2} - v_O - v_D\right) \\ &= \frac{v_O C_G {v_{DD}}^2}{2(v_O + v_D)}. \end{aligned} \quad (13)$$

When v_D is 0, (13) simplifies to E_I, so S_E becomes 100% in the ideal case. Otherwise, the transfer efficiency is:

$$S_E = \frac{v_O}{v_O + v_D}. \quad (14)$$

Fig. 7 below depicts transfer efficiency as a function of the ratio of v_O over v_{DD}, when v_D is zero. As long as (7) is verified, S_E is 100%. When (7) no longer holds (which corresponds to a ratio v_O over v_{DD} of 50%), the savings efficiency starts to drop.

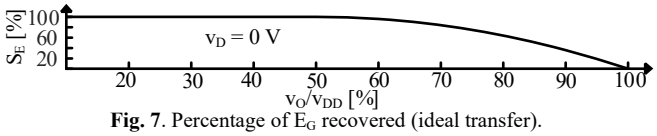

Fig. 7. Percentage of E_G recovered (ideal transfer).

For a non-ideal case, Fig. 8 shows transfer efficiency across v_O for different v_{DD}. Each transfer efficiency peaks when (7) is met for that given v_{DD}, and reaches up to 70%.

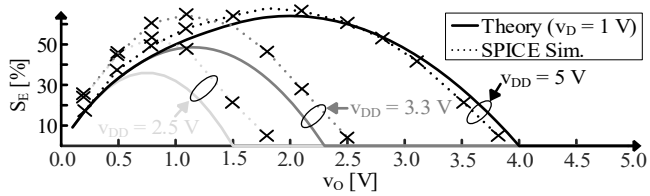

Fig. 8. Percentage of E_G recovered across v_O for a v_{DD} of 2.5 V, 3.3 V, 5 V.

The theoretical plots in Fig. 8 are plot with only 1 lossy element, a diode dropping a constant voltage. Circuit in Fig. 4 is simulated with level 1 SPICE MOSFET model. M_{PSW} and M_{NSW} are 4 mm wide, M_{DSW} is 60 mm wide, and R_G is 12 Ω. Unlike the theory, simulations include a resistive ohmic loss, E_{SW}, which is the loss which mainly degrades S_E. Thanks to R_G, M_{DSW} only drops a small voltage.

It is worth noting that when sizing down the size of the switch, S_E drops, as Fig. 9 shows. This is because the size of M_{NSW} and M_{PSW} must scale down with C_G. They will then become increasingly more resistive (as resistance is inversely proportional to width). Because of voltage breakdown for high voltage applications, power supplies are usually designed with a large technology node, that can lead to a gate capacitance of hundreds of pico-farads [28].

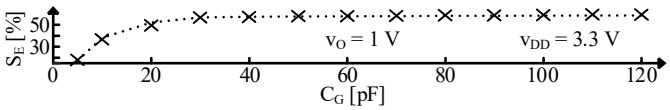

Fig. 9. Simulated savings efficiency across C_G.

B. Recycle Gate Energy

This section presents a second way to salvage E_G. In this scenario, C_{SO} is the gate capacitance of another switch in the system. Those 2 switches need to work in a complimentary fashion, one gate being discharged when the other needs to be charged. Fig. 10 shows a representation of this implementation with a PMOS and an NMOS switch. The energy from each FET's gate capacitance is recycled to the other gate capacitance.

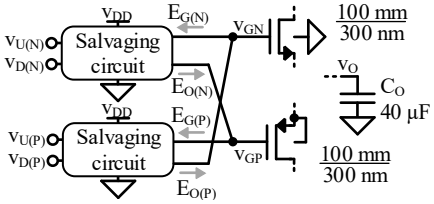

Fig. 10. Salvaging circuit connects to the gate of another switch.

Unlike recovery, there is no initial voltage across C_{SO}. Assuming a transfer from C_{GN} to C_{GP}, the transfer is governed by the conservation of charges and energy. If C_{GN} does not drain completely, then v_{GN} will be at $v_{GN(\infty)}$ when the transfer is over, and v_{GP} at $v_{GP(\infty)}$. Equation (15) sets the condition for C_{GN} to drain completely:

$$C_{GN} \le C_{GP}\left[1 - \left(\frac{2v_D}{v_{DD}}\right)\right]. \quad (15)$$

Solving (16) and (17) for $v_{GN(\infty)}$ and $v_{GP(\infty)}$ allow to find the transfer efficiency S_E, which simplifies to (19) when v_D is 0.

$$\frac{C_{GN}[{v_{DD}}^2 - {v_{GN(\infty)}}^2]}{2} = C_{GN} v_D\left(v_{DD} - v_{GN(\infty)}\right) + \frac{C_{GP}{v_{GP(\infty)}}^2}{2}. \quad (16)$$

$$C_{GN}\left(v_{DD} - v_{GN(\infty)}\right) = C_{GP} v_{GP(\infty)}. \quad (17)$$

$$S_E = 4\left[\frac{C_{GP}C_{GN}}{(C_{GP} + C_{GN})^2}\right]\left(1 - \frac{v_D}{v_{DD}}\right)^2. \quad (18)$$

$$S_E = 4\left[\frac{C_{GP}C_{GN}}{(GP + C_{GN})^2}\right]. \quad (19)$$

When the transfer is complete ((15) is met), L_{BW} is still energized with $E_{L(0)}$ when v_{GN} reaches 0. Applying a reasoning similar to (13), solving (20) for $v_{GP(\infty)}$ allows to find S_E; no simple expression for S_E exists in this case.

$$E_{L(0)} = v_D C_{GP}\left(v_{GP(\infty)} - \frac{C_{GN}v_{DD}}{C_{GP}}\right) + \frac{C_{GP}\left[{v_{GP(\infty)}}^2 - \left(\frac{C_{GN}v_{DD}}{C_{GP}}\right)^2\right]}{2}. \quad (20)$$

Fig. 11 illustrates S_E across v_{DD} for the recycling technique. The theoretical plots were generated with only 1 lossy element, a diode that drops a constant voltage v_D. Simulated S_E

ultimately flattens because both E_I and E_{SW} scale quadratically with v_{DD}. M_{PSW} and M_{NSW} are 4 mm wide, M_{DSW} is 10 mm wide, and R_G is 47 Ω.

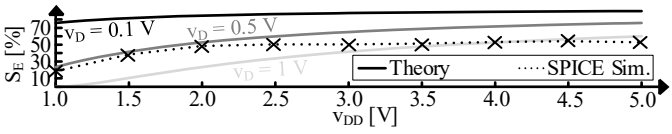

Fig. 11. Percentage of E_G recycled across v_{DD}.

IV. Context

A. Salvaging Strategies

The main difference between recovery and recycling lies in the nature of C_{SO}. For recovery, C_{SO} is the output capacitor of the power supply. It can also be a battery for instance. The distinctions with recycling are that C_O is significantly larger than C_G, and it can carry an initial voltage across it when the transfer starts. On the other hand, C_{SO} in the recycling technique is another gate capacitance, so it is roughly the same size as C_G, and it is initially discharged.

A characteristic of RC energy transfer is that the switch will always burn as much energy as the capacitance receives. This is a fundamental limitation of the recovery technique. In this case, the gate capacitance is charged to v_{DD} thanks to a regular driver, so a full E_G has already been burned in the driver and cannot be salvaged at all. Recovering 70% of E_G leads to a net saving of 35% of the total loss E_D.

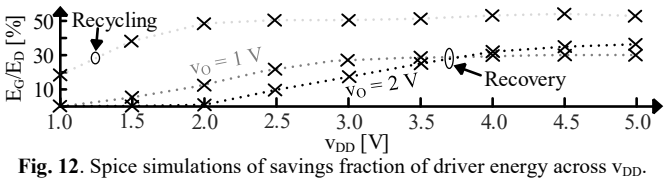

Fig. 12. Spice simulations of savings fraction of driver energy across v_{DD}.

On the other hand, with the recycling technique, E_G is directly recycled to another gate via a lossless LC transfer, with no additional driver loss. Savings with recycling are twice as much compared to recovery, as Fig. 12 shows. A 50% recycling rate yields a net saving of 50% on E_D. However, recycling needs to be implemented on 2 complementary switches. It can be 2 NMOS, but their respective gates need to be controlled with a 180° phase shift.

B. Output Power

When implemented, those gate energy techniques can allow for some energy savings on the total energy, E_{LOSS}, lost in the power supply. Equation (21) defines the fractional weight of the savings compared to the total amount of loss in the power stage.

$$\sigma_S = \frac{P_{SO}}{P_{LOSS}} = \frac{E_{SO} f_{SW}}{E_{LOSS} f_{SW}}. \quad (21)$$

For example, in a switched-inductor converter, losses may be modeled according to (22) [2, 29–32] with a constant term P_0 (accounting for losses that do not scale with average output current, $i_{O(AVG)}$, such as P_D and quiescent power loss, P_Q), a term proportional to $i_{O(AVG)}$ (overlap and dead time losses), P_1, and a term proportional to the square of $i_{O(AVG)}$ (ohmic loss), P_2. P_D is simply E_D multiplied by the switching frequency, f_{SW}.

$$P_{LOSS} = P_0 + v_{PS} i_{O(AVG)} + R_{PS} i_{O(AVG)}^2. \quad (22)$$

v_{PS} (modeling the average voltage drop in overlap and dead time loss) can be approximated to 3.5 mV for a converter operating at 200 kHz [33], and at 14 mV for a fully integrated converter [19]. P_Q is about 30 µW [34], while P_D is 0.5 mW for a converter operating at 200 kHz [33], and at 33 mW for a fully integrated converter [28]. Average resistance in the power path, R_{PS}, is 100 mΩ for a discrete converter [35], and about 500 mΩ for a fully integrated one [36].

Fig. 13 illustrates an example of how σ_S scales with output power, P_O, for 2 different switched-inductor power supplies: a fully integrated system with on-chip inductor operating at 10 MHz, and a system with a discrete off-chip inductor operating at 200 kHz. Fig. 13 also displays how P_0, P_1, and P_2 scale with P_O for a fully integrated converter. Gate-drive loss is independent of output power. As P_O increases, ohmic loss starts to overwhelm all other losses, so the savings made on P_G starts to become less significant. Nonetheless, because of the high switching frequency, f_{SW}, which the fully integrated converter is operating at, at low power levels, recycling results to a total loss saving of nearly 50%. This is because at low P_O, P_0 (namely gate-charge loss) accounts for a very large portion of the total loss at a high f_{SW}. However, this total energy savings is only 25% at low power for a converter with an off-chip inductor operating at a lower f_{SW}.

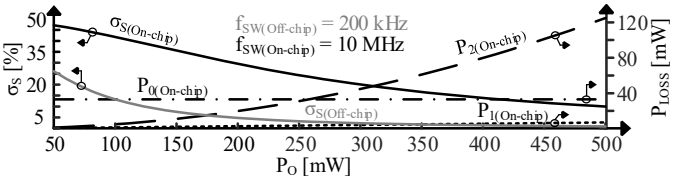

Fig. 13. Fractional weight of savings across P_O.

When E_D represents a significant fraction of the total loss (ohmic loss, gate-drive loss, etc.) occurring in the power supply, salvaging allows a noticeable improvement in the power efficiency of the system [3]. This is especially true for instance for fully integrated switched-inductor with on-chip inductor that operate at a very high f_{SW} [28]. However, salvaging gate-drive energy on an already optimized for low loss power stage may not yield significant improvements.

V. Conclusions

This paper has presented 2 implementations of a circuit to salvage gate-drive energy. Gate energy can be recovered to the large output capacitance of the power supply, with simulation results indicating that recovering up to 70% of the gate energy is feasible. Recycling the gate energy to another gate makes it possible to save up to 50% of driver energy, which can result in a total loss saving of nearly 50% for a high frequency fully integrated converter with an on-chip inductor. This loss saving is up to 25% for a converter operating at a lower frequency with an off-chip inductor. Additionally, this salvaging circuit is a fully integrated solution that uses a bond wire inductor and does not rely on complex and precise timing for operation.

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