Optimal High-Efficiency DCM Design of Switched-Inductor CMOS Power Supplies

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***Abstract*—Improving efficiency for switched-inductor (SL) power-supplies is vital for energy-limited battery-supplied microsystems such as wireless microsensors and portable devices. These micro-systems idle mostly so efficiency in Discontinuous Conduction Mode (DCM) is crucial. Moreover, limited volumes of these tiny micro-systems often lead to using tiny lossy inductors, which further reduce efficiency. Therefore, this paper theorizes how to select the optimal inductor, design the optimal power stage, and optimize the current profile to achieve the highest efficiency in DCM, using insightful derivations. This proposed co-design of inductor and current profile is absent in the state-of-the-art. The theory is accurate, and the percentage error is 0.3–4.9%. Using the proposed theory, with a 1.6 × 0.8 × 0.8 mm³ inductor, efficiency improvement can reach 6.4% compared with the State of the Art.**

Keywords—Switched inductor, power supply, high efficiency, discontinuous conduction mode, peak current, optimization.

I. Battery-Supplied Microsystems

Wireless microsensors and portable devices (i.e., cell phones and tablets) become increasingly multi-functional and power-demanding [1–2]. As Fig. 1 shows, sensing, data processing, and wireless transmission are all integrated into one device, which consequently making portable devices power-hungry. Moreover, aggressive demand for small form factor limits the total energy stored in the batteries that supply these devices. Therefore, minimizing power loss and extending battery life is the primary concern for battery-supplied microsystems [3–4].

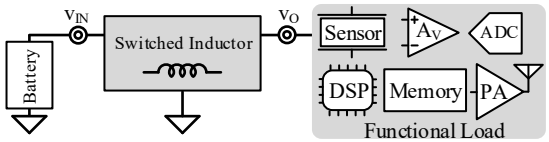

Fig. 1. A battery-supplied microsystem.

Wireless microsensors and portable devices idle mostly. So, the switched-inductor (SL) power supply in Fig. 1 mostly operates in Discontinuous Conduction Mode (DCM). Thus, maximizing DCM efficiency η_C is crucial. A comprehensive DCM high-η_C design strategy, however, is missing in [5–9]. So, this paper theorizes how to co-optimize the inductor, the power stage, and the current profile to achieve the highest η_C in DCM. Section II explains this theory using insightful derivations and shows a SL buck-boost example. Section III validates this theory with simulations. Section IV assesses η_C improvement compared with the prior art. Section V concludes this paper.

II. High-Efficiency DCM Design

Fig. 2 shows the non-inverting SL buck-boost design example. During energizing time t_E, input switch M_{EI} and ground switch M_{EG} closes to energize the transfer inductor L_X from v_{IN}, so L_X's current i_L rises linearly. During drain time t_D, ground switch M_{DG} and output switch M_{DO} closes to drain i_L into v_O, and i_L drops linearly. As Fig. 3 shows, in DCM, L_X conducts during t_E and t_D, and reaches zero at the end of conduction time t_C.

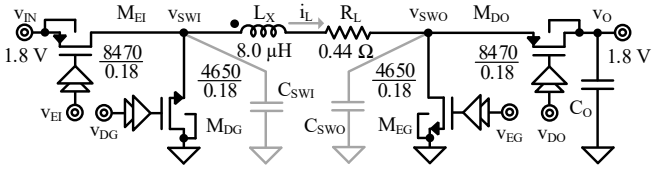

Fig. 2. A non-inverting switched-inductor buck-boost power-supply.

Since a buck is just a buck-boost without M_{EG} and M_{DO}, and a boost is a buck-boost without M_{EI} and M_{DG}, the buck-boost is representative of all cases.

A. Optimal Switching Scheme

Efficiency η_C often peaks at a specific output power P_O [5–6]. In DCM, however, SL buck-boost delivers discrete energy packets to feed v_O. So, if energy packets (i.e., L_X's energy E_L) are identical and the buck-boost only adapts the frequency f_{SW} of energy delivery across P_O, η_C can stay flat across P_O. This is because input power P_{IN}, L_X's Equivalent Series Resistance (ESR) loss P_{RL}, MOS power switches loss P_{MOS}, and switch-node parasitic capacitance loss P_{CSW} all scale with f_{SW} and P_O:

$$\eta_C = \frac{P_O}{P_{IN}} \approx \frac{P_{IN} - P_{RL} - P_{MOS} - P_{CSW}}{P_{IN}} \propto \frac{f_{SW}}{f_{SW}} \neq f(P_O) \cdot \qquad (1)$$

Therefore, designers should maximize the η_C of each energy packet so η_C can stay maximally high across P_O [10].

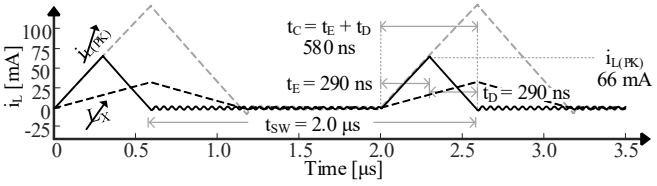

Fig. 3. Inductor current profile with different $i_{L(PK)}$ and L_X.

B. Optimal Switches

Power switches create ohmic loss P_{MR} when conducting current, and charge loss P_{MC} when gate drivers switch them on and off. For MOS switches, P_{MR} scales with channel resistance R_{MOS}, which is inversely proportional to channel width W_{MOS}, as (2) shows. k_{MR} is the W_{MOS}-independent coefficient.

$$P_{MR} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 R_{MOS} \frac{t_{E/D}}{t_{SW}} \equiv \frac{k_{MR}}{W_{MOS}} \cdot \qquad (2)$$

P_{MC} scales with the parasitic gate capacitance C_G of MOS power switches, which is proportional to W_{MOS} as (3) shows:

$$P_{MC} = (C_G "L_{MIN} W_{MOS}) v_{GD}^2 f_{SW} \equiv k_{MC} W_{MOS} \,, \qquad (3)$$

where C_G" is C_G per unit area, L_{MIN} is the minimum channel length, v_{GD} is the gate-drive voltage, and k_{MC} is the coefficient.

P_{MOS} is minimum if W_{MOS} balances P_{MR} and P_{MC} so they are equal, as Fig. 4 shows [10]. Optimal W_{MOS} (denoted as W_{MOS}') is:

$$W_{MOS}' = \sqrt{\frac{k_{MR}}{k_{MC}}} \ . \quad (4)$$

With optimal W_{MOS}', the minimum P_{MOS} (denoted as P_{MOS}') is:

$$P_{MOS}' = P_{MR}' + P_{MC}' = 2P_{MR}' = 2\sqrt{k_{MR}k_{MC}} \ , \quad (5)$$

where P_{MR}' & P_{MC}' are the P_{MR} & P_{MC} when the width is W_{MOS}'. Fig. 4 exemplifies M_{EG}'s P_{MR}, P_{MC}, and total loss P_{MOS} across its width W_{MG} with 180-nm devices. M_{EI}, M_{DG}, M_{DO}'s calculated optimal widths W_{EI}', W_{DG}', W_{DO}' are detailed in Table I.

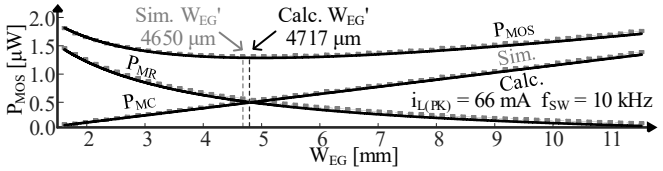

Fig. 4. Ohmic loss P_{MR}, charge loss P_{MC}, and total MOS loss P_{MOS} across W_{EG}.

C. Optimal Inductor

The desire for small form factor limits the volume of wireless microsensors and portable devices [11–12]. So, inductor volume is limited. As Fig. 5 shows, ESR R_L is roughly proportional to L_X for inductors constrained by the same volume. R_L thus is:

$$R_L \equiv k_{LX} L_X \ , \quad (6)$$

where k_{LX} is the proportionality coefficient.

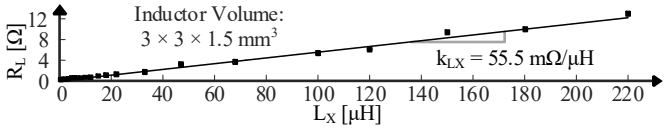

Fig. 5. Inductor ESR R_L vs. inductance L_X.

This subsection explains how to find the optimal L_X (denoted as L_X') for any given energy packet size (i.e., inductor energy E_L). Since E_L is quadratic to peak inductor current $i_{L(PK)}$. So, for the same E_L, $i_{L(PK)}$ reduces if L_X increases, as (7) shows:

$$i_{L(PK)} \propto \frac{1}{\sqrt{L_X}} \ . \quad (7)$$

Similarly, a higher L_X reduces the rate at which i_L rises. So, to have the same E_L, conduction time t_C (as labeled in Fig. 3) is proportional to the square-root of L_X, as (8) shows:

$$t_C \propto \sqrt{L_X} \ . \quad (8)$$

Thus, L_X's ESR loss P_{RL} is derived as:

$$P_{RL} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 R_L \frac{t_C}{t_{SW}} \equiv k_{RL}\sqrt{L_X} \ , \quad (9)$$

where t_{SW} is the switching period, and k_{RL} is the L_X-independent coefficient. P_{RL} is proportional to $L_X^{0.5}$ as Fig. 6 shows.

For optimally sized MOS power switches, they energize and drain L_X across t_E or t_D, which are both proportional to t_C. Therefore, optimal MOS loss P_{MOS}' is expressed as:

$$P_{MOS}' = 2\sqrt{k_{MR}k_{MC}} \propto \sqrt{i_{L(PK)}^2 t_{E/D}} \equiv \frac{k_{MOS}'}{\sqrt[4]{L_X}} \ , \quad (10)$$

where k_{MOS}' is the L_X-independent coefficient, and P_{MOS}' is proportional to $L_X^{-0.25}$ as Fig. 6 shows. With (9) and (10), there exists a L_X' that minimizes (P_{RL} + P_{MOS}'). L_X' is derived as:

$$L_X' = \left(\frac{k_{MOS}'}{2k_{RL}}\right)^{\frac{4}{3}} \ . \quad (11)$$

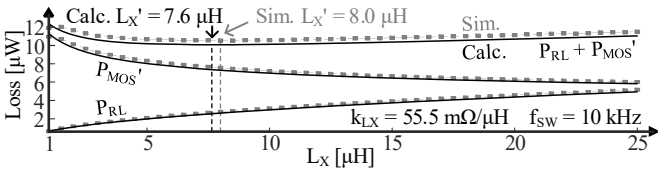

Fig. 6. ESR loss P_{RL}, optimal switches loss P_{MOS}', and their sum across L_X.

As Fig. 6 shows, the calculated L_X is 7.6 µH in this example.

D. Optimal Peak Inductor Current

There are two types of loss in a SL buck-boost: ohmic loss P_R and charge loss P_C. P_R consists of ESR loss P_{RL} and MOS ohmic loss P_{MR}. P_C consists of MOS charge loss P_{MC} and switch-node parasitic capacitance loss P_{CSW}. With the optimal L_X and W_{MOS}, this subsection explains how to find the optimal energy packet, or in other words, the optimal $i_{L(PK)}$ (denoted as $i_{L(PK)}'$) to achieve the highest η_C.

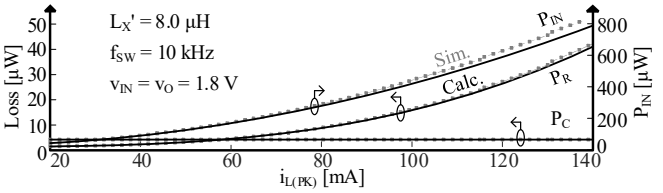

Fig. 7. Ohmic loss P_R, charge loss P_C, and input power P_{IN} across $i_{L(PK)}$.

To maximize η_C, $i_{L(PK)}'$ minimizes fractional (percentage) loss. Fractional ohmic loss σ_R is the fraction of P_{IN} lost in P_R. σ_R is:

$$\sigma_R = \frac{P_R}{P_{IN}} = \frac{P_{RL}' + P_{MR}'}{P_{IN}} = \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 \frac{R_L'(t_C/t_{SW}) + R_{MOS}'(t_{E/D}/t_{SW})}{v_{IN}(0.5i_{L(PK)})(t_E/t_{SW})} \equiv k_R i_{L(PK)} \ , \quad (12)$$

where R_{MOS}' is the channel resistance of optimal MOS power switches, and k_R is the $i_{L(PK)}$-independent coefficient. Fig. 7 shows P_R scales with $i_{L(PK)}^3$ while P_{IN} scales with $i_{L(PK)}^2$, therefore, σ_R is proportional to $i_{L(PK)}$ as Fig. 8 shows.

Fractional charge loss σ_C is the fraction of P_{IN} lost in P_C. σ_C is:

$$\sigma_C = \frac{P_C}{P_{IN}} = \frac{P_{MC}' + P_{CSW}}{P_{IN}} = \frac{\left(C_{MOS}' v_{GD}^2 + 0.5 C_{SWI/O} v_{SWI/O}^2\right) f_{SW}}{v_{IN}(0.5i_{L(PK)})(t_E/t_{SW})} \equiv \frac{k_C}{i_{L(PK)}^2} \ , \quad (13)$$

where C_{MOS}' is the parasitic capacitance of optimal MOS power switches, $C_{SWI/O}$ is the parasitic capacitances at switch-nodes $v_{SWI/O}$, and k_C is the $i_{L(PK)}$-independent coefficient. Fig. 7 shows that P_C is independent of $i_{L(PK)}$. Therefore, σ_C is proportional to $i_{L(PK)}^{-2}$ as Fig. 8 shows.

With (12) and (13), there exists a $i_{L(PK)}'$ that minimizes the total fractional loss σ_{TOT}. That is, $i_{L(PK)}'$ maximizes η_C. $i_{L(PK)}'$ is:

$$i_{L(PK)}' = \left(\frac{2k_C}{k_R}\right)^{\frac{1}{3}} , \quad (14)$$

In this example, the calculated $i_{L(PK)}'$ is 68 mA as Fig. 8 shows.

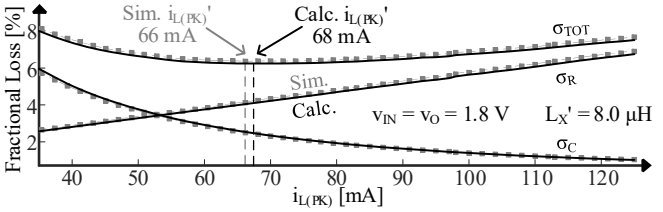

Fig. 8. Fractional ohmic loss σ_R, charge loss σ_C, total loss σ_{TOT} across $i_{L(PK)}$.

III. Validation

A. Optimal Switches

The total P_{MOS} lost in the energizing switches M_{EI} and M_{EG} is shown in Fig. 9. Simulated using a 180-nm process, an 8470-µm W_{EI} and a 4650-µm W_{EG} give the lowest total P_{MOS}, which is 4.1 µW. Compared with calculated values listed in Table I, this theory has 1.3% and 1.4% error in W_{EI} and W_{EG} calculation.

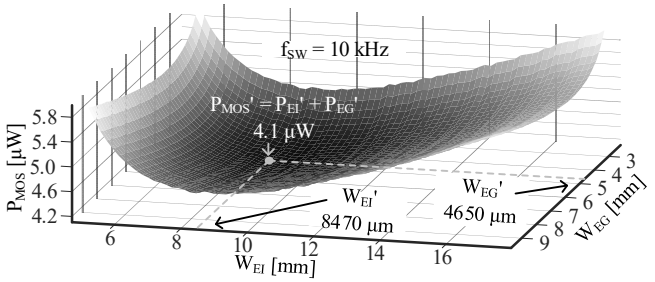

Fig. 9. Simulated MOS energizing switch losses across W_{EI} and W_{EG}.

Fig. 10 shows the simulated total P_{MOS} caused by the draining switches M_{DO} and M_{DG}. Similarly, an 8470-µm W_{DO} and a 4650-µm W_{DG} give the lowest total P_{MOS}, which is 4.1 µW, and the error is 1.3–1.4%. Because v_{IN} equals v_O in this design example, so both the converter topology and the v_{IN} & v_O settings are symmetric. Thus, both calculation and simulation result in the same optimal widths for NMOS ground switches M_{EG} and M_{DG}, and PMOS input/output switches M_{EI} and M_{DO}.

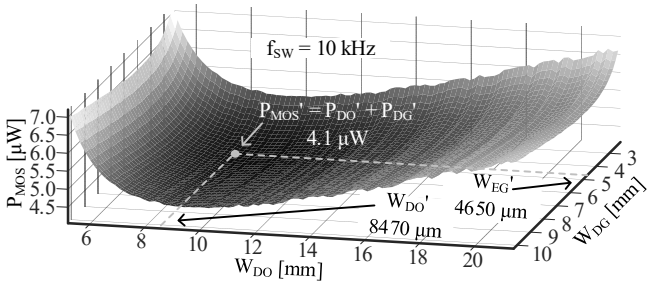

Fig. 10. Simulated MOS draining switch losses across W_{DG} and W_{DO}.

Calculated optimal widths are larger than simulated because this theory neglects gate driver shoot-through loss P_{ST} [13], which effectively underestimates k_{MC}. P_{ST} is the loss when both NMOS and PMOS in a driver are conducting. Nonetheless, with lowest-delay drivers as described in [13], drivers shoot through for less than 450 ps in simulation and the resulting error is less than 1.4%.

B. Optimal Inductor & Peak Current

Fig. 11 and 12 shows simulated η_C and σ_{TOT} across L_X and $i_{L(PK)}$, with optimal power switches. The simulation targets a 3.0 × 3.0 × 1.5 mm^3 off-the-self inductor series, which presents about 55.5 mΩ ESR per micro-Henry. Simulated L_X' and $i_{L(PK)}$' is 8.0 µH and 66 mA, respectively. Compared with the calculated results listed in Table I, the theory has 4.9% and 3.0% error in L_X' and $i_{L(PK)}$' calculation, respectively. Simulated $i_{L(PK)}$' is lower than calculated. Because simulated optimal switches are smaller and more resistive than calculated, so in simulations, a lower-than-predicted $i_{L(PK)}$' balances P_R and improves η_C as (14) indicates.

This theory underestimates σ_{TOT} because shoot-through, dead-time, & i_{DS}-v_{DS} overlap losses are not included [14]. However, portable devices and microsensors consume about or less than tens of milli-Watts. For such P_O and $i_{L(PK)}$, these losses are not significant. C_O's ESR loss is neglected since the ESR of surface-mount device can be as low as 25 mΩ [15], which is much lower than R_L. Thus, this theory only underestimates σ_{TOT} by 4.8%.

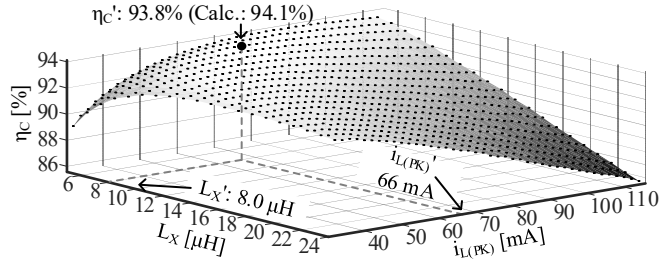

Fig. 11. Simulated η_C across L_X and $i_{L(PK)}$.

Table I details the calculated and simulated optimal design parameters, optimal fractional loss σ_{TOT}', optimal η_C (denoted as η_C'), and the corresponding percentage error. In sum, the error is 0.3–4.9% for design parameters, 4.8% for σ_{TOT}' and 0.3% for η_C', which proves the accuracy and effectiveness of this theory.

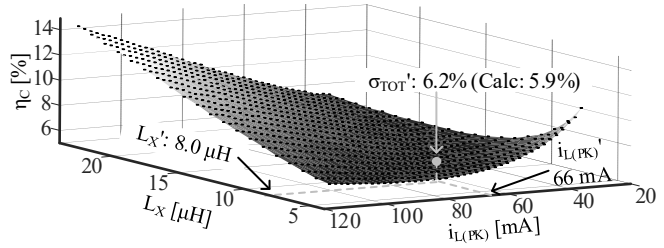

Fig. 12. Simulated total fractional loss σ_{TOT} across L_X and $i_{L(PK)}$.

Table I: Optimization Error

Parameter	Calc.	Sim.	Error	Parameter	Calc.	Sim.	Error
L_X'	7.6 µH	8.0 µH	4.9%	$i_{L(PK)}$'	68 mA	66 mA	3.0%
W_{EI}'	8583 µm	8470 µm	1.3%	W_{EG}'	4717 µm	4650 µm	1.4%
W_{DG}'	4717 µm	4650 µm	1.4%	W_{DO}'	8583 µm	8470 µm	1.3%
σ_{TOT}'	5.9%	6.2%	4.8%	η_C'	94.1%	93.8%	0.3%

Simulation Settings: $v_{IN} = v_O = 1.8$ V, $P_O = 10$ µW–10 mW.

IV. Performance

A. Loss Breakdown

Fig. 13 shows simulated loss breakdown of the design example. With the switching scheme described in Section II.A, fractional ESR loss σ_{RL}, MOS loss σ_{MOS}, and C_{SW} loss σ_{CSW} are steady across P_O. This explains why η_C stays optimally high across P_O.

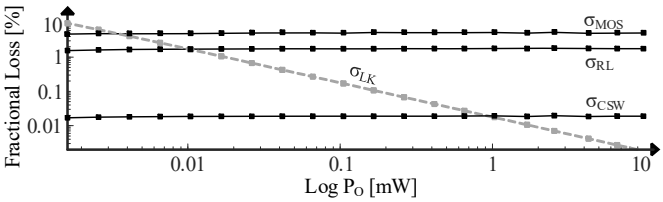

Fig. 13. Simulated loss breakdown across output power P_O.

Simulated power switches' and gate drivers' leakage is the sub-threshold current when they are idling. Leakage loss P_{LK} does not scale with P_O, so fractional leakage loss σ_{LK} keeps rising as P_O reduces, and η_C cannot be optimally high once σ_{LK} dominates. This is why η_C drops when P_O reduces, as Fig. 14 shows.

B. Efficiency η_C

Fig.14 shows simulated optimal η_C across P_O using inductors with different volumes. Usually, a larger volume reduces inductor ESR and improves inductor quality factor [16]. This implies P_{RL} will decrease if an inductor with a larger volume is chosen. Therefore, the maximum η_C rises if an inductor with larger volume is used.

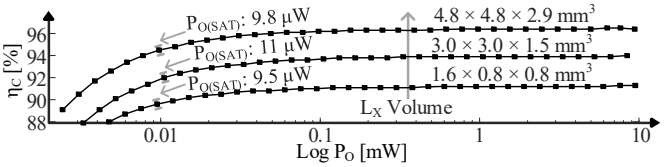

Fig. 14. Simulated efficiency η_C across P_O with different inductor volumes.

Labelled in Fig. 14, $P_{O(SAT)}$ is the P_O at which η_C saturates to the maximum efficiency $\eta_{C(MAX)}$. This paper defines $P_{O(SAT)}$ if η_C reaches 98% of $\eta_{C(MAX)}$. Despite P_{LK} reduces η_C when P_O is low, η_C drops less than 2% across 1000–1300× P_O variation. This switching scheme results in a 104–135× increase in P_O range compared to [8]. Feedback control is designed so the SL always delivers the optimal energy packet and only varies f_{SW}, and a controller like that in [9] can serve this purpose. Also, conversion ratio affects t_E, t_D, and t_C in DCM, and process technology affects L_{MIN}, which this theory have taken into account in (2)–(5) and (12)–(14). Thus, this theory applies to various v_{IN}-v_O combinations and process technologies.

C. State of the Art

A SL charger-supply is presented in [9] without optimizing L_X. Because [9] reports measured data while this paper reports simulated data. For fairness, instead of directly comparing with the measured η_C in [9], this paper re-simulates η_C using the same v_{IN}, v_O, L_X, R_L, and $i_{L(PK)}$ as in [9]. Then, this paper simulates the η_C with the optimal L_X and $i_{L(PK)}$ (while keeping the same v_{IN}, v_O, and k_{LX}), and illustrates η_C improvement.

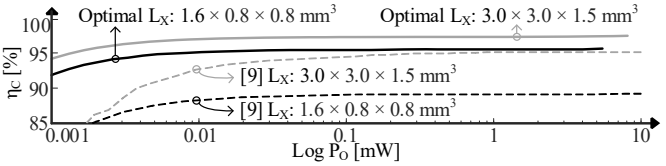

Fig. 15. Simulated η_C improvement by optimizing L_X.

Dashed lines in Fig. 15 shows the re-simulated η_C using the same settings as in [9]. For a 1.6 × 0.8 × 0.8 mm³ L_X, L_X is 22 µH with 2 Ω ESR in [9], and re-simulated $\eta_{C(MAX)}$ is 89.2%. As the black solid line shows in Fig. 15, using this proposed theory, the optimal L_X is 4.4 µH with 244 mΩ ESR, and simulated $\eta_{C(MAX)}$ can reach 95.6%. $\eta_{C(MAX)}$ improvement is 6.4%. For a 3.0 × 3.0 × 1.5 mm³ L_X, L_X is 18 µH with 1 Ω ESR in [9], and re-simulated $\eta_{C(MAX)}$ is 95.1%. Using this proposed theory, the optimal L_X is 6.3 µH with 573 mΩ ESR, and simulated $\eta_{C(MAX)}$ can reach 97.2% as the grey solid line shows in Fig. 15. $\eta_{C(MAX)}$ improvement is 2.1%. Table II details the design parameters with and without optimizing L_X for comparable state-of-the-arts (that reports k_{LX} and uses the same process technology).

TABLE II: COMPARISON WITH THE STATE OF THE ART

Parameters	1.6 × 0.8 × 0.8 mm³ L_X		3.0 × 3.0 × 1.5 mm³ L_X		
	[9]	Optimal	[9]	[12]	Optimal
L_X'	22 µH	6.3 µH	18 µH	47 µH	4.4 µH
R_L'	2 Ω	570 mΩ	1 Ω	2 Ω	240 mΩ
$i_{L(PK)}$'	*31 mA	26 mA	*31 mA	*17 mA	57 mA
Sim. η_C'	89.2%	95.6%	95.1%	96.0%	97.2%

Simulation Setting: v_{IN} = 1.8 V, v_O = 1.0 V, P_O = 10 µW–10 mW.
*Extrapolated from transient waveforms.

V. CONCLUSIONS

This paper theorizes the optimal inductor and the optimal peak current for switched-inductor dc-dc converters, in order to achieve the highest DCM efficiency. With insightful analytical equations, the optimal inductor, peak current, and power switch sizing can be accurately derived. This proposed co-optimization strategy is absent in the state of the art. This theory is accurate and only produces 0.3–4.9% error when calculating the optimal setting. Using 180-nm process, the proposed SL buck-boost can achieve 93.8% efficiency with a 3.0 × 3.0 × 1.5 mm³ inductor. Compared with the state of the art, efficiency can be improved by 6.4% if the inductor is optimized.

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