Lowest V_{IN} Possible for Switched-Inductor Boost Converters

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***Abstract*—The minimum input voltage from which switched-inductor boost converters can draw power is a critical parameter, especially for power supplies that draw power from low-voltage sources like thermoelectric generators. When a battery is absent or fully discharged, the power supply relies on a millivolt input to wake and supply the system. This paper explains and quantifies what determines this minimum threshold both with and without a charged battery present. Analyses show that CMOS converters can wake with 44 mV, but not output power until the input source voltage v_S is 268 mV. With a charged battery, they can transfer energy with 4.6 mV, but not output net power until v_S is 64 mV.**

Keywords—Switched inductor, CMOS boost converter, power supply, charger, minimum input voltage, wake, startup.

I. Switched-Inductor Boost Converters

Wireless microsensors can save energy and save lives [1]–[4]. They can rely on 40–350-mV photovoltaic (PV) cells and thermoelectric generators (TEGs) for energy and power [5]. Chargers and regulators must therefore boost this 40–350 mV to 0.5–2.0 V so that wireless microsystems can operate.

With such a low input voltage v_{IN} and a resistive source, input power is very low. The power supply should therefore be as power efficient as possible. This is why switched inductors (SLs) are so popular. When the battery is absent or fully discharged, however, the SL in Fig. 1 must wake with a low v_{IN}. Even when the battery voltage is over the headroom voltage V_{HR} of the CMOS circuit [6], v_{IN} must still rise above a certain threshold for the boost converter to output net power.

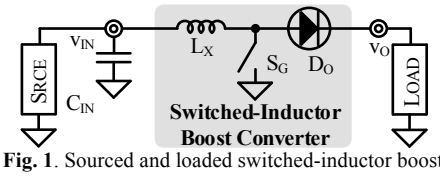

Fig. 1. Sourced and loaded switched-inductor boost.

The value of this theoretical limit is absent in literature [5], [7], [10], and [13]. This paper therefore explains and quantifies the lowest possible voltage of the input source with which SL boost converters can wake and can output net power. Sections II and III derive this threshold without and with a charged battery present, respectively. Section IV then discusses the effects of temperature and Section V draws final conclusions.

II. Wake Thresholds

M_G in the SL boost from Fig. 2 closes to energize L_X from v_{IN}. When M_G opens, L_X's current i_L charges C_{SW} until D_O forward-biases and steers i_L into the output C_O. But when the output (battery) is fully discharged, the SL relies on the low-voltage source v_S to wake the microsystem. R_S is the source resistance.

When the source v_S raises v_{IN} above the SL's first threshold, v_{IN} supplies the ring oscillator and drives the switch M_G. Below this functional threshold $v_{W(F)}$, the oscillator does not work. $v_{W(F)}$ is therefore the lowest v_S with which the SL can operate. The SL, however, cannot output power P_O until input power P_{IN} is high enough to supply the power lost in the SL. Thus, loss-limited output threshold $v_{W(O)}$ is the lowest v_S such that the SL can output power when waking without a charged output.

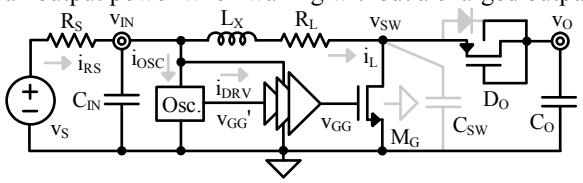

Fig. 2. Waking (input-supplied) switched-inductor boost.

A. Wake Functional Threshold

In the ring oscillator, one inverter drives another. So v_{IL} equals v_{OL}, and v_{IH} equals v_{OH}, where v_{IH}, v_{OH}, v_{IL}, and v_{OL} are the high and the low voltage levels of the input and the output of an inverter, respectively. An inverter is a series stack of PMOS and NMOS, so the gate-source voltages v_{GS}'s and the drain-source voltages v_{DS}'s of the inverter's PMOS and NMOS add up to v_{IN}:

$$v_{IN} = v_{SGP} + v_{GSN} = v_{SDP} + v_{DSN}, \tag{1}$$

where v_{IN} is the oscillator's supply voltage as labeled in Fig. 2.

When v_S is near $v_{W(F)}$, the ring oscillator is in sub-threshold (later validated by $v_{W(F)}$'s value), and the boost hardly draws current from v_S. So, v_{RS} (the voltage across R_S) is negligible and v_{IN} is near v_S. MOSFET sub-threshold current $i_{M(ST)}$ is [8]:

$$i_{M(ST)} = I_S\left(\frac{W}{L}\right)\exp\left(\frac{|v_{GS}|}{nV_t}\right)\left[1-\exp\left(\frac{-|v_{DS}|}{V_t}\right)\right], \tag{2}$$

where n is sub-threshold slope factor, and V_t is thermal voltage. When the inverter's input is high and output is low, its PMOS current $i_{MP(ST)}$ equals its NMOS current $i_{MN(ST)}$, and vice versa:

$$i_{MN(ST)} = i_{MP(ST)}\Big|_{v_{GSN}=v_{IH},\ v_{DSN}=v_{OL}} \tag{3}$$

and

$$i_{MP(ST)} = i_{MN(ST)}\Big|_{v_{GSN}=v_{IL},\ v_{DSN}=v_{OH}}. \tag{4}$$

The oscillator halts if v_{OH} equals v_{OL}, and it oscillates if v_{OH} is higher than v_{OL} [9]. Solving the lowest v_S such that v_{OH} is higher than v_{OL} using (1) – (4) gives $v_{W(F)}$. Fig. 3 plots the calculated $v_{W(F)}$ versus PMOS and NMOS widths W_P and W_N.

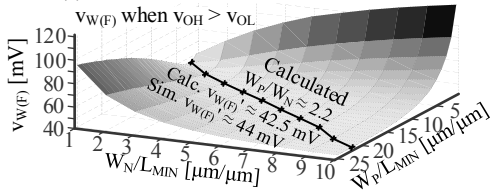

Fig. 3. Wake functional threshold across W_P and W_N.

In addition to [9], this paper finds the optimal W_P and W_N. In Fig. 3, the solid line labels the lowest $v_{W(F)}$ (denoted by $v_{W(F)}$'). It shows that the optimal W_P and W_N can counter the

differences between PMOS and NMOS in mobility μ, sub-threshold slope factor n, and MOSFET threshold voltage v_{TH} to balance their strengths, and thus can reduce $v_{W(F)}$. $v_{W(F)}$' is 44 mV in simulation. By observation the optimal sizes satisfy:

$$\left.\frac{(W/L)_P}{(W/L)_N}\right|_{v_S=v_{W(F)}'} = \frac{I_{S(N)}}{I_{S(P)}} = \frac{\mu_N n_N}{\mu_P n_P}\exp\left[\left(\frac{v_{TH(P)}}{n_P V_t}\right)-\left(\frac{v_{TH(N)}}{n_N V_t}\right)\right]. \quad (5)$$

Fig. 4 plots the error compared with simulations using 0.18-μm CMOS. The highest error of the $v_{W(F)}$ analysis is 7.06%. With v_{TH} variations, $v_{W(F)}$ is about 44–220 mV across corners.

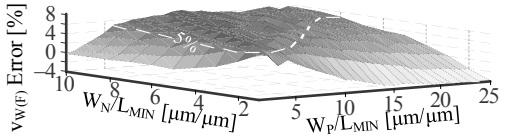

Fig. 4. Wake functional threshold error (compared with simulations).

B. Wake Loss-Limited Output Threshold

This paper finds $v_{W(O)}$ in two steps. First, find the lowest v_{IN} for the SL boost to output energy. Then, add v_{RS} to v_{IN} to get the minimum source voltage $v_{W(O)}$. High C_{IN} suppresses the voltage ripple of v_{IN}, so v_{IN}, v_{RS}, and i_{RS} are roughly dc. To reduce cost, M_G is not a native NMOS [10]. So, M_G is in sub-threshold (later validated by $v_{W(O)}$'s value) and its conduction resistance R_{MG} is much higher than the inductor's equivalent series resistance (ESR) R_L. Thus, R_L is neglected. The boost is in Discontinuous Conduction Mode (DCM) since the current level is low. The wake-up process ends if v_O is charged to V_{HR}.

The boost converter in Fig. 2 can output energy if the inductor L_X's peak energy $E_{L(PK)}$, along with the input energy $E_{IN(D)}$ provided by v_{IN} during the drain phase, can charge C_{SW} to one diode voltage v_D above the output voltage v_O:

$$E_{IN(D)} + E_{L(PK)} > E_{CSW(VO+VD)}. \quad (6)$$

Parasitic pin capacitance $C_{SW(PIN)}$ and M_G's drain capacitance add up to the total capacitance C_{SW}. C_{SW}'s loss $E_{CSW(VO+VD)}$ is:

$$E_{CSW(VO+VD)} = 0.5C_{SW}(v_O + v_D)^2. \quad (7)$$

Fig. 5 shows that this high sub-threshold R_{MG} limits the growth of L_X's current i_L. L_X's highest current is $i_{L(PK)}$, and $E_{L(PK)}$ is:

$$E_{L(PK)} = 0.5L_X i_{L(PK)}^2 = 0.5L_X\left(\frac{v_{IN}}{R_{MG}}\right)^2. \quad (8)$$

As i_L drains C_{SW} across drain time t_D (L_XC_{SW}'s quarter resonance period $t_{LC}/4$), i_L's sinusoid draws $E_{IN(D)}$ from v_{IN}:

$$E_{IN(D)} = v_{IN} i_{IN(D.AVG)} t_D \approx v_{IN} i_{L(D.AVG)} t_D = v_{IN}\left(\frac{2}{\pi}\right) i_{L(PK)}\left(\frac{t_{LC}}{4}\right), \quad (9)$$

where $i_{IN(D.AVG)}$ and $i_{L(D.AVG)}$ are the averaged input current and averaged inductor current across the drain time t_D (a quarter of t_{LC}). Substitute (7), (8), and (9) into (6), and solve for v_{IN}:

$$v_{IN} = (v_O + v_D)R_{MG}\sqrt{\frac{\pi C_{SW}}{\pi L_X + R_{MG}t_{LC}}}. \quad (10)$$

The oscillator's switching period t_{OSC} is long since it is in sub-threshold. So i_L is roughly a square wave (Fig. 5). Assuming the oscillator has 50% duty-cycle, L_X's average current $i_{L(AVG)}$ is:

$$i_{L(AVG)} \approx 0.5 i_{L(PK)} = 0.5\left(\frac{v_{IN}}{R_{MG}}\right). \quad (11)$$

The driver draws average current $i_{C(MG.AVG)}$ to charge/discharge M_G's gate capacitance $C_{G(MG)}$ to turn on/off M_G. $i_{C(MG.AVG)}$ is:

$$i_{C(MG.AVG)} = \frac{C_{G(MG)}v_{IN}}{t_{OSC}} = \frac{C_{OX}"W_{MG}L_{MG}v_{IN}}{t_{OSC}}, \quad (12)$$

where W_{MG} and L_{MG} are M_G's width and length. Neglecting the oscillator's current consumption i_{OSC}, the theory finds v_{RS} by:

$$v_{RS} = i_{RS(AVG)}R_S \approx \left(i_{L(AVG)} + i_{C(MG.AVG)}\right)R_S. \quad (13)$$

The theory then finds the minimum source voltage $v_{W(O)}$ by:

$$v_{W(O)} = v_{RS} + v_{IN}, \quad (14)$$

and $v_{W(O)}$ is the lowest v_S such that v_O can be charged to V_{HR}.

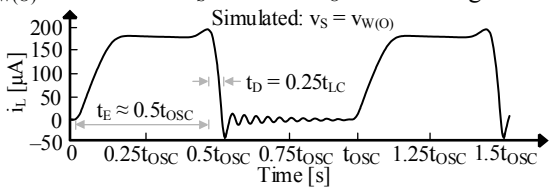

Fig. 5. Simulated inductor current during wake-up.

V_{HR} is 1V, R_S is 350 Ω (TEG resistance [11]), v_D is 0.4 V, and t_{OSC} is 100 μs in calculations and simulations. Fig. 6 plots the calculated $v_{W(O)}$ versus W_{MG} and L_X. Raising W_{MG} lowers R_{MG} and thus reduces the lowest v_{IN} required to output energy. But raising W_{MG} raises M_G's parasitic capacitance. This raises $i_{C(MG.AVG)}$ and raises v_{RS}. Therefore, the lowest source voltage $v_{W(O)}$ (denoted by $v_{W(O)}$' in Fig. 6) for a given L_X satisfies:

$$\frac{\partial v_{W(O)}}{\partial W_{MG}} = \frac{\partial v_{RS}}{\partial W_{MG}} + \left.\frac{\partial v_{IN}}{\partial W_{MG}}\right|_{v_{W(O)}'} = 0. \quad (15)$$

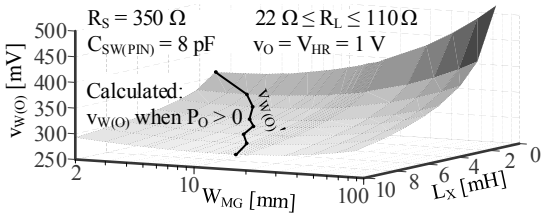

Fig. 6. Wake loss-limited output threshold across W_{MG} and L_X.

Fig. 7 plots the error compared with simulations using 0.18-μm CMOS. The highest error of the $v_{W(O)}$ analysis is 9.84%.

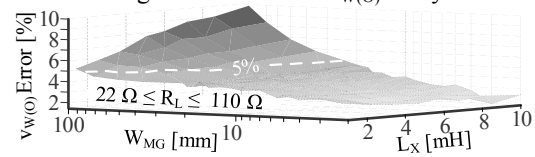

Fig. 7. Wake loss-limited output threshold error (compared with simulations).

Since the SL boost often wakes the system with a low v_S [6], $v_{W(O)}$ is the bottleneck and should be minimized. A higher L_X carries more energy for a given current, and thus can reduce $v_{W(O)}$. Since R_{MG} is much higher than the inductor's ESR R_L, we should use the highest L_X within the system's volume constraints regardless of R_L to minimize $v_{W(O)}$. For system miniaturization, miniature inductors should be used. Off-the-shelf miniature inductors can offer a highest L_X of 10 mH (3.7 × 3 × 3.6 mm^3) with 110 Ω ESR. With this miniature inductor, $v_{W(O)}$' is 268 mV in simulations and is 280 mV in calculations.

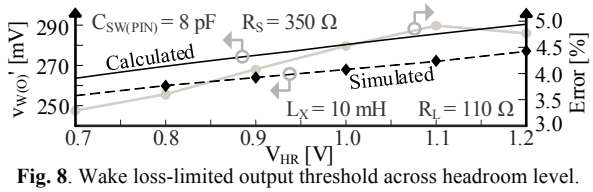

Fig. 8. Wake loss-limited output threshold across headroom level.

Fig. 8 plots the calculated and simulated $v_{W(O)}$' versus V_{HR}. Raising V_{HR} raises the loss in C_{SW} and raises $v_{W(O)}$'. Thus, V_{HR} should be the lowest voltage that meets system specifications.

III. Static Thresholds

When the SL boost's output v_O is above V_{HR}, which is the lowest voltage to supply the system's controller and to fully turn on power switches [6], v_O supplies the controller and the gate-driver in Fig. 9. This way, the boost charges or regulates v_O. Under this static steady-state condition, the static functional threshold $v_{S(F)}$ is the lowest v_S such that the boost can operate.

Static transfer-limited threshold $v_{S(X)}$ is the lowest v_S such that i_L can charge C_{SW} until comparator CP_O closes M_O [14] to let i_L drain and transfer energy into C_O. However, the boost does not output net power to v_O until input power P_{IN} is high enough to overcome all the power losses, including the power lost in the v_O-supplied controller and the gate-drivers. Static loss-limited output threshold $v_{S(O)}$ is thus the lowest v_S such that the boost can output net power when operating with a charged output.

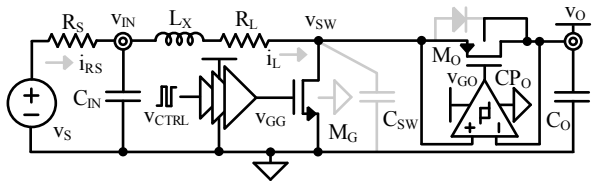

Fig. 9. Static (output-supplied) switched-inductor boost.

A. Static Functional Threshold

In static operation v_O is above V_{HR}, so the controller and the driver can always operate. Therefore, the SL boost can always draw energy from v_S if v_S is above 0 V. Therefore, $v_{S(F)}$ is 0 V.

B. Static Transfer-Limited Threshold

In static operation, the v_O-supplied driver turns M_G fully on. Thus, M_G's on-resistance R_{MG} is low (less than 1 Ω). Again, for miniaturized systems, the miniature inductor's ESR R_L can be up to 110 Ω. Thus, R_L overwhelms R_{MG}, and R_{MG} is neglected.

L_X can transfer energy to v_O if its peak energy $E_{L(PK)}$, along with the input energy $E_{IN(D)}$ offered by v_{IN} across the drain phase, can overcome R_L's loss E_{RL} and charge C_{SW} above v_O:

$$E_{IN(D)} + E_{L(PK)} > E_{CSW(VO)} + E_{RL}. \tag{16}$$

The boost operates differently to minimize $v_{S(X)}$. After v_{IN} is charged to v_S, the controller closes M_G to energize L_X. This maximizes the voltage across L_X. Moreover, a high C_{IN} holds v_{IN} close to v_S across the energizing time t_E until i_L reaches its limit. This maximizes $E_{L(PK)}$ and thus minimizes $v_{S(X)}$. $E_{L(PK)}$ is:

$$E_{L(PK)} = 0.5L_X i_{L(PK)}{}^2 = 0.5L_X\left(\frac{v_{IN}}{R_L}\right)^2 \approx 0.5L_X\left(\frac{v_S}{R_L}\right)^2. \tag{17}$$

$E_{CSW(VO)}$ is the energy lost in C_{SW}. $E_{CSW(VO)}$ is:

$$E_{CSW(VO)} = 0.5C_{SW}v_O{}^2. \tag{18}$$

Similarly, at $v_{S(X)}$, i_L drains into C_{SW} across a quarter of L_X-C_{SW} resonance period t_{LC}. During this drain time t_D, E_{RL} is:

$$E_{RL} = i_{L(D.RMS)}{}^2 R_L t_D \approx \left(\frac{i_{L(PK)}}{\sqrt{2}}\right)^2 R_L\left(\frac{t_{LC}}{4}\right), \tag{19}$$

where $i_{L(D.RMS)}$ is L_X's root-mean-square (RMS) current during t_D. Like (9), during this drain time t_D, v_{IN} offers energy $E_{IN(D)}$:

$$E_{IN(D)} = v_{IN} i_{IN(D.AVG)} t_D \approx v_S i_{L(D.AVG)} t_D \approx v_S\left(\frac{2}{\pi}\right) i_{L(PK)}\left(\frac{t_{LC}}{4}\right). \tag{20}$$

Substitute (17), (18), (19), and (20) into (16), and solve for v_S:

$$v_{S(X)} = v_S \approx R_L v_O \sqrt{\frac{C_{SW}}{L_X - (R_L t_{LC}/4) + (R_L t_{LC}/\pi)}}. \tag{21}$$

Fig. 10 plots the calculated $v_{S(X)}$ versus L_X and R_L when v_O is 1.4 V. Fig. 11 shows that the highest error is 10.99%.

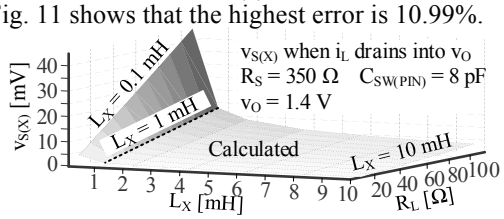

Fig. 10. Static transfer-limited threshold across L_X and R_L.

For miniaturization, the inductor used in static operation must be the same inductor used for system wake-up (10 mH with 110 Ω ESR in this paper) to reduce system volume. In this case, $v_{S(X)}$ is 4.6 mV in simulation (4.36 mV in calculation).

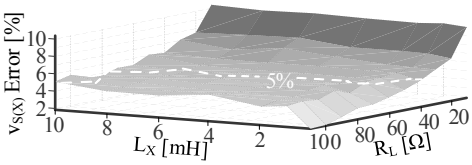

Fig. 11. Static transfer-limited threshold error (compared with simulations).

C. Static Loss-Limited Output Threshold

Similarly, v_{IN}, v_{RS}, i_{RS} are roughly dc in static operation, and the boost converter operates in DCM. The input power P_{IN} is:

$$P_{IN} = P_S - P_{RS}, \tag{22}$$

where P_S is the power from v_S, P_{RS} is the power burned in R_S.

$$P_S = v_S i_{RS(AVG)} = v_S\left(\frac{v_S - v_{IN}}{R_S}\right), \tag{23}$$

and

$$P_{RS} = \frac{(v_S - v_{IN})^2}{R_S}. \tag{24}$$

At $v_{S(O)}$, v_{IN} is much lower than v_O, so drain time t_D is much less than energizing time t_E (Fig. 12). L_X's peak current $i_{L(PK)}$ is:

$$i_{L(PK)} = \left(\frac{v_{IN}}{L_X}\right) t_E \approx \left(\frac{v_{IN}}{L_X}\right) t_X, \tag{25}$$

where $t_X = (t_E + t_D)$ is the time during which the boost converter draws and transfers energy. R_L's power loss P_{RL} is:

$$P_{RL} = i_{L(RMS)}{}^2 R_L\left(\frac{t_X}{t_{SW}}\right) \approx \left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2 R_L\left(\frac{f_{SW}}{f_X}\right), \tag{26}$$

where $i_{L(RMS)}$ is the RMS value of i_L, f_X is the reciprocal of t_X, and f_{SW} is the switching frequency. C_{SW}'s power loss P_{CSW} is:

$$P_{CSW} = 0.5C_{SW}v_O{}^2 f_{SW}. \tag{27}$$

Again, the inductor used in static operation is the same inductor used for system wake-up. Thus, R_L is much higher than R_{MG}, and R_L's ohmic loss P_{RL} is much higher than R_{MG}'s conduction loss P_{MR}. Also, for optimized power switches, the gate-drive loss P_{MC} should be equal to the conduction loss P_{MR} [12]. Thus, P_{MR} and P_{MC} are both negligible compared to P_{RL}.

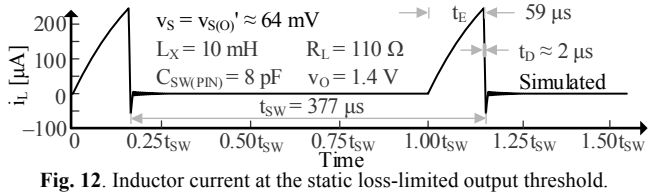

Fig. 12. Inductor current at the static loss-limited output threshold.

Part of the controller is always on (i.e., voltage monitoring circuits), and draws steady state current $i_{Q(SS)}$. Its loss $P_{Q(SS)}$ is:

$$P_{Q(SS)} = i_{Q(SS)} v_O. \tag{28}$$

The other part of the controller is duty-cycled (i.e., comparator CP_O), and draws current $i_{Q(X)}$ only during t_X. Its loss $P_{Q(X)}$ is:

$$P_{Q(X)} = i_{Q(X)} v_O \left(\frac{t_X}{t_{SW}}\right) = i_{Q(X)} v_O \left(\frac{f_{SW}}{f_X}\right). \quad (29)$$

Neglecting P_{MR} and P_{MC}, the total loss is approximately:

$$P_{LOSS} \approx P_{RL} + P_{CSW} + P_{Q(SS)} + P_{Q(X)}. \quad (30)$$

The minimum v_S such that P_{IN} is no less than P_{LOSS} is $v_{S(O)}$:

$$\begin{aligned} v_{S(O)} &= i_{RS(AVG)} R_S + v_{IN} = i_{IN(AVG)} R_S + v_{IN} = \left(\frac{P_{IN}}{v_{IN}}\right) R_S + v_{IN} \\ &= \left(\frac{P_{LOSS}}{v_{IN}}\right) R_S + v_{IN} \approx \left(\frac{P_{RL} + P_{CSW} + P_{Q(SS)} + P_{Q(X)}}{v_{IN}}\right) R_S + v_{IN}. \end{aligned} \quad (31)$$

Figure 13 plots the simulated and calculated $v_{S(O)}$ when $i_{Q(SS)}$ is 151 nA [13], $i_{Q(X)}$ is 2.45 µA [14], and f_X is 16.7 kHz. P_{IN} rises when f_{SW} climbs because the converter draws energy more frequently. Except, P_{CSW} and $P_{Q(X)}$ also increase with f_{SW}. So the lowest $v_{S(O)}$ (called $v_{S(O)}'$) results at the f_{SW} that balances P_{IN}, P_{CSW}, and $P_{Q(X)}$. (v_{IN} is not the $0.5v_S$ that conventional maximum-power-point theory predicts because the inductor needed for wake-up adds R_L's 110 Ω to R_S. So with the values mentioned, theory predicts $v_{S(O)}'$ is 63 mV and simulations show that $v_{S(O)}'$ is 64 mV, where the highest error in Fig. 14 is 2.25%. $v_{S(O)}'$ in [15] is lower at 20 mV because R_L in [15] is only 230 mΩ, which requires a bulkier L_X.

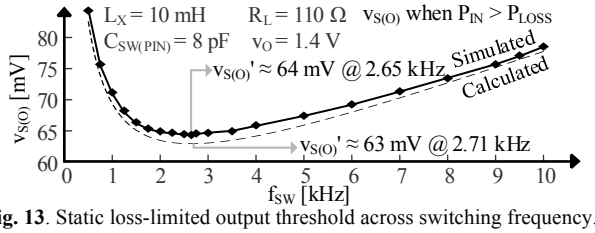

Fig. 13. Static loss-limited output threshold across switching frequency.

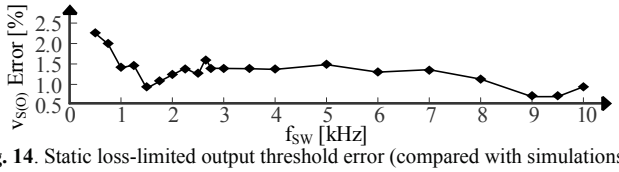

Fig. 14. Static loss-limited output threshold error (compared with simulations).

IV. Effects of Temperature

Figure 15 plots v_{OH}, v_{OL}, and trip-point v_{TRIP} of an optimally sized inverter under different supply voltages v_S at 0°C, 27°C, and 85°C when normalized to the thermal voltage V_t. When v_S is below $v_{W(F)}'$, v_{OH} equals v_{OL}, so the inverter cannot invert and cannot function. When v_S is higher than $v_{W(F)}'$, v_{OH} is higher than v_{OL}. So the inverter can trip and the oscillator can function. Simulations at these three temperatures match and show that $v_{W(F)}'$ is $1.69V_t$ to $1.76V_t$. During wake-up, M_G is in sub-threshold, where current is largely the result of diffusion. So R_{MG} falls as temperature climbs, which means $i_{L(PK)}$ and $E_{L(PK)}$ rise. $v_{W(O)}'$ therefore drops when temperature climbs.

Since wake-up requires an L_X with a R_L that is high and climbs with temperature, static operation suffers the same R_L. $v_{S(X)}$ and $v_{S(O)}$ therefore rise with temperature. Table I summarizes the input source voltage thresholds and their simulated temperature coefficients (TCs).

V. Conclusions

This paper theorizes the minimum input source voltage v_S for switched-inductor boost converters with and without a charged battery. Theory shows that without a charged battery, boost converters can wake with 44 mV, but not output power until v_S is 268 mV. With a charged battery, they can transfer energy with 4.6 mV, but cannot output power until v_S is 64 mV. Simulations using 0.18-µm CMOS validate this theory.

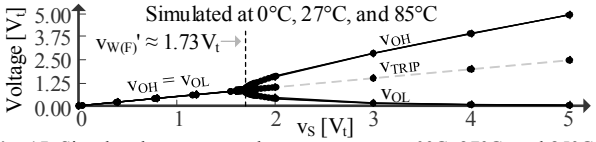

Fig. 15. Simulated v_{OH}, v_{OL}, and v_{TRIP} across v_S at 0°C, 27°C, and 85°C.

Table I: Voltage Thresholds and Temperature Coeefficents (TCs)

	$v_{W(F)}$	$v_{W(O)}$	$v_{S(F)}$	$v_{S(X)}$	$v_{S(O)}$	Unit
Theory 27°C	42.5	280	0	4.36	63	mV
Simulated 27°C	44	268	0	4.6	64	mV
Error	3.4%	4.5%	0	5.2%	1.6%	
Simulated TC	150	–700	0	20	90	µV/°C

* R_S = 350 Ω, L_X = 10 mH, R_L = 110 Ω at 27°C, and $C_{SW(PIN)}$ = 8 pF.

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