Lowest $V_{\text{IN}}$ Possible for Switched-Inductor Boost Converters

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Abstract—The minimum input voltage from which switched-inductor boost converters can draw power is a critical parameter, especially for power supplies that draw power from low-voltage sources like thermoelectric generators. When a battery is absent or fully discharged, the power supply relies on a millivolt input to wake and supply the system. This paper explains and quantifies what determines this minimum threshold both with and without a charged battery present. Analyses show that CMOS converters can wake with 44 mV, but not output power until the input source voltage $V_S$ is 268 mV. With a charged battery, they can transfer energy with 4.6 mV, but not output net power until $V_S$ is 64 mV.

Keywords—Switched inductor, CMOS boost converter, power supply, charger, minimum input voltage, wake, startup.

I. SWITCHED-INDUCTOR BOOST CONVERTERS

Wireless microsystems can save energy and save lives [1]–[4]. They can rely on 40–350-mV photovoltaic (PV) cells and thermoelectric generators (TEGs) for energy and power [5]. Chargers and regulators must therefore boost this 40–350-mV photovoltaic cells and the low voltage levels of the input and the output of an inverter, respectively. An inverter is a series stack of PMOS and NMOS, so the gate-source voltages $V_{GS}$'s and the drain-source voltages $V_{DS}$'s of the inverter's PMOS and NMOS add up to $V_{IN}$:

$$V_{IN} = V_{GSP} + V_{GSN} = V_{SDP} + V_{DSN}, \quad (1)$$

where $V_{IN}$ is the oscillator's supply voltage as labeled in Fig. 2. When the inverter's input is high and output is low, its PMOS and NMOS current $i_{MPST}$ equals its NMOS current $i_{MNST}$, and vice versa:

$$i_{MNST} = i_{MPST} = I_n \frac{W}{L} \exp \left( \frac{V_{GS}}{nV_T} \right) \left[ 1 - \exp \left( \frac{-V_{DS}}{V_T} \right) \right], \quad (2)$$

where $n$ is sub-threshold slope factor, and $V_T$ is thermal voltage. When the inverter's input is high and output is low, its PMOS current $i_{MPST}$ equals its NMOS current $i_{MNST}$, and vice versa:

$$i_{MNST} = i_{MPST} = I_n \frac{W}{L} \exp \left( \frac{V_{GS}}{nV_T} \right) \left[ 1 - \exp \left( \frac{-V_{DS}}{V_T} \right) \right]. \quad (3)$$

The oscillator halts if $V_{OH}$ equals $V_{OL}$, and it oscillates if $V_{OH}$ is higher than $V_{OL}$ [9]. Solving the lowest $V_{S}$ such that $V_{OH}$ is higher than $V_{OL}$ using (1)–(4) gives $V_{W(FL)}$. Fig. 3 plots the calculated $V_{W(FL)}$ versus PMOS and NMOS widths $W_P$ and $W_N$.

In addition to [9], this paper finds the optimal $W_P$ and $W_N$. In Fig. 3, the solid line labels the lowest $V_{W(FL)}$ (denoted by $V_{W(FL)}$). It shows that the optimal $W_P$ and $W_N$ can counter the...
differences between PMOS and NMOS in mobility $\mu$, sub-threshold slope factor $n$, and MOSFET threshold voltage $V_{TH}$ to balance their strengths, and thus can reduce $V_{W(IF)}$. $V_{W(IF)}'$ is 44 mV in simulation. By observation the optimal sizes satisfy:

$$\frac{(W/L)_{W}}{(W/L)_{IN}} = \frac{I_{W}}{I_{IN}} = \frac{\mu_{W}n_{W}e^{\left(\frac{V_{TH}}{n_{W}V_{IN}} - \frac{V_{TH}}{n_{IN}V_{IN}}\right)}}{\mu_{IN}n_{IN}}. \tag{5}$$

Fig. 4 plots the error compared with simulations. The highest error of the $V_{W(IF)}$ analysis is 7.06%. With $V_{TH}$ variations, $V_{W(IF)}'$ is about 44–220 mV across corners.

B. Wake Loss-Limited Output Threshold

This paper finds $V_{W(O)}$ in two steps. First, find the lowest $V_{IN}$ for $E_{IN(D)} + E_{L(PK)} > E_{CSW}(V_{O} + V_{D})$. Substitute (7), (8), and (9) into (6), and solve for $V_{IN}$:

$$V_{IN} = v_{RS} + v_{L} + v_{W(O)} = v_{RS} + v_{L}, \tag{14}$$

and $V_{W(O)}$ is the lowest $V_{S}$ such that $V_{O}$ can be charged to $V_{HR}$.

The highest error of the $V_{W(O)}$ analysis is 9.84%.

$V_{HR}$ is 1V, $R_{S}$ is 350 $\Omega$ (TEG resistance [11]), $V_{D}$ is 0.4 V, and $I_{OSC}$ is 100 $\mu$A in calculations and simulations. Fig. 6 plots the calculated $V_{W(O)}$ versus $W_{MG}$ and $L_{X}$. Raising $W_{MG}$ lowers $R_{MG}$ and thus reduces the lowest $V_{IN}$ required to output energy. But raising $W_{MG}$ raises $M_{G}$'s parasitic capacitance. This raises $i_{C(MG,AVG)}$ and raises $v_{RS}$. Therefore, the lowest source voltage $V_{W(O)}$ (denoted by $V_{W(O)}'$ in Fig. 6) for a given $L_{X}$ satisfies:

$$\frac{\partial V_{W(O)}}{\partial W_{MG}} = \frac{\partial v_{RS}}{\partial W_{MG}} + \frac{\partial v_{IN}}{\partial W_{MG}} \approx 0. \tag{15}$$

where $W_{MG}$ and $L_{MG}$ are $M_{G}$'s width and length. Neglecting the oscillator's current consumption $I_{OSC}$, the theory finds $V_{RS}$ by:

$$v_{RS} = i_{RS(AVG)}R_{S} = \left(i_{L(AVG)} + i_{C(MG,AVG)}\right)R_{S}. \tag{13}$$

The theory then finds the minimum source voltage $V_{W(O)}'$ by:

$$V_{W(O)}' = v_{RS} + v_{IN}. \tag{14}$$

Since the SL boost often wakes the system with a low $V_{S}$ [6], $V_{W(O)}'$ is 350 $\Omega$ (TEG resistance [11]), $V_{D}$ is 0.4 V, and $I_{OSC}$ is 100 $\mu$A in calculations and simulations. Fig. 7 plots the calculated $V_{W(O)}'$ versus $W_{MG}$ and $L_{X}$. Raising $W_{MG}$ lowers $R_{MG}$ and thus raises $V_{W(O)}'$. Thus, $V_{HR}$ should be the lowest voltage that meets system specifications.
III. STATIC THRESHOLDS

When the SL boost's output $v_O$ is above $V_{HR}$, which is the lowest voltage to supply the system's controller and to fully turn on power switches [6], $v_O$ supplies the controller and the gate-driver in Fig. 9. This way, the boost charges or regulates $v_O$ until input power $P_{IN}$ is high enough to overcome all the power losses, including the power lost in the $v_O$-supplied controller and the gate-drivers. Static loss-limited output threshold $v_{SOX}$ is thus the lowest $v_S$ such that the boost can operate.

Static transfer-limited threshold $v_{SOX}$ is the lowest $v_S$ such that $i_L$ can charge $C_{SW}$ until comparator $CPO$ closes $MO$ [14] to let $i_L$ drain and transfer energy into $C_O$. However, the boost does not output net power to $v_O$ until input power $P_{IN}$ is high enough to overcome all the power losses, including the power lost in the $v_O$-supplied controller and the gate-drivers. Static loss-limited output threshold $v_{SOX}$ is thus the lowest $v_S$ such that the boost can output net power when operating with a charged output.

A. Static Functional Threshold

In static operation $v_O$ is above $V_{HR}$, so the controller and the driver can always operate. Therefore, the SL boost can always draw energy from $v_S$ if $v_S$ is above $0$ V. Therefore, $v_{SF}$ is $0$ V.

B. Static Transfer-Limited Threshold

In static operation, the $v_O$-supplied driver turns $M_G$ fully on. Thus, $M_G$'s on-resistance $R_{MG}$ is low (less than $1$ Ω). Again, for miniaturized systems, the miniature inductor's ESR $R_L$ can be up to $110$ Ω. Thus, $R_L$ overwhelms $R_{MG}$, and $R_{MG}$ is neglected.

$L_X$ can transfer energy to $v_O$ if its peak energy $E_{L(PK)}$ offers energy $E_{IN(D)}$ across the drain phase $t_D$. $E_{L(PK)}$ is:

$$E_{L(PK)} = 0.5 i_L(PK)^2 R_L$$

(17)

$E_{CSW(VO)}$ is the energy lost in $C_{SW}$. $E_{CSW(VO)}$ is:

$$E_{CSW(VO)} = 0.5 C_{SW} v_O^2$$

(18)

Similarly, at $v_{SOX}$, $i_L$ drains into $C_{SW}$ across a quarter of $L_X$-$C_{SW}$ resonance period $t_{LC}$. During this drain time $t_D$, $E_{RL}$ is:

$$E_{RL} = i_L(DMS)^2 R_L t_D = \frac{i_L(PK)^2}{2} R_L t_L = \frac{i_L t_L}{4}$$

(19)

where $i_L(DMS)$ is $L_X$'s root-mean-square (RMS) current during $t_D$. Like (9), during this drain time $t_D$, $v_{IN}$ offers energy $E_{IND}$:

$$E_{IND} = \frac{v_{IN}}{2 \pi} i_{L(DMS)} t_D = v_{IN} (\frac{2}{\pi}) i_L(PK) t_L$$

(20)

Substitute (17), (18), (19), and (20) into (16), and solve for $v_S$:

$$v_{SOX} = v_S \approx R_L v_O \sqrt{\frac{C_{SW}}{L_X(R_{L}t_L/4)+R_L t_L/\pi}}$$

(21)

For miniaturization, the inductor used in static operation must be the same inductor used for system wake-up (10 mH with 110 Ω ESR in this paper) to reduce system volume. In this case, $v_{SOX}$ is 4.6 mV in simulation (4.36 mV in calculation).

C. Static Loss-Limited Output Threshold

Similarly, $v_{IN}$, $v_{SOX}$, $i_L$ is roughly dc in static operation, and the boost converter operates in DCM. The input power $P_{IN}$ is:

$$P_{IN} = P_S - P_{RS}$$

(22)

where $P_S$ is the power from $v_S$, $P_{RS}$ is the power burned in $R_S$.

$$P_S = v_S i_{RS AVG} = \frac{v_S - v_{IN}}{R_S}$$

(23)

and

$$P_{RS} = \frac{(v_S - v_{IN})^2}{R_S}$$

(24)

At $v_{SOX}$, $v_{IN}$ is much lower than $v_O$, so drain time $t_D$ is much less than energizing time $t_E$ (Fig. 12). $L_X$'s peak current $i_L(PK)$ is:

$$i_L(PK) = \frac{v_{IN}}{L_X} t_E = \frac{v_{IN}}{L_X} t_X$$

(25)

where $t_X = (t_E + t_D)$ is the time during which the boost converter draws and transfers energy. $R_L$'s power loss $P_{RL}$ is:

$$P_{RL} = i_{L(RMS)}^2 R_L \left(\frac{L_X}{t_{SW}}\right) = \frac{(L_X t_{SW})^{2}}{L_X \sqrt{3}} R_L$$

(26)

where $i_{L(RMS)}$ is the RMS value of $i_L$, $f_X$ is the reciprocal of $t_X$, and $f_{SW}$ is the switching frequency. $C_{SW}$'s power loss $P_{CSW}$ is:

$$P_{CSW} = 0.5 C_{SW} v_O^2 t_{SW}$$

(27)

Again, the inductor used in static operation is the same inductor used for system wake-up. Thus, $R_L$ is much higher than $R_{MG}$, and $R_L$'s ohmic loss $P_{RL}$ is much higher than $R_{MG}$'s conduction loss $P_{MR}$. Also, for optimized power switches, the gate-drive loss $P_{MC}$ should be equal to the conduction loss $P_{MR}$ [12]. Thus, $P_{MR}$ and $P_{MC}$ are both negligible compared to $P_{RL}$.

Fig. 10 plots the calculated $v_{SOX}$ versus $L_X$ and $R_L$ when $v_O$ is 1.4 V. Fig. 11 shows that the highest error is 10.99%.

Fig. 11. Static transfer-limited threshold across $L_X$ and $R_L$.

FIG. 10. Static transfer-limited threshold across $L_X$ and $R_L$.

Part of the controller is always on (i.e., voltage monitoring circuits), and draws steady state current $i_{Q(SS)}$. Its loss $P_{Q(SS)}$ is:

$$P_{Q(SS)} = i_{Q(SS)} v_O$$

(28)
The other part of the controller is duty-cycled (i.e., comparator CP0), and draws current iQ(X) only during tX. Its loss PLOSS is:

\[ P_{LOSS}\approx P_{R} + P_{CSW} + P_{Q(X)} \]

(29)

Neglecting PMR and PMC, the total loss is approximately:

\[ P_{LOSS}\approx P_{R} + P_{CSW} + P_{Q(X)} + P_{Q(X)} \]

(30)

The minimum \( P_{IN} \) such that \( P_{LOSS} \) is less than \( P_{LOSS} \) is:

\[ v_{S(O)} = i_{RS(AVG)} R_S + v_{IN} = i_{S(O)} R_S + v_{IN} \]

(31)

Figure 13 plots the simulated and calculated \( v_{S(O)} \) when \( i_{Q(SS)} \) is 151 nA [13], \( i_{Q(X)} \) is 2.45 µA [14], and \( f_X \) is 16.7 kHz. \( P_{IN} \) rises when \( f_X \) climbs because the converter draws energy more frequently. Except, PCSW and PQ(X) also increase with fSW. So the lowest \( v_{S(O)} \) (called \( v_{S(O)}' \)) results at the fSW that balances \( R_L \)'s 110 Ω to \( R_L \). So with the values mentioned, theory predicts \( v_{S(O)}' \) is 63 mV and simulations show that \( v_{S(O)}' \) is 64 mV, where the highest error in Fig. 14 is 2.25%. \( v_{S(O)}' \) in [15] is lower at 20 mV because \( R_L \) in [15] is only 230 mΩ, which requires a bulkier \( L_X \).

**IV. EFFECTS OF TEMPERATURE**

Figure 15 plots \( v_{OH}, v_{OL}, \) and trip-point \( v_{TRIP} \) of an optimally sized inverter under different supply voltages \( V_S \) at 0°C, 27°C, and 85°C when normalized to the thermal voltage \( V_T \). When \( V_S \) is below \( V_W(F) \), \( v_{OH} \) equals \( V_T \), so the inverter cannot invert and cannot function. When \( V_S \) is higher than \( V_W(F) \), \( v_{OH} \) is higher than \( V_T \). So the inverter can trip and the oscillator can function. Simulations at these three temperatures match and show that \( V_W(F) \) is 1.69V for 1.76V. During wake-up, \( M_G \) is in sub-threshold, where current is largely the result of diffusion. So \( R_{MG} \) falls as temperature climbs, which means \( i_{LPK} \) and \( E_{LPK} \) rise. \( v_{W(F)} \) therefore drops when temperature climbs.

Since wake-up requires an \( L_X \) with a \( R_L \) that is high and climbs with temperature, static operation suffers the same \( R_L \). \( v_{S(X)} \) and \( v_{S(O)} \) therefore rise with temperature. Table I summarizes the input source voltage thresholds and their simulated temperature coefficients (TCs).

**V. CONCLUSIONS**

This paper theorizes the minimum input source voltage \( V_S \) for switched-inductor boost converters with and without a charged battery. Theory shows that without a charged battery, boost converters can wake with 44 mV, but not output power until \( V_S \) is 268 mV. With a charged battery, they can transfer energy with 4.6 mV, but cannot output power until \( V_S \) is 64 mV. Simulations using 0.18-µm CMOS validate this theory.

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**REFERENCES**


