Stability and Design of Hysteretic Current-Mode Single-Inductor Multiple-Output Power Supplies

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***Abstract*—When supplied well and with little power losses, multifunctional microsystems can add life- and cost-saving intelligence to hospitals, factories, and cars. Unfortunately, fitting the multiple power supplies that diverse subsystems require into millimeters is challenging. One reason for this is, although efficient and therefore necessary, inductors are bulky. And supplying several outputs with one switched inductor requires several feedback loops that respond quickly. Even though hysteretic loops can react within one switching cycle, the nonlinear dynamics of intertwined hysteretic loops are difficult to manage. This paper explains how to analyze and design these fast single-inductor multiple-output (SIMO) power supplies. Designed this way, the 5-output, 500-mA SIMO presented recovers all outputs after 400-mA load dumps in less than 26 µs, which is only 6 µs over the time the uninterrupted inductor requires to slew its current to a level that can supply all loads.**

***Index Terms*—Single switched inductor, multiple output, SIMO, dc–dc converter, power supply, hysteretic, current mode.**

I. Multifuntional Microsystems

Microsystems that sense, process, store, transmit, and receive information can save lives, energy, and money [1]. Unfortunately, tiny batteries exhaust quickly, so functional blocks cannot afford to lose unnecessary power. This is why subsystems often derive power from dedicated power supplies [2], and why wireless microsensors like Fig. 1 shows can incorporate three to five independent supplies [3].

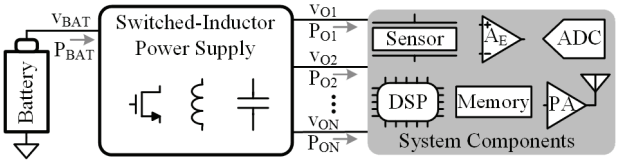

Fig. 1. Wireless microsensor.

Of alternatives, linear supplies are small and quick, but also lossy when supplying mW's [4]. Switched capacitors are small and power efficient only when supplying µW's [5]. And although efficient, switched inductors are bulky. But since power losses are so critical, switched inductors are necessary, but only acceptable when confined to one inductor L_O [6]–[8].

Unfortunately, L_O can only supply one output at a time. So to keep outputs from drooping too much, L_O should connect to outputs as often as possible. So L_O should not energize and drain each time L_O connects to a new output. Instead, L_O should supply all outputs within one switching cycle of L_O [9].

To keep sudden load dumps from similarly offsetting outputs, the power-supply system should also react quickly. Unfortunately, pulse-width modulated (PWM) loops require multiple switching cycles to respond [10]. And although hysteretic loops react within one cycle [10]–[12], stability analysis and design of single-inductor multiple-output (SIMO) supplies are largely absent in literature.

This paper shows how to analyze and design hysteretic SIMO supplies. For this, Section II first describes how to manage the loops that control the system. Sections III–V then explain loop operation and limits. For validation, Section VI demonstrates how a 5-output, 500-mA SIMO designed this way responds. And Section VII finishes with conclusions.

II. Hysteretic Current-Mode SIMO Power Supply

A switched inductor L_O into an output capacitor C_O produces the effects of two poles: L_O pole p_L and C_O pole p_C [13]. Regulating L_O's current i_L to a frequency-independent level is like transforming L_O into a current source. So when directed into C_O, i_L establishes p_C, but not p_L [13]. This is the purpose of a current-mode loop like Fig. 2 shows around L_O: to remove p_L. This way, the output capacitor of each voltage loop establishes one dominant low-frequency pole that ensures its loop gain reaches unity with sufficient phase margin [14].

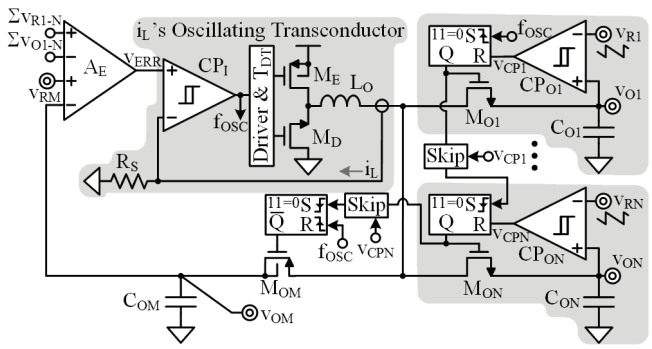

Fig. 2. Hysteretic current-mode SIMO power-supply system.

The current loop here is a hysteretic oscillator that outputs a rippling current i_L about a level that the error amplifier A_E sets [12]. Each independent output v_{O1} through v_{ON} incorporates a regulating loop that feeds sufficient i_L to satisfy each load. With A_E, the master loop then adjusts i_L so that the last output v_{OM} receives enough leftover i_L to satisfy v_{OM}'s load. L_O therefore feeds one output at a time, from v_{O1} to v_{OM}.

Since each load drains energy from L_O, individual load dumps can starve or oversupply other outputs to the extent that L_O requires several cycles to recover. To diminish these cross-regulation effects, each independent loop can satisfy its own

The authors thank J.D. Morris, B. Legates, T. Bonte, and Linear Technology Corporation in Milpitas, California, for their sponsorship and support.

load before redirecting L_O to another output. As such, independent loops can respond within L_O's switching period t_{OSC}. And since v_{OM} can starve or receive too much L_O energy before the master loop can adjust i_L, v_{OM}'s loop adjusts i_L after one or more switching cycles. This way, v_{O1}–v_{ON} exhibit minimal cross-regulation effects and v_{OM} suffers effects that the master loop corrects after some cycles.

III. Oscillatating Transconductor

Comparator CP_I, drivers, M_E and M_D, L_O, and R_S close an oscillating loop that ripples i_L about a level that A_E's v_{ERR} and R_S set. For this, M_E energizes L_O until R_S's voltage translation of i_L reaches CP_I's upper threshold. So irrespective of which output L_O feeds, i_L in Fig. 3 climbs until i_LR_S rises above v_{ERR} by half of CP_I's hysteresis v_{HYS}. M_D then drains L_O until i_LR_S reaches CP_I's lower threshold $v_{ERR} - 0.5v_{HYS}$. i_L therefore swings across v_{HYS}/R_S and about v_{ERR}/R_S. And the time that lapses across these events is the oscillating period t_{OSC}.

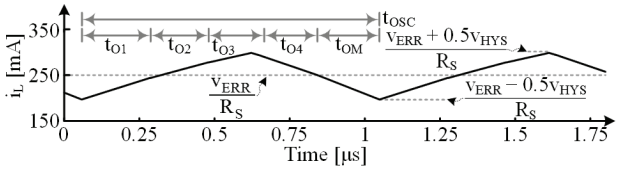

Fig. 3. Simulated inductor current for an evenly loaded 5-output SIMO.

A. Closed-Loop Response

Variations in A_E's v_{ERR} shift the level about which i_L ripples. So the oscillator is basically a transconductor whose small-signal input is v_{err}, output is L_O's mid-level current i_l, and low-frequency input–output translation and gain G_{OSC0} is $1/R_S$:

$$G_{OSC} = \frac{i_l}{v_{err}} = \frac{G_{OSC0}}{1+\frac{s}{2\pi f_{IBW}}} = \frac{1/R_S}{1+\frac{s}{2\pi f_{IBW}}}. \qquad (1)$$

Since CP_I is considerably faster than the oscillating period t_{OSC}, CP_I responds within t_{OSC}. So if v_{ERR} variations are small, t_{OSC} in Fig. 3 sets the loop's bandwidth f_{IBW} to nearly f_{OSC}.

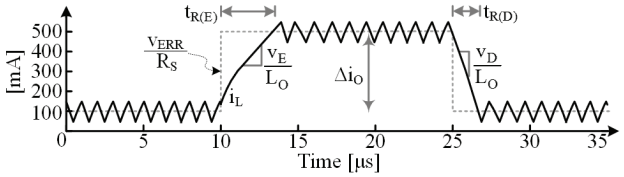

Fig. 4. Simulated closed-loop response to 50–450-mA load dumps.

In practice, load dumps can drain L_O to the extent A_E produces a wide variation in v_{ERR}, and as a result, in i_L. Unfortunately, L_O's voltage v_L slews i_L at v_L/L_O, like Fig. 4 shows at 10–14 and 25–27 µs. This delays the response by the time i_L requires to cover the entire load-dump variation Δi_O. Since v_L depends on which output L_O connects to, the longest delay $t_{R(MAX)}$ results at $\Delta i_{O(MAX)}$ and $v_{L(MIN)}$, which is L_O's lowest possible energizing or drain voltage v_E or v_D:

$$t_{R(MAX)} \approx \Delta i_{O(MAX)}\left(\frac{L_O}{v_{L(MIN)}}\right) \equiv 4R_RC_R = \frac{4}{2\pi f_{IBW(MIN)}}. \qquad (2)$$

Since an R_RC_R circuit reaches 98% of its target after four time constants, $t_{R(MAX)}$ is roughly the equivalent of four time constants [14]. The minimum bandwidth $f_{IBW(MIN)}$ is therefore

$$f_{IBW(MIN)} \approx \frac{4}{2\pi}\left(\frac{1}{\Delta i_{O(MAX)}}\right)\left(\frac{v_{L(MIN)}}{L_O}\right) \le f_{OSC}. \qquad (3)$$

So the oscillator behaves like a transconductor current source with a $1/R_S$ translation and no L_O dynamics below $f_{IBW(MIN)}$.

IV. Independent Voltage Loops

The oscillator starts every cycle by energizing L_O (with f_{OSC} in Fig. 2) to the first independent output v_{O1} (by way of M_E and M_{O1}). L_O's i_L then charges C_{O1} like Fig. 5 shows until v_{O1} reaches comparator CP_{O1}'s threshold v_{R1}. At that point, CP_{O1} opens M_{O1} and closes M_{O2} to redirect i_L to the next output. This lets v_{O1}'s load discharge C_{O1} until f_{OSC} reconnects L_O back to v_{O1}. Since identical feedback loops close each independent output v_{OI}, i_L feeds all outputs like a current source and each v_{OI} ripples and peaks to its respective target v_{RI}. In short, each loop regulates v_{OI}'s peak to its target v_{RI}.

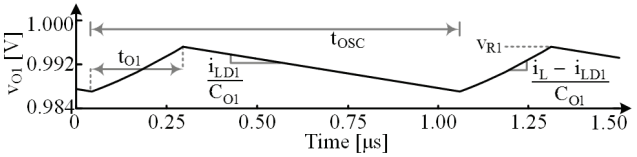

Fig. 5. Simulated response of the first independent output in a 5-output SIMO.

When the load is absent, v_{O1} does not droop enough to trip CP_{O1} low. So the next time f_{OSC} starts, the flip-flop does not set. Instead, the logic sets the next one in the chain. This way, the system can skip outputs that do not require energy. But since a slight droop may be too light to replenish, hysteresis in the comparators defines a skipping droop range.

A. Subharmonic Oscillations

Each independent loop regulates peak voltage like peak-current converters regulate peak inductor currents. So when L_O connects to an output longer than 50% of the period t_{OSC}, small variations grow to produce the subharmonic oscillations in Fig. 6. But like in peak-current control, adding a ramp [13] to each threshold v_{RI} that shortens L_O's connection to v_{OI} when responding to loop variations reduces the growth rate of these oscillations. And if the ramp drops at half the falling rate of v_{OI}, which its load i_{LDI} dictates and the maximum load $i_{LDI(MAX)}$ sets to $0.5i_{LDI(MAX)}/C_{OI}$, oscillations disappear for all connecting duty-cycles d_{OI}.

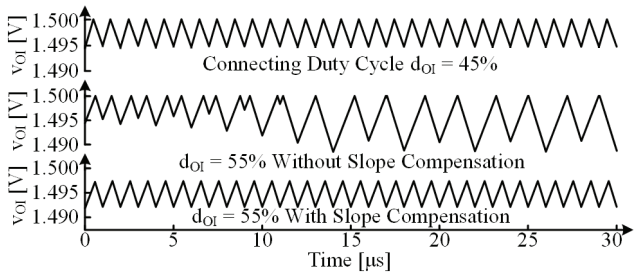

Fig. 6. Simulated response of an independent peak-voltage loop.

B. Loop Gain and Stability

Each CP_{OI}, flip-flop, and M_{OI} combination closes a feedback loop that regulates $v_{OI(PK)}$ to v_{RI}. So variations in v_{OI} prompt CP_{OI} to adjust v_{OI}'s connection time t_{OI} and connecting duty cycle d_{OI}. This, in turn, modifies the current i_{LI} that v_{OI} receives. The small-signal loop gain A_{VLG} is therefore the gain from CP_{OI}'s error $v_{oi(pk)} - v_{ri}$ to $v_{oi(pk)}$ via t_{oi}, d_{oi}, and i_{li}:

$$A_{VLG} = \left(\frac{t_{oi}}{v_{oi(pk)} - v_{ri}}\right)\left(\frac{d_{oi}}{t_{oi}}\right)\left(\frac{i_{li}}{d_{oi}}\right)\left(\frac{v_{oi(pk)}}{i_{li}}\right) = \left(\frac{C_{OI}}{i_L + 0.5i_{LDI(MAX)} - i_{LDI}}\right)\left(\frac{1}{t_{OSC}}\right)(i_L)\left(R_{OI} \parallel \frac{1}{sC_{OI}}\right) \quad (4)$$

v_{OI}'s rising and v_{RI}'s falling ramps dictate how soon CP_{OI} ends t_{OI}. Since v_{RI}'s fall into CP_{OI} reinforces v_{OI}'s rise, t_{oi} is the combined slew-rate translation $C_{OI}/(i_L - i_{LDI} + 0.5i_{LDI(MAX)})$ of the error $v_{oi(pk)} - v_{ri}$. L_O connects a t_{oi}/t_{OSC} fraction of the time d_{oi} to deliver with i_{li} a d_{oi} fraction of L_O's current i_L. This current i_{li} into the combined impedance that v_{OI}'s resistance R_{OI} and C_{OI} establish determines $v_{OI(PK)}$'s variation $v_{oi(pk)}$.

C_{OI} sets the only shunting pole p_{OI} at $1/2\pi R_{OI}C_{OI}$ that attenuates A_{VLG} to unity-gain frequency f_{V0dB}. So the product of A_{VLG}'s low-frequency gain A_{VLG0} and its bandwidth p_{OI} is constant and equivalent to f_{V0dB}:

$$f_{V0dB} = A_{VLG0}p_{OI} = \left(\frac{f_{OSC}}{2\pi}\right)\left[\frac{1}{1 + \left(0.5i_{LDI(MAX)} - i_{LDI}\right)/i_L}\right]. \quad (5)$$

This means A_{VLG} reaches f_{V0dB} with 90° of phase margin. Using the time-domain simulation technique in [15] when i_{LDI} is $i_{LDI(MAX)}$, $i_{LDI(MAX)}$ is 20% of i_L, R_{O1} is 10 kΩ, C_{O1} is 4.7 µF, and t_{OSC} is 1 µs, Fig. 7 shows that A_{VLG0} is 94 dB, f_{V0dB} is 177 kHz, and phase margin is 90°, which matches theory.

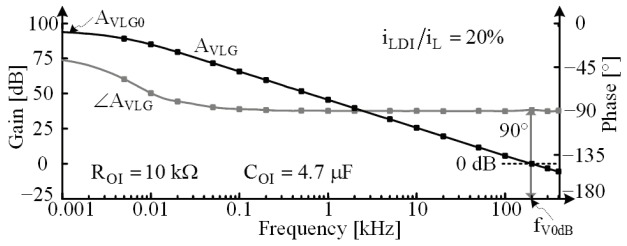

Fig. 7. Simulated small-signal loop gain with slope compensation.

V. Master Voltage Loop

After CP_{ON} senses that L_O satisfies the last independent output v_{ON}, CP_{ON} opens M_{ON} and closes M_{OM} to direct L_O's i_L to v_{OM}. So after L_O supplies all independents outputs, L_O's leftover energy feeds v_{OM}. The error amplifier A_E and oscillating transconductor G_{OSC} close a loop that regulates v_{OM} to v_{RM}. For this, A_E amplifies v_{OM}'s error $v_{OM} - v_{RM}$ to a voltage v_{ERR} that adjusts the level about which G_{OSC} ripples L_O's current i_L. This way, the loop adjusts i_L to a value that is sufficiently high to satisfy all outputs: v_{O1} to v_{ON} and v_{OM}.

A. Equivalent Feedback Loop

For G_{OSC}'s output i_L to behave like a current source within the master loop's bandwidth f_{M0dB}, G_{OSC}'s minimum bandwidth $f_{IBW(MIN)}$ should surpass f_{M0dB}. Irrespective of i_L, however, each independent output sinks a d_{OI} fraction of i_L before connecting L_O to the next output. To v_{OM}, these fractional losses $d_{OI}i_L$ are equivalent to current loads i_{OI}–i_{ON} in Fig. 8. Stated differently, the bandwidths of the independent loops f_{V0dB} are closer to f_{OSC} and therefore higher than f_{M0dB}, so their closed-loop effects on v_{OM} up to f_{M0dB} are like independent load currents.

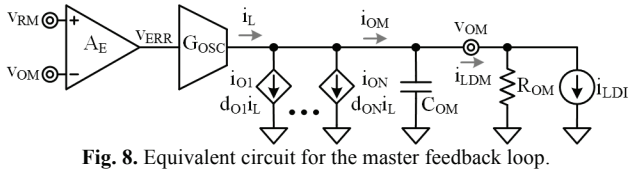

Fig. 8. Equivalent circuit for the master feedback loop.

B. Loop Gain and Stability

Although C_{OM} keeps v_{OM}'s ripple Δv_{OM} low, A_E can amplify Δv_{OM} to an extent that i_L's average can also ripple. But since outputs receive i_L at different times, summing output ripples into A_E, like Fig. 2 illustrates, tends to produce a ripple-free sum. Since independent loops regulate their outputs near their targets, their small-signal errors in A_E are largely absent. A_E therefore senses v_{OM}'s median error to v_{RM}, as Fig. 8 shows.

A_E and G_{OSC} in Fig. 2 close a loop that regulates v_{OM} to v_{RM}. For this, A_E senses and amplifies v_{OM}'s error $v_{OM} - v_{RM}$ to adjust the current i_L that G_{OSC} feeds to all independent outputs and v_{OM}'s load R_{OM} and C_{OM}. The loop gain A_{MLG} is therefore the gain translations across A_E and G_{OSC} to v_{om}:

$$A_{MLG} = A_E\left[\frac{G_{OSC0}}{1 + \left(s/2\pi f_{IBW}\right)}\right]\left(R_{OM} \parallel \frac{1}{sC_{OM}}\right). \quad (6)$$

Since this loop's bandwidth f_{M0dB} should precede $f_{IBW(MIN)}$, C_{OM} should shunt well below f_{IBW} to set a pole p_{OM} at $1/2\pi R_{OM}C_{OM}$ that attenuates A_{MLG} to unity at f_{M0dB}. So the product of A_{MLG}'s low-frequency gain A_{MLG0} and its bandwidth p_{OM} is constant and equal to f_{M0dB}:

$$f_{M0dB} = A_{MLG0}p_{OM} = \frac{A_E}{2\pi R_S C_{OM}}. \quad (7)$$

p_{OM}'s and f_{IBW}'s phase shifts therefore determine the phase margin left PM_M at f_{M0dB} to the 180° inversion point:

$$PM_M = 180 - \mathrm{Tan}^{-1}\left(\frac{f_{M0dB}}{p_{OM}}\right) - \mathrm{Tan}^{-1}\left(\frac{f_{M0dB}}{f_{IBW}}\right). \quad (8)$$

The simulation in Fig. 9 shows that f_{M0dB} is 191 kHz and PM_M is 83° when A_E is 28 V/V; R_S is 5 Ω; R_{OM} is 10 kΩ; C_{O1}, C_{O2}, C_{O3}, C_{O4}, and C_{OM} are 4.7 µF; i_{O1}, i_{O2}, i_{O3}, i_{O4}, and i_{OM} are 50 mA; and t_{OSC} is 1 µs. PM_M nears 90° because the small-signal simulation cannot account for the large-signal delay that wide load dumps produce. f_{IBW} is therefore close to f_{OSC}, near which switching feedback dynamics reduce PM_M to 83°.

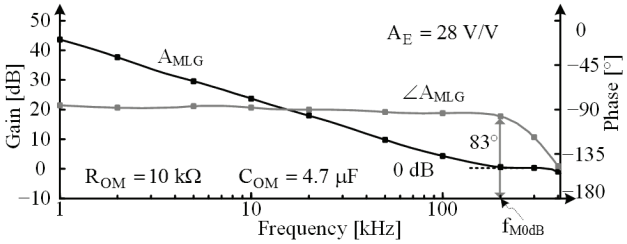

Fig. 9. Simulated small-signal loop gain for a 5-output SIMO.

VI. Large-Signal Response and Validation

For validation, consider a 5-output supply with a 2.7–4.2-V input v_{IN}; 1.00-, 1.25-, 1.50-, 1.75-, and 2.00-V outputs; 100-mA loads; and combined 400-mA load dumps. L_O's drain voltages are therefore v_{O1}'s, v_{O2}'s, v_{O3}'s, v_{O4}'s, and v_{OM}'s 1–2 V. L_O energizes from v_{IN} into these outputs, so L_O's lowest energizing voltages are 0.7–1.7 V. This means, L_O's lowest weighted average voltage $v_{L(MIN)}$ happens when L_O energizes, which from simulations is 0.98 V when evenly loaded.

To keep i_L's ripple at 20% of the highest combined load: at 100 mA, R_S and CP_I's hysteresis in Fig. 2 can be 5 Ω and 500 mV. For i_L to oscillate at 1 MHz when evenly, but half-way loaded and supplied from v_{IN}'s 2.7 V, L_O should be 8.2 µH. This way, 4.7 µF per channel can keep 100-mA loads from rippling outputs more than 20 mV.

The bandwidths of the independent loops f_{V0dB} when evenly loaded are therefore 177 kHz. The oscillating transconductor's minimum bandwidth $f_{IBW(MIN)}$ can be 191 kHz. So to keep the phase margin of the master loop PM_M above 45°, its bandwidth f_{M0dB} should be no greater than 191 kHz, for which A_E can be 28 V/V. This way, i_L can slew up to $1/f_{IBW(MIN)}$ or 5 µs and independent outputs can recover $1/f_{V0dB}$ or 6 µs after that and v_{OM} $1/f_{M0dB}$ or 5 µs after that.

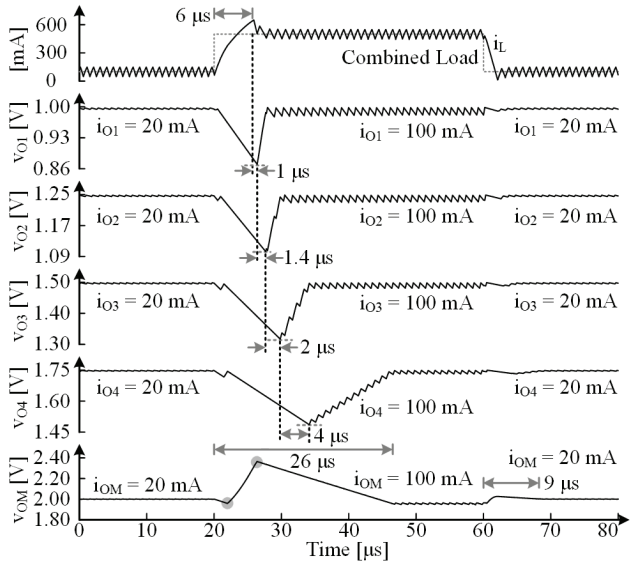

Fig. 10. Simulated 100–500-mA load-dump response of the 5-output SIMO.

To test this, all loads in Fig. 10 rise 80 mA in 10 ns at 20 µs. When reaching v_{OM}, the master loop energizes L_O until i_L slews to a level that can supply and replenish all outputs, so v_{OM} overshoots to 2.40 V. v_{O1}–v_{O4} stop drooping within 4 µs of one another and recover within another 12 µs. v_{OM} under- and overshoots like 45° of phase margin would predict [14].

All transitions are faster for the falling load dump at 60 µs because L_O drains with higher voltages than with which L_O energizes. So i_L requires less time to slew and outputs drift less. All outputs therefore recover within 9 µs without under- or overshooting, as 90° of phase margin would predict [14]. So like theory predicts, i_L slews across $1/f_{IBW}$, independent outputs stop drooping within $1/f_{V0dB}$ of one another, and the last output settles $1/f_{M0dB}$ after the previous outputs recover.

VII. Conlusions

Hysteretic power supplies can recover from load dumps nearly as fast as their inductors can slew their currents, which is as fast as any switched inductor can ever expect to react. Unfortunately, how to design fast and stable hysteretic single-inductor multiple-output (SIMO) supplies is largely unknown and absent in literature. With the theory developed here, however, the 5-output converter designed was stable and able to slew the inductor uninterruptedly to a level that supplied and replenished all 5 outputs. Recovering this quickly is critical because modern state-of-the-art subsystems cannot tolerate the droops that supply lines suffer when disconnected from the shared inductor that feeds them.

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