Abstract—Wireless microsensors add intelligence to otherwise inaccessible locations and large infrastructures, such as tiny crevices in hospitals, factories, and farms. These small devices, however, store little energy, so functionality is low or lifetime is short, or both. Luckily, harnessing ambient energy can replenish these microsystems, and because solar light generates considerably higher power density than motion, temperature, and radiation, photovoltaic (PV) systems are appealing options. Still, chip-sized CMOS PV cells produce only microwatts, and power-conditioning circuits consume some of that, leaving little energy for the sensor system. In view of this constraint, this paper shows that a 0.18-μm CMOS system is 6% more efficient with four stacked 1-mm² PV cells than with one 4-mm² cell. However, stacking P⁺–N Well cells, which is the only stackable PV structure, is 20% less efficient than one cell, so systems that draw power from one N⁺ or N well in substrate cell are better.

Index Terms—Ambient light energy, harvester, CMOS photovoltaic (PV) cells, microsystem, switched-inductor converter.

I. PHOTOVOLTAIC MICROSYSTEMS

Wireless microsensors monitor, process, and transmit data that can improve the performance and energy efficiency of cars, airplanes, trains, hospitals, factories, and others [1]. The tiny batteries these microsystems incorporate, however, cannot sustain monitoring, signal-processing, and telemetric functions for long. Fortunately, light, motion, radiation, and thermal energy in the environment can replenish these otherwise exhaustible reservoirs of energy [2]. And of these, photovoltaic (PV) systems that draw energy from solar light generate the highest power density [3–5]. Still, small surface areas can only capture a small fraction of light.

In fact, PV cells supply only 5% – 20% of the light power \( P_{\text{LIGHT}} \) they receive [5]. And of that, of \( P_{\text{PV}} \), the dc–dc converter that recharges the battery and supplies the system in Fig. 1 consumes another fraction. In other words, \( P_{\text{PV}} \) cells and power-conditioning efficiencies \( \eta_{\text{PV}} \) and \( \eta_{X} \) limit how much output power the system avails to the battery and load:

\[
P_{\text{O}} = P_{\text{PV}} \eta_{X} = P_{\text{LIGHT}} \eta_{\text{PV}} \eta_{X} = P_{\text{LIGHT}} \eta_{\text{SYS}}.
\]

Note the converter uses excess power to recharge the battery, and in cases where load power \( P_{\text{L}} \) surpasses \( P_{\text{O}} \), the battery supplies the difference. Irrespective, though, the system loses power across both the cells and the converter, which is why raising system efficiency \( \eta_{\text{SYS}} \) is so important.

Although PV cells built with custom processes out-power their standard CMOS counterparts [6–9], CMOS cells are inexpensive and, considering they can share the substrate with the integrated circuits (ICs) they support, also compact. Section II of this paper therefore explains how photodiodes in low-cost N-well CMOS process technologies work. Because converter efficiency is also important, Section III explores the effects of PV voltage on conditioning losses. Sections IV and V then describe the impact of stacked cells on leakage losses and system performance and Section VI draws conclusions.

II. CMOS PHOTOVOLTAIC CELLS

Electron and hole concentration differences between butted P- and N-type regions propel holes and electrons to diffuse across the junction. As these carriers deplete their home sites, they leave behind ionized immobile atoms that establish a built-in electric field across the resulting depletion region, as Fig. 2a exemplifies. This field attracts charge carriers back to their home sites to result in no current flow.

Incident light on the semiconductor, however, excites loosely bound outer shell (valence) electrons to the extent they break away from their parent atoms to generate electron–hole pairs (EHPs). As light penetrates, the semiconductor absorbs some of the passing photons, so as Fig. 2b shows, EHP concentration \( N_{\text{EHP}} \) is exponentially lower with higher absorption coefficients \( A_{\lambda} \) and at deeper levels \( d_{\lambda} \).
Interestingly, absorption is higher for shorter wavelengths \[\text{[10]}\].

Once free, EHPs diffuse in all directions and, barring other factors, eventually recombine. EHPs generated within electron and hole diffusion lengths \(L_E\) and \(L_H\) of the depletion region and in the region, however, do not have enough time to recombine before the region's built-in electric field \(\varepsilon_{PN}\) sweeps them across. The result is that \(\varepsilon_{PN}\) carries electrons in the depletion region to the N-type side and holes to the P side, as Fig. 2a shows, establishing a photonic current \(i_{PH}\) whose current density \(J_{PH}\) rises with \(L_E, L_H,\) and depletion width \(W_D\):

\[
J_{PH} \propto L_E + L_H + W_D. \tag{3}
\]

Higher donor and acceptor doping concentrations in the N- and P-type regions, however, shorten \(L_H\) and \(L_E\). Metallic contacts also obstruct light, so they limit the number of photons that produce EHPs. Plus, surface irregularities can trap charges long enough for them to recombine.

All this means that all junction diodes work as PV cells when exposed to light. In a low-cost N-well CMOS process, for example, the N\(^+\), P\(^+\), and N-well regions used to build MOSFETs in a P substrate can also fashion N\(^+\) in substrate, N well in substrate, and P\(^+\) in N well PV cells. Diffusion depths, doping concentrations, and parasitic junctions, however, differ, so performance also differs.

\(A.\) N\(^+\) in P Substrate PV Cells

The built-in potential across the N\(^+\) in P substrate diode of Fig. 2a sweeps EHPs in the depletion region and holes and electrons that reach this space to produce the photon current \(i_{PH}\) that Fig. 3 models. Because the N\(^+\) region is at the surface and shallow, EHP concentration is high. High donor doping concentration, however, limits hole-diffusion length \(L_H\), so a fraction of the holes generated in the N\(^+\) region reach the depletion space. Because EHPs fall exponentially from the surface, few electrons deeper in the substrate contribute to \(i_{PH}\).

Accumulation of electrons in the N\(^+\) region and holes in the substrate that do not traverse the depletion space establish a voltage \(v_{PV}\) across the junction. This 0.3 to 0.5 V forward-biases the diode \(D_{PV}\) that the junction implements, so \(i_{PH}\) loses current \(i_D\) to \(D_{PV}\) and the cell outputs \(i_{PH} - i_D\). Plus, series resistances in the cell \(R_S\) drop voltage and dissipate power.

\(B.\) N well in P Substrate PV Cells

The N well in Fig. 4 can replace the N\(^+\) in Fig. 2a. Here, lower concentration in the N region extends hole diffusion length \(L_H\) to counter the lower EHP concentration of a deeper junction. Surface recombination, however, ultimately limits \(L_H\) to a fraction of the well's depth. Still, charge collection and model are similar to those of its N\(^+\) counterpart \[11\].

\(C.\) P\(^+\) in N Well PV Cells

P\(^+\) diffusion in an N well in Fig. 5 also collects electrons and holes that reach the depletion region and EHPs generated there to produce photon current \(i_{PH}\). P\(^+\) depth and doping levels mirror those of N\(^+\), so \(i_{PH}\) can be similar to that of N\(^+\). Note, however, the deeper well–substrate junction also collects carriers. The problem here is the resulting current \(i_S\) steals and dumps carriers from the main junction to substrate.

\(III.\) CONVERTER'S POWER-TRANSFER EFFICIENCY

The system not only loses light energy in the PV cells but also in the circuit that transfers power from the cells to the load and battery. In fact, DC–DC converters consume Ohmic, quiescent, and often times, gate-drive power. Of these, Ohmic losses in switched circuits drop more quickly with input power than in linear circuits, and switched inductors normally
employ less switches than switched capacitors, so switched inductors lose less Ohmic and gate-drive losses when transferring microwatts [3]. One challenge with switching converters, however, is the ripple voltage they induce across the cells. This can be a problem because PV voltage \( v_PV \) forward-biases diodes and BJTs that steer current away from the output, so output power peaks at an optimal value of \( v_{PV} \) and deviations from it amount to additional losses.

### A. Switched-inductor Converters

DC–DC switchers like the booster of Fig. 7a energize and drain an inductor \( L_X \) from the input \( v_{IN} \) (with \( M_X \)) to the output \( v_O \) (with \( M_E \)) in alternating phases across a switching period \( t_{SW} \). Because \( v_{IN} \) and \( v_O \) change little over \( t_{SW} \), constant voltages across \( L_X \) raise and lower \( L_X \)'s current \( i_L \) in Fig. 7 seriously when energized and drained across \( t_{E} \) and \( t_{D} \). For \( L_X \) to conduct continuously across \( t_{SW} \) when input current is low, ripples in \( i_L \) must be small and frequent. Switching the network more frequently, however, raises gate-drive power losses. This means sending larger, but less frequent ripples (packets) discontinuously is ultimately more power efficient.

#### Fig. 7. (a) Switched-inductor booster and (b) its inductor current across time.

Larger \( i_L \) ripples, however, raise \( v_{IN} \)'s ripple, which shift the PV cells away from their maximum power point. The purpose of input capacitor \( C_{IN} \) in Fig. 7a is to keep \( v_{IN} \)'s ripple low by supplying and sinking what the circuits should not. A higher \( L_X \) would also reduce ripples in \( i_L \), except chip-size inductors with higher inductances have higher power-consuming resistances \( R_{L,ESR} \). Needless to say, balancing power losses in the converter is of paramount importance.

### B. Packet Losses

Since \( i_L \) flows through \( M_N \), \( M_P \), and \( R_{L,ESR} \), together they introduce an equivalent resistance \( R_{EQ} \) whose power \( P_R \) rises quadratically with \( L_X \)'s RMS current \( i_{L,RMS} \):

\[
P_R = R_{EQ} \cdot i_{L,RMS}^2 = R_{EQ} \left( \frac{i_{L,PK}}{\sqrt{3}} \right)^2 \cdot \frac{t_C}{t_{SW}} = E_R \cdot f_{SW}.
\]

Here, the RMS current of \( i_L \)'s triangle across conduction time \( t_C \) is \( i_{L,PK}/\sqrt{3} \) [12] and \( i_{L,RMS} \) across \( t_{SW} \) is \( t_C/t_{SW} \) times that. Every time the converter transitions, capacitances \( C_{EQ} \) in the switches (\( M_N \) and \( M_E \)) also draw gate-drive charge \( Q_{GD} \) and energy \( E_{GD} \) from the battery \( V_{BAT} \) across every period \( t_{SW} \):

\[
P_{GD} = E_{GD} = \left( Q_{GD} \cdot V_{BAT} \right) f_{SW} = C_{EQ} \cdot V_{BAT}^2 \cdot f_{SW},
\]

where \( Q_{GD} \) is \( C_{EQ} \cdot V_{BAT} \). Similarly, because portions of the controller operate and dissipate power only across \( t_C \), controller losses \( P_C \) rise with \( t_C \) and frequency \( f_{SW} \):

\[
P_C = P_Q + P_D \left( \frac{t_C}{t_{SW}} \right) = P_Q + E_D f_{SW},
\]

where \( P_Q \) is the quiescent, time-independent portion of \( P_C \) and \( P_D \) the duty-cycled counterpart.

### C. Packet Size Optimization

\( i_L \)'s peak \( i_{L,PK} \) and \( L_X \)'s conduction time \( t_C \) set how much energy per period \( L_X \) draws from \( v_{PV} \) and \( f_{SW} \) sets how frequent. In terms of losses, each energy packet \( L_X \) transfers dissipates Ohmic, gate-drive, and controller energy \( E_R \), \( E_{GD} \), and \( E_C \). So, optimizing the converter to dissipate the least energy across one packet and sending several of those packets is as efficient as sending one. This means that fixing \( i_{L,PK} \) and \( t_C \), optimally sizing \( M_N \) and \( M_P \) to deliver one packet, and adjusting \( f_{SW} \) to track PV power \( P_{PV} \) yields nearly constant conversion efficiency \( \eta_X \) across \( P_{PV} \), as Fig. 8 demonstrates.

#### Fig. 8. Simulated efficiency and losses across \( P_{PV} \) and number of PV cells.

In contrast, fixing \( f_{SW} \) fixes \( E_{GD} \) and \( E_C \) and adjusting \( i_{L,PK} \) and \( t_C \) to track \( P_{PV} \) changes and unbalances \( E_R \) with respect to \( E_{GD} \) and \( E_C \). As a result, the optimal dimensions of \( M_N \) and \( M_P \) that keep losses at a minimum change with \( P_{PV} \), which is a less appealing design choice. Instead, with one \( i_{L,PK} \) and \( t_C \) setting, adjusting \( f_{SW} \) tracks \( P_{PV} \), so all \( P_R \), \( P_{GD} \), and \( P_C \) rise and track across most of \( P_{PV} \)'s range in Fig. 8. \( P_C \)'s quiescent component \( P_Q \), however, does not change with \( f_{SW} \), so \( P_Q \) dominates when \( P_{PV} \) is low and \( \eta_X \) drops accordingly in that region.

### D. Photovoltaic Voltage Optimization

Another parameter to consider is how many PV cells to derive from a given chip area \( A_{TOT} \). While one large cell generates \( J_{PHATOT} \) of current, \( N_{PV} \) smaller cells generate \( J_{PHATOT}/N_{PV} \), so multiple cells in series generate less current at a higher voltage than one cell outputs. For a fixed \( i_{L,PK} \) and \( t_C \), a lower average inductor current \( i_{L,AVG} \) means lower \( f_{SW} \) and, as a result, converter losses are lower. In other words, losses drop with more cells, which is why conversion efficiency \( \eta_X \) in the 0.18-\( \mu \)m CMOS system of Fig. 8, which uses a 47-\( \mu \)H, 5.6-\( \Omega \) inductor, is 6% higher for four stacked 1-mm\(^2\) cells than with one 4-mm\(^2\) cell.

### IV. STACKED PV CELLS

Of possible N-well CMOS PV cells, N\(^+\) and N well in P substrate variations cannot disconnect from the substrate, so they have no isolated terminals with which to stack. The P\(^+\) in N well cell is the only one that can stack. Unfortunately, however, each cell in the stack leaks substrate and BJT currents whose losses reduce the gains that using multiple cells to drive a switched-inductor converter produces.
A. Design

Since PV cells are essentially current sources, the chief design challenge with connecting PV cells in series is managing current mismatches. The problem is that substrate and BJT currents between cells leak currents. In a stack like Fig. 9 shows, for example, the BJT current of the first cell $i_{E1}$ and the substrate current of the second $i_{S2}$ steal current from the first cell. So, to match currents, the photon current of the second $i_{PH2}$ should be lower than that of the first $i_{PH1}$. Similarly, subsequent photon currents should be smaller than those of their preceding stages, so cell areas should be progressively smaller from the bottom to the top of the stack.

![Electrical model of three P+ in N well CMOS PV cells stacked.](image)

Still, imperfections across the die produce mismatches that are difficult to manage with cell area. Connecting dc–dc converters across each cell that ensure each cell voltage is optimum is one way of absorbing mismatches [13], except each converter dissipates power and requires space. The resistors in Fig. 9 can also absorb current differences, especially in tiny platforms where nearby cells match better. The tradeoff is the test time required to trim these resistors.

![Power losses across the number of cells stacked and wavelengths.](image)

B. Stack Losses

Since absorption for higher wavelengths $\lambda_{\text{LIGHT}}$ is lower, substrate currents and related losses usually overwhelm those of the BJT currents above roughly 490 nm [9–10]. This means $i_S$ normally causes most cell-stack losses. So, since the voltage at each intermediate connection (in Fig. 9) is the lower cell’s emitter voltage $v_{E1}$, which corresponds to the number of PV voltages the lower cells produce, $P_{\text{LOSS}}$ reduces to roughly

$$P_{\text{LOSS}} = \sum i_{S(i)} v_{E(i)} = \sum i_{S(i)} (1 - 1) v_{PV},$$

where each junction loses power. This means $P_{\text{LOSS}}$ rises with the number of cells in the stack, as Fig. 10 shows when total chip area is 4 mm² and collectable power $P_{PH}$ is 54 µW.

V. OVERALL ENERGY-HARVESTING EFFICIENCY

Recall from Fig. 8 that Fig. 7a’s converter has 6% higher conversion efficiency $\eta_X$ when supplying a 1.8-V load with power from four stacked 1-mm² 0.4-V cells than from one 4-mm² cell. Unfortunately, substrate losses cause PV collection efficiency $\eta_{PV}$ for Fig. 9’s cell stack when subjected to 450-nm light to fall 20% below their one-cell counterpart. In other words, substrate losses in stacked cells negate converter gains in efficiency. This means one cell is better, and because N⁺ and N wells in P substrates do not leak substrate or BJT currents, $P^+$ diffusion in an N well cells are less optimal.

VI. CONCLUSIONS

This paper shows that the efficiency of a 0.18-µm CMOS PV system with one 0.4-V 4-mm² cell is 16% higher than with four stacked 1-mm² cells. This is because, although stacking four cells raises converter efficiency by 6%, substrate losses reduce PV collection efficiency by 20%. Plus, of the three possible junctions that can collect carriers in an N-well CMOS process, $P^+$ in an N well is the only one that leaks. The problem with leaking substrate currents is that absorption of light with wavelengths above 490 nm is low, so the parasitic N well in P substrate junction steals appreciable carriers from the isolated cell. This means single N⁺ and N well in substrate cells are optimal.

REFERENCES