A Continuous, Low-Glitch, Low-Offset, Programmable Gain and Bandwidth G_M–C Filter

H. Pooya Forghani-zadeh, *Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Senior Member, IEEE*
Georgia Tech Analog and Power IC Design Lab

***Abstract*- A programmable gain and bandwidth first-order low-pass Gm-C filter is proposed, designed, and simulated. Continuous low-offset operation is achieved by combining the continuity and low offset features of the ping-pong and auto-zeroing schemes. In the proposed strategy, clock feedthrough and charge injection are also reduced by decoupling the holding capacitor from the ac-signal path and increasing its value without affecting filter response. The ping-pong operation is designed to occur on the dominant pole-setting node, where a large capacitor resides, thereby also attenuating the glitches normally associated with "hand-over" events. The gain and bandwidth are programmed by adjusting the transconductance and loading resistance of the filter, achieving gain and bandwidth ranges and resolutions of 2 – 40 V/V, 75 mV/V, 1 – 5 KHz, and 32 Hz, respectively. Worst-case Monte Carlo simulations of the proposed 0.5 µm CMOS IC resulted in an input-referred offset of less than 0.5 mV and hand-over glitches below 5 mV.**

Keywords: Gm-C, programmable, low-offset, auto-zeroing, ping pong, current-sensing.

I. INTRODUCTION

Low-offset operation of filters can be as important as their high frequency response, as is the case for measurement and instrumentation applications, where the DC portion of the signal contains important information. When sub-1mV input-referred offsets are required, such as in sensor applications, increasing the dimensions of critically matched CMOS transistors is not practical and dynamic offset-cancellation circuit techniques are therefore necessary. Additionally, if the circuit is analog and continuous, low-offset operation must also remain continuous, negating the attributes of simple auto-zeroing schemes. Although appearance of spikes and glitches are inherent in dynamic offset-cancellation circuits because of their switching nature, glitches more than a few milli-volts cannot be tolerated in some high performance applications because of noise sensitivity. For example, if undesired glitches appear at the input of a high-speed, high-resolution comparator, they trigger unwanted transitions, which adversely affect system performance parameters like noise and jitter. Tuning the gain and bandwidth of analog filters is also increasingly important in a wide range of applications, such as radio-frequency (RF) filters in receivers, where the filter bandwidth must match the received signal frequency to discern the signal from the noise present.

The filter proposed in this paper is designed to meet the low-glitch, continuous low-offset operation requirements of a current-sensing filter for dc-dc converters [1]. Programming the gain and bandwidth of the filter is necessary for accuracy. While the filter bandwidth is only a few kilo-Hertz, its single pole response extends through several decades of frequency and parasitic poles must therefore lie well above the operating frequencies of the system, which can easily exceed 10 MHz. High linearity and rail-to-rail input common-mode range (ICMR) are also required to prevent distortion at the output. Currently, state-of-the-art solutions for current-sensing filters in DC-DC converter applications are discrete, where the filter gain and bandwidth are adjusted manually through off-chip resistors and capacitors [1-2].

II. SYSTEM DESIGN

A. Programmability

A system-level schematic of the proposed monolithic Gm-C filter is shown in Fig. 1. The underlying scheme of the proposed circuit is to use a variable-gain transconductor g_m, a filter capacitor C, and a variable resistor R to set the bandwidth and gain in two separate phases, by adjusting g_m first and then R. This tuning and calibration process only takes place during start-up, power-on-reset, and/or time-out events, digitally storing the programmed values for normal operating conditions.

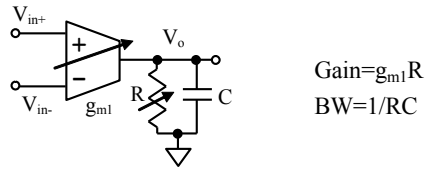

Fig. 1. First-order low-pass Gm-C filter block diagram.

B. Low offset

Dynamic offset cancellation techniques normally fall in two categories, auto-zeroing or chopper-stabilized, which are based on sampling and modulation principles, respectively [3]. In basic form, the auto-zeroing scheme only processes the input signal half of the time and is therefore not continuous. Chopper-stabilized techniques, on the other hand, are continuous, but also band-limited, since the frequency of the input signal must be less than half the chopping frequency (to prevent aliasing) [3]. What is more, the chopping frequency cannot exceed several tens of kilo Hertz because of switch charge injection non idealities, limiting them to low bandwidth applications. However, combining the attributes of auto-zeroing with ping-pong constitute a viable solution for continuous low-offset operation with minimal constraints on signal bandwidth [3-5]. For instance, as shown in Fig. 2, two identical units are used in parallel and, while one is in the signal path, the other is offset canceling, and the two subsequently swap positions periodically.

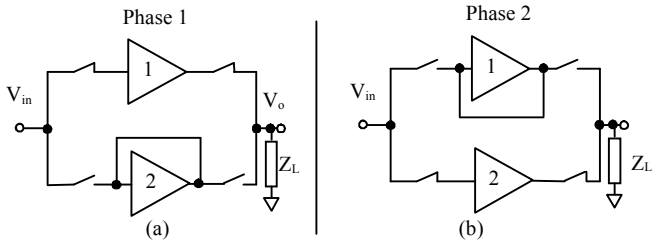

Fig. 2. Basic ping-pong operation.

Fig. 3 illustrates the proposed ping-pong offset cancellation scheme, as applied to the Gm-C filter shown in Fig. 1, which uses two identical (i.e., well matched) transconductors g_{m11} and g_{m12} and non-overlapping clocks (to prevent cross wiring). While one transconductor processes the input signal (e.g., for φ_1 equal to ''1'' and φ_2 ''0'', g_{m11}), the other one auto-zeroes (e.g., g_{m12}) by closing the unity-gain loop through auxiliary summing differential inputs a+ and a- and short-circuiting the main inverting and non-inverting terminals. The measured offset is then stored across the

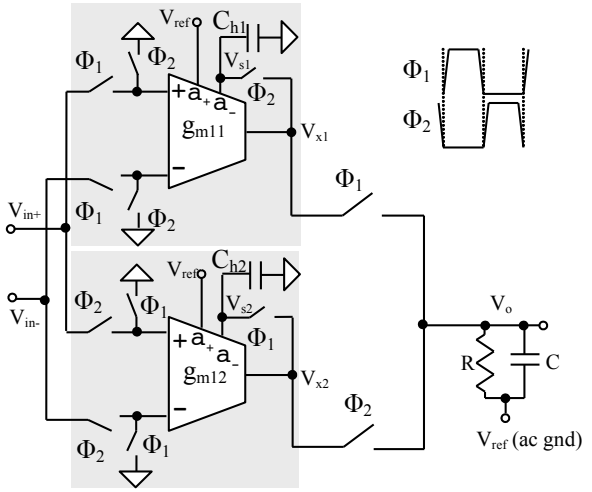

Fig. 3. Schematic of the proposed ping-pong based, offset-cancelled Gm-C filter.

holding capacitor connected to port a- and the input signal is connected to the main input terminals.

Storing the offset voltage in ac-insensitive nodes, in other words, in remote nodes that do not process the input signal, affords the designer some luxuries. The size of the holding capacitor, for instance, can be increased without affecting the frequency response of the Gm-C filter. In this way, clock feedthrough and charge injection are reduced and offset cancellation performance is therefore improved.

The basic idea in auto-zeroing is to measure the offset in one phase and subtract it from the forward path in the other, and measuring the offset is achieved by disconnecting the amplifier from the output and configuring it for unity gain [3]. In the proposed circuit, a summing transconductor is used to decouple the signal path from the offset holding capacitor (Fig. 4). Since the output current is the sum of the transconductances of two input pairs, if one pair is short-circuited and the other used in unity-gain (Fig. 5(a)) with reference V_{ref}, the output voltage is the sum of the combined cumulative offset of the circuit and V_{ref},

$$V_s = \left[\frac{(V_{ref}g_{ma} + V_{os1}g_{m1} + V_{os2}g_{ma})R_o}{1+g_{ma}R_o}\right] + V_{INJ\text{-}err} \approx V_{ref} + V_{os2} + V_{os1}\frac{g_{m1}}{g_{ma}} + V_{INJ\text{-}err}, \quad (1)$$

where V_s is the offset voltage stored in holding capacitor C_h, g_{m1} and g_{ma} are the transconductance values of the main and auxiliary pairs, V_{os1} and V_{os2} are the input-referred offsets of the main and auxiliary ports, $V_{INJ\text{-}err}$ is clock feedthrough and charge injection errors introduced via switch S_1, and $g_{ma}R_o$ is the loop gain, which is significantly higher than 1 because R_o is the output resistance of cascoded current sources and current mirrors.

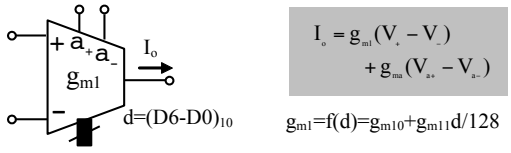

Fig. 4. g_{m1} top-level block diagram.

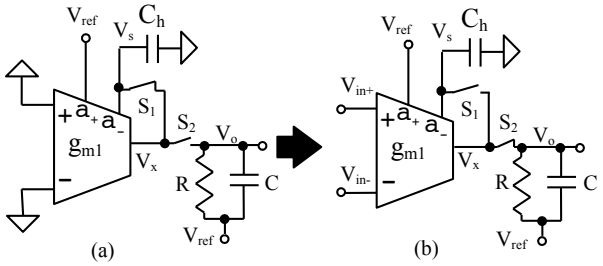

Fig. 5. Offset cancellation: (a) offset storage and (b) normal operation.

During the other phase, when the transconductor is processing input signals, the offset is subtracted from the signal path by reconfiguring the summing transconductor as shown in Fig. 5(b), where the stored offset voltage is applied to the inverting terminal of the auxiliary pair. The output voltage during this phase is

$$V_o = \left[(V_{in} + V_{os1})g_{m1} + (V_{ref} - V_s + V_{os2})g_{ma}\right](R_o \| R) \approx \left[V_{in}g_{m1} + V_{os1}g_{m1} + V_{ref}g_{ma} + V_{os2}g_{ma} - \left(V_{ref} + V_{os2} + V_{os1}\frac{g_{m1}}{g_{ma}} + V_{INJ\text{-}err}\right)g_{ma}\right](R_o \| R) = (V_{in}g_{m1} + V_{INJ\text{-}err}g_{ma})(R_o \| R). \quad (2)$$

The accuracy of the foregoing technique is therefore only limited by charge injection and clock feedthrough errors ($V_{INJ\text{-}err}$) since $R \ll R_o$, as is the case in all of auto-zeroing schemes [3]. Unlike other schemes, however, increasing the holding capacitor's value, which reduces these errors, is acceptable because the signal path's bandwidth is unaffected.

In ping-pong schemes, hand-over glitches result when the units are swapped, since the output voltage of one device is not necessarily equal to the other. In the proposed circuit, the filter's dominant low-frequency pole (1/RC) is placed outside the switching network, thereby attenuating these glitches. The resulting spike is therefore the result of charge distribution between the large filter capacitor C and transconductor's parasitic output capacitor C_{par} (Fig. 6),

$$V_{glitch} = \left(\frac{C_{par}}{C + C_{par}}\right)\Delta V, \quad (3)$$

where ΔV is the voltage difference between the offset-cancelled unit and the output voltage of the processing unit just before the hand-over event. For a filter capacitor C of 60pF, 0.6pF of C_{par}, and 0.5 V of ΔV, the glitches are limited to 5 mV.

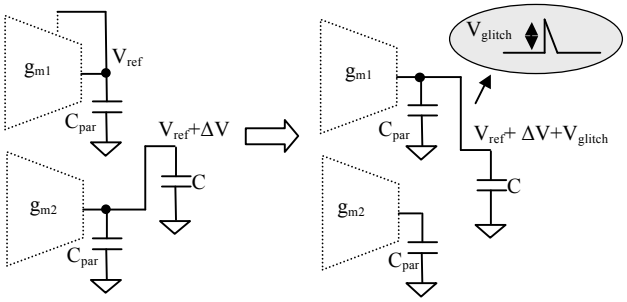

Fig. 6. Hand-over ping-pong glitch mechanism.

IV. CIRCUIT DESIGN

A. Transconductor

High linearity, rail-to-rail input common-mode range (ICMR), programmability, high output resistance, and an auxiliary transconductance path for offset cancellation are the key design parameters of the transconductor. The topology proposed is derived from a second-generation current conveyor (CCII) [6],

where a resistor (R_1) is connected in series with the inverting input of a unity-gain amplifier (Fig. 7). Shunt feedback ensures that the impedance at node 2 is low [7-8] and the input voltage across resistor R_1 (differential input voltage across the transconductor) therefore causes current I_{R1} to flow into node 2,

$$I_{R1}=(V_+-V_-)/R_1. \quad (4)$$

This current and I_b are summed and mirrored by M1-M2, which subtracts it from another I_b, resulting in a bi-directional output current whose magnitude is linearly proportional to the differential input voltage and inversely proportional to R_1.

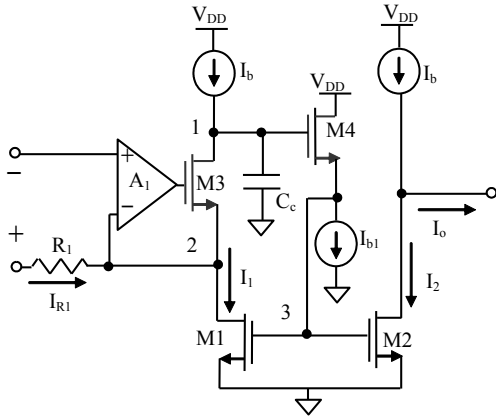

Fig. 7. Basic topology of the proposed transconductor.

The feedback loop around device M1 (M1, common-gate M3, and source-follower M4) is used to bias and decouple the gates of current mirror M1-M2 from node 2, which partially defines the ICMR of the transconductor. Capacitor C_c sets the dominant pole frequency of that loop. In closed loop, the mirror adds a high frequency parasitic pole to the filter, at its unity-gain frequency (gain-bandwidth product) – g_{M1}/C_c, where g_{M1} is the transconductance of M1. Amplifier A_1 is a standard PMOS input, two-stage, Miller-compensated amplifier with a gain-bandwidth product of 10 MHz.

The programmability feature is added by digitally controlling the gain of the current-mirror (Fig. 8), and more specifically, by programming the connectivity of a binarily weighted array of current mirrors (Fig. 9(a)). For example, if bit D_i is low, the gate of cascode transistor N_i is connected to ground and the i^{th} mirror is disabled; otherwise, it is connected to a bias voltage and therefore enabled. Since the mirror amplifies both I_{R1} and DC bias current I_b, an equally gained DC bias current is sourced to the output, resulting in a net DC and ac bidirectional current gain of K and therefore a net transconductance of

$$g_{m1}=K/R_1. \quad (5)$$

Cascoding transistors are added to the current mirrors and sources to increase the output resistance of the transconductor.

The auxiliary transconductance input path (g_{ma}) used for offset cancellation is realized by summing a voltage-controlled current source to the output of the aforementioned circuit, as shown in Fig. 8. For functional efficiency, the bias current generator and this auxiliary path are combined into a single circuit (Fig. 9(b)). Transistor pairs Pa-P1 and Pb-P2 form current sources. Current-canceling differential pair N_a-N_d is used to generate low transconductance values [9]. The resulting transconductance of the auxiliary path is

$$g_{ma}=Kg_{mad}, \quad (6)$$

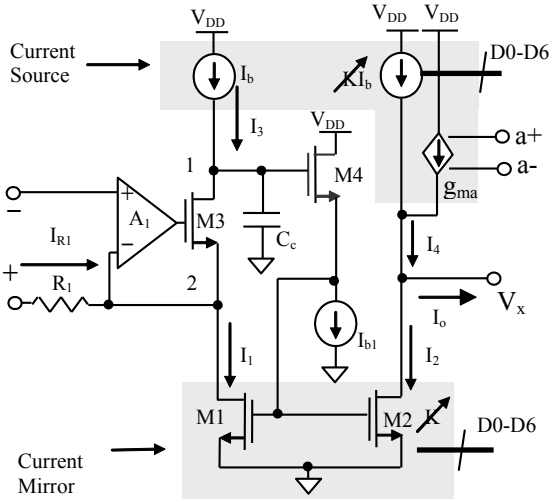

Fig. 8. Proposed programmable transconductor and its auxiliary input pair.

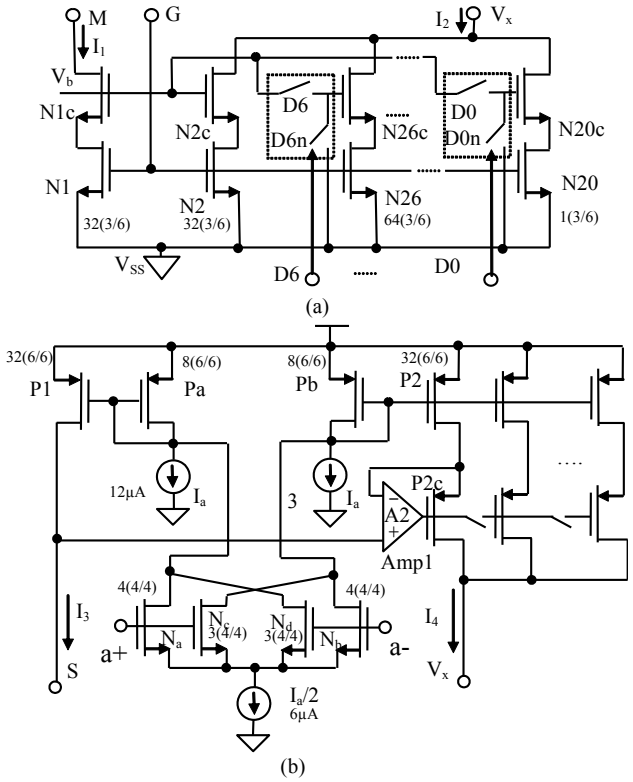

Fig. 9. Implementation of (a) the current mirror and (b) auxiliary transconductor g_{ma}.

where g_{mad} is the transconductance of the composite differential pair N_a, N_b, N_c, and N_d. Amplifier A_2, which is a conventional single-stage amplifier, forces the drain voltages of transistors P1 and P2 to be equal, thereby mitigating channel-length modulation effects and improving accuracy performance.

B. Programmable Resistor

The bandwidth of the Gm-C filter is tuned via a high-resistivity (1 KΩ/□) poly resistor (R in Figs. 1 and 3), which is, again, realized by digitally re-arranging the connectivity of a binary weighted resistor array (Fig. 10). Switches D0-D7 are NMOS transistors with aspect ratios 20 times larger than the minimum size allowed to ensure their respective switch-on resistances are low enough not to affect the resolution of the array. It is noted that this scheme is not applied to R_1 in the transconductor circuit (Fig.

7) because the parasitic capacitors of the switches degrade the overall frequency response of the filter. These parasitic capacitors, on the other hand, have negligible effects when applied to R because the dominant low frequency capacitor C also resides on that node, in parallel with R.

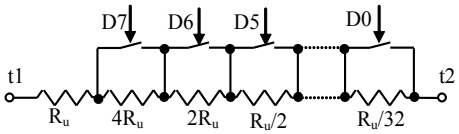

Fig. 10. Tunable, bandwidth-setting resistor R.

IV. SIMULATION RESULTS

Worst-case Monte Carlo simulations with fast and slow MOSFET models and ±20% tolerances for capacitors, resistors, and bias currents across a military temperature range (-40 – 125 °C) and through the voltage lifespan of a Li-Ion battery (2.7 – 4.2 V) verified the performance of the proposed circuit, whose summary is shown in Tables 1 and 2. Special attention was dedicated to the offset-cancellation capabilities of the circuit and its process-dependent performance. The dominant source of offset error, before subjecting the circuit to offset cancellation, is the mismatch performance of the current mirrors in the transconductor circuit. Fig. 11(a) shows the worst-case corner simulation results for a 5% mismatch in the current mirrors for a filter gain (i.e., $g_{m1}R$) of 10, where 70 to 150 mV of offset was measured in the first phase and cancelled to within 5 mV at the output in the second (i.e., 0.5mV input-referred offset).

Table 1. Critical design parameters.

R_1 in g_m	250KΩ	**R No. bits**	8
Mirror Ratio in g_m	1-5	**C**	60 pF
No. of Bits for Mirror	7	**C_{h1}, C_{h2}**	6 pF
R	325-2900 KΩ	**Clock freq.**	1 KHz

Table 2. Summary of simulated circuit performance.

Technology	0.5 µm CMOS
Supply Voltage	2.7 to 4.2 V (Li-Ion)
Temperature range	-40 to 125 °C
Switching (V_{in+}) ICMR	0 to V_{DD} (rail to rail)
Non-switching (V_a) ICMR	0.8V to V_{DD}-1V (Nom: 1.5V)
Input-referred offset	< 0.5 mV
Nonlinearity ($\Delta g_{m1}/g_{m1}$)	< -67 dB (w/ rail-to-rail input signal)
BW programmability	1 to 5 KHz in 30 Hz steps
Gain programmability (V_o/V_{in})	2.5 to 40 V/V in 75 mV/V steps

Fig. 11(b) shows the output voltage during a "hand-over" event for a pulse input voltage. The worst-case hand-over glitch occurs when the difference of output voltage (V_o) from offset cancellation desired output (V_{ref}) is maximum. This maximum difference is 0.5V in the proposed application (i.e., V_o is 0.85V and V_{ref} is 1.35V), which results in a glitch of less than 5 mV, as predicted by Eq. 3.

V. CONCLUSIONS

A continuous low-offset programmable gain and bandwidth first-order g_m-C filter has been proposed, designed, and simulated. Worst-case Monte Carlo Spectre simulations show less than 0.5 mV of input-referred offset and less than 5 mV of hand-over glitches. The offset-cancellation scheme implemented combined the continuity and low offset features of the ping-pong and auto-zeroing schemes, respectively.

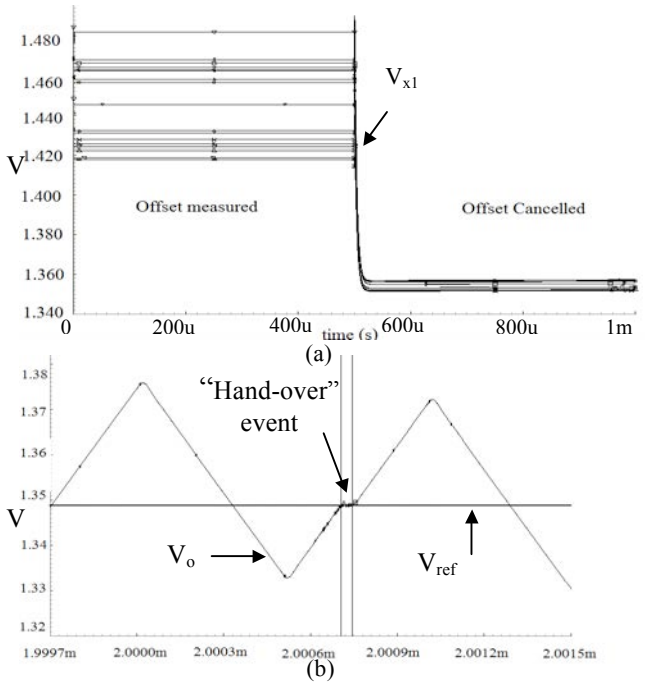

Fig. 11. (a) Single cycle, offset-cancellation functionality and (b) hand-over glitch performance of the proposed circuit.

In the proposed circuit, clock feedthrough and charge injection are reduced by decoupling the holding capacitor from the ac-signal path with a summing transconductor, thereby affording the luxury of increasing the holding capacitance and therefore decreasing charge injection and clock feedthrough without affecting filter response. "Hand-over" glitches are also reduced because the ping-pong operation occurs on the dominant pole-setting node, where a large capacitor resides. The gain and bandwidth are digitally programmable by adjusting the transconductance of the circuit and its loading resistor, respectively, achieving 75 mV/V and 30 Hz of resolution. The proposed circuit technique is suitable for many applications like instrumentation and measurement devices, where the accuracy of both DC and high frequency ac information are critical.

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