PREDICTING THE EFFECTS OF ERROR SOURCES IN BANDGAP REFERENCE CIRCUITS AND EVALUATING THEIR DESIGN IMPLICATIONS

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ABSTRACT

Errors that arise from tolerance variations and mismatches between devices severely degrade the performance of bandgap reference circuits, which are essential building blocks to all high-performance systems. All these error sources have been analyzed (and verified through SPICE) and their design implications have been addressed. It has been found that resistor tolerance and current-mirror mismatch are the dominant sources of error in bandgap reference-type circuits. Further, it has been found that resistor mismatch, transistor mismatch, and current-mirror mismatch errors have a PTAT variation, while resistor tolerance error has a CTAT dependence – both PTAT and CTAT errors are eliminated by trimming the PTAT terminating resistor in a bandgap circuit, only at room temperature. Resistor TC errors cannot be trimmed out and hence resistors must therefore be carefully selected and designed.

1. INTRODUCTION

The study of the sources of error in reference circuits is extremely important in an environment in which shrinking voltages impose severe performance specifications on accuracy. Their relative impact on the reference voltage is particularly important in the design phase. Bandgap reference circuits, which play a pivotal role in most of today's high-performance wireless and portable systems, must therefore carefully cater to these errors.

A number of factors give rise to errors in the voltage produced by the bandgap reference. This work presents analytical expressions for the effects of these errors on the bandgap voltage, and an evaluation of their implications on bandgap reference design. The analysis presented is applicable to any bandgap circuit; however, for purposes of clarity and convenience, it is applied to a sample circuit topology, based on the bandgap's basic building block (described in Section 2). Section 3 presents the analysis of the various error sources – resistor mismatch, resistor tolerance, resistor's temperature drift, transistor mismatch, and current-mirror mismatch. A discussion on the analyses is presented in Section 4, with the conclusions in Section 5. The Appendix contains the derivations of the analytical expressions introduced in Section 3.

2. BASIC CELL

The basic topology of the circuit used for analysis is shown in Figure 1. This is the building block for most bandgap reference circuits [1]-[8], and the expressions for the resulting error sources of this circuit can easily be applied to most practical implementations.

The detailed circuit is shown in Fig. 2. The circuit uses the Brokaw topology [3]. M_{P1}, M_{P2} and M_{P3} comprise a current mirror. M_{P4} is a start-up device; it draws current from the low-impedance node when the circuit is in the "off" state, thus pulling current into M_{P3} and starting up the circuit. The difference of the base-emitter voltages of transistors Q_1 and Q_2, when applied to the resistor R, produces a Proportional To Absolute Temperature (PTAT) current and, consequently, a PTAT voltage across R_{PTAT}. This voltage, having a positive temperature coefficient, is then added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. Transistor Q_3 helps to eliminate current mismatches resulting from Early-voltage effects [3].

The resistor-capacitor network consisting of R_D and C_D damps the positive feedback gain that occurs in the loop consisting of the base-collector of Q_3 and the gate-drain of M_{P2}. Capacitor C_{S1}, along with the input impedance seen at the base of Q_3, determines the dominant pole of the circuit. Capacitor C_{S2} reduces the effective emitter-degeneration caused by resistor R_{PTAT}. These components contribute to the stability of the circuit.

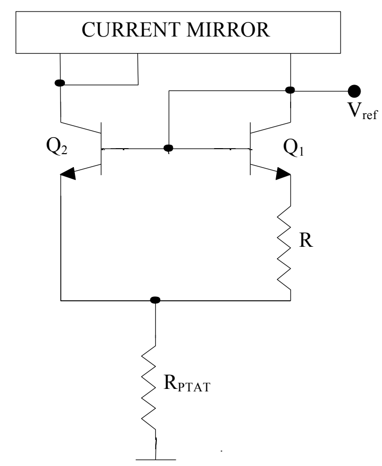

Figure 1. Basic cell.

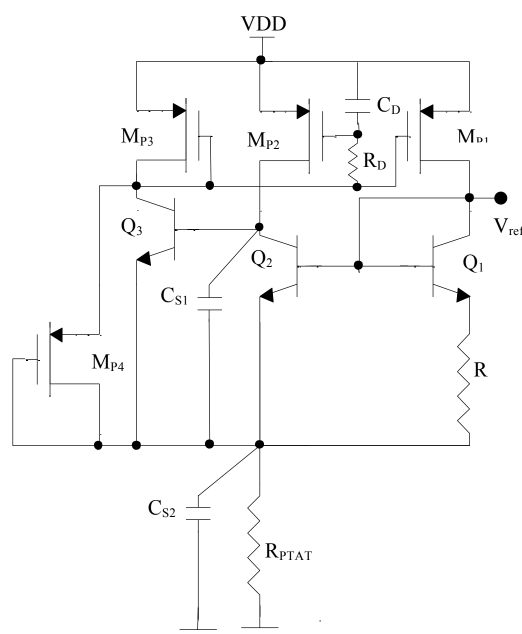

Figure 2. A first-order bandgap reference.

3. ERROR SOURCES

Errors in the bandgap reference voltage and its temperature coefficient arise from the non-idealities in the values and matching of resistors and transistors in the circuit.

Errors also result from Early-voltage effects between Q_1 and Q_2. These errors can be significantly reduced through circuit design techniques though, where their collector voltages are forced to be equal. In the present case, transistor Q_3 reduces the mismatch between the collector voltages of Q_1 and Q_2 such that their effects on the reference voltage are negligible. Further package-stress may introduce more errors, depending on the type of package (plastic, ceramic, etc.) [8]. This effect is difficult to model and it's analysis is beyond the scope of this work, which studies the effect of the sources of error introduced through circuit and die non-idealities.

In the analyses presented, the variable subscripted by 'x' represents the erroneous quantity. For example, I_{PTAT-x} represents the erroneous PTAT current. Further, the symbol Δ followed by a quantity represents the variation error in that quantity. For example, ΔV_{ref} represents the variation of V_{ref} from ideality.

The reference voltage generated by the first-order bandgap reference is given by

$$V_{ref} = V_{BE2} + 3 I_{PTAT} R_{PTAT} \tag{1}$$

and, consequently,

$$\Delta V_{ref} = \Delta V_{BE2} + 3\Delta I_{PTAT} R_{PTAT} \ . \tag{2}$$

The factor of '3' arises since the current through R_{PTAT} is the sum of the PTAT currents flowing through Q_1, Q_2 and Q_3 and this value will change from circuit to circuit.

3.1 Resistor Mismatch

Mathematical Analysis: The mismatch between resistors R and R_{PTAT} can be described as

$$R_{PTAT-x} = \frac{R_{PTAT}}{R} R(1+\delta_{RR}) = R_{PTAT}(1+\delta_{RR}) \ , \tag{3}$$

where δ_{RR} is the fractional resistor mismatch. From Eqns. (A1) and (A2), it is clear that the mismatch affects only the PTAT component of the reference voltage. Thus, it can be seen that

$$V_{ref-x} = V_{ref} + 3 I_{PTAT} R_{PTAT} \delta_{RR} \ , \tag{4}$$

$$\Rightarrow \Delta V_{ref} = 3\frac{V_T \ln C}{R} R_{PTAT} \delta_{RR} \ . \tag{5}$$

Eqn. (5) suggests that the error is a PTAT error.

Simulation Results: This mismatch can be modeled by a resistor in series with R_{PTAT} having a value of ΔR_{PTAT} where $\Delta R_{PTAT}=R_{PTAT}\delta_{RR}$. For the analysis, a mismatch of 2% was assumed. Fig. 3 shows a comparison between the error in V_{ref} obtained through the analysis and that obtained through simulations. As can be seen, the error predicted through both procedures is in close agreement (within 4%).

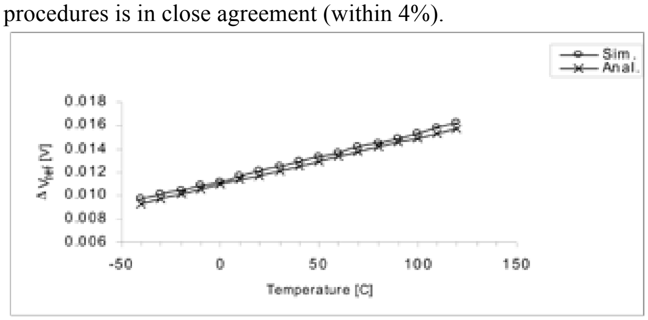

Figure 3. Comparison of simulated and analytical ΔV_{ref} for a resistor mismatch of 2%.

3.2 Resistor Tolerance

Mathematical Analysis: Process variations can lead to error sources due the deviation of the resistor values from their desired values. The variation of R_{PTAT} is absorbed by resistor mismatch for its variation is gauged against resistor R. The tolerance can then by quantitatively described as $R_x=R(1+\delta_{RA})$,where δ_{RA} is the fractional deviation of resistor R from its nominal value. Using Eqns. (A1), (A3), and (A5), we can see that the expression for the error in V_{ref} is given by

$$\Delta V_{ref} = -\left[V_T\delta_{RA} + 3\frac{V_T \ln C}{R} R_{PTAT}\left(\delta_{RA} - \delta_{RA}^2 + \delta_{RA}^3\right)\right], \tag{6}$$

a Complementary To Absolute Temperature (CTAT) error.

Simulation Results: Assuming a fractional tolerance error δ_{RA}, this error can be simulated by adding a resistor of value $\delta_{RA}R$ in series with R. Fig. 4 shows a comparison of the simulated and analytical results for a 20% tolerance variation. The simulated results are within 2% of the analytical results.

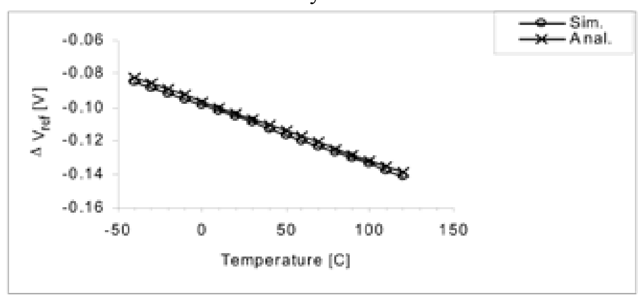

Figure 4. Comparison of simulated and analytical ΔV_{ref} for a resistor tolerance of 20%.

3.3 Temperature Coefficient of Resistors

Mathematical Analysis: The temperature drift of resistors R and R_{PTAT} also deteriorate the performance of the reference. Since the PTAT term of the reference voltage involves the ratio of R and R_{PTAT}, it is unaffected by the temperature drift of the resistors, as their temperature coefficients track one another. However, the V_{BE2} term is affected since I_{PTAT} is affected. Using Eqns. (A1), (A6) and (A8), we see that the error in the reference voltage due to resistor temperature drift is given by

$$\Delta V_{ref} = -V_T \ln[1+A(T-T_r)+B(T-T_r)^2] \ , \tag{7}$$

a non-PTAT error.

Simulation Results: First-order and second-order temperature coefficients having values of $5x10^{-4}$/°C and $2x10^{-4}$/°C^2, respectively, have been assumed for the simulations. Fig. 5 shows the close agreement (within 6%) obtained from a comparison of ΔV_{ref} from the analytical expression and simulations.

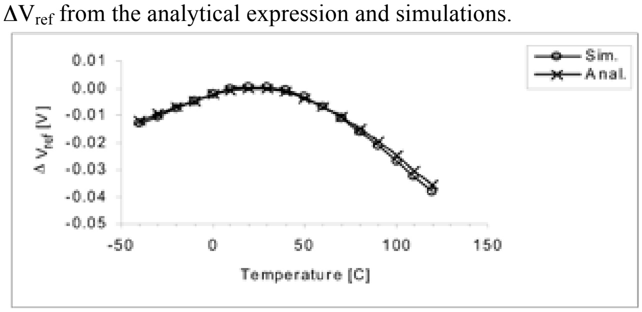

Figure 5. Comparison of simulated and analytical ΔV_{ref} for resistor TCs of $5x10^{-4}$/°C and $2x10^{-4}$/°C^2.

3.4 Transistor Mismatch

Mathematical Analysis: Transistor mismatch errors result from a deviation in the desired ratio of the areas of transistors Q_1 and Q_2. The mismatch in the transistors adversely affects the PTAT current. Using Eqns. (A1), (A2), (A10) and (A11), if δ_{NPN} is the fractional error in the ratio, the error in the reference voltage is given by

$$\Delta V_{ref} = \frac{V_T \delta_{NPN}}{\ln C} + 3\frac{V_T}{R} R_{PTAT} \delta_{NPN}, \qquad (8)$$

a PTAT error.

Simulation Results: This error source is simulated by changing the ratio of the transistors by a relative quantity, δ_{NPN}. Fig. 6 shows a comparison of the error in V_{ref} obtained through the analysis and that obtained through simulations. As can be seen, there is a close agreement between the analysis and simulations within 2%.

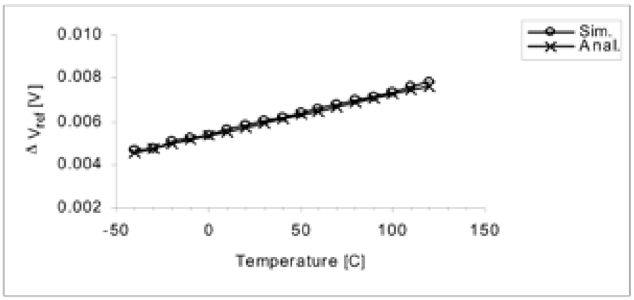

Figure 6. Comparison of simulated and analytical ΔV_{ref} for a transistor mismatch of 2%.

3.5 Current-Mirror Mismatch

Mathematical Analysis: Current-mirror mismatch arises from the deviation in the required W/L ratio of the mirroring MOS transistors, or, equivalently, a mismatch in the areas of BJT transistors. Using Eqns. (A1), (A2), (A13)-(A16), for a mismatch of δ_M between transistors M_{P1} and M_{P2},

$$\Delta V_{ref} = V_T \delta_M \left(1 + \frac{1}{\ln C}\right) + \frac{V_T}{R}\left[3\delta_M + \ln C\left(1 + \frac{\delta_M}{\ln C}\right)\delta_M\right] R_{PTAT}. \qquad (9)$$

Eqn. (9) shows that the error has a PTAT dependence.

Simulation Results: The mismatch was simulated by adding a transistor having a W/L ratio δ_M times that of M_{P2} in parallel with it. A typical mismatch, δ_M, of 10% was assumed. Figure 7 shows a close agreement (within 5%) of the simulated and analytical values of ΔV_{ref}.

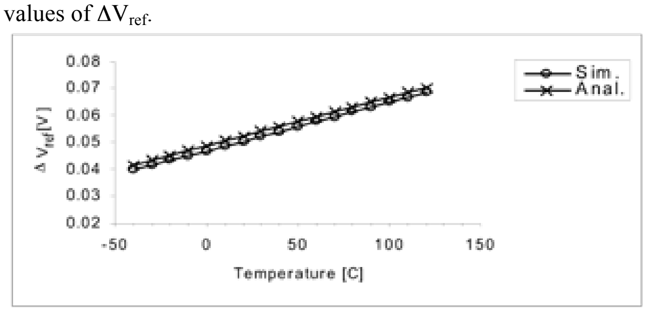

Figure 7. Comparison of simulated and analytical ΔV_{ref} for a current-mirror mismatch of 10%.

4. DISCUSSION

The errors due to resistor mismatch, transistor tolerance, and current-mirror mismatch (resistor tolerance) have a PTAT (CTAT) temperature dependence. Consequently, tuning a PTAT trimming resistor eliminates the effects of these errors [8], as shown in Figures 8-11 (comparison of ideal reference, erroneous reference, and erroneous after trim). On trimming resistor R_{PTAT}, the erroneous curve falls back to the ideal reference voltage curve (within 0.5% of the original trace). This has been shown for a resistor mismatch of 2% (Figure 8), resistor tolerance of 20% (Figure 9), transistor mismatch of 2% (Figure 10), and current-mirror mismatch of 10% (Figure 11), respectively.

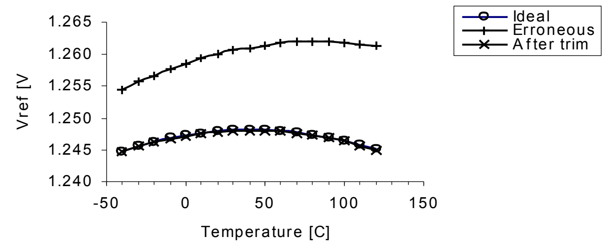

Figure 8. Ideal and erroneous reference voltage (before and after trimming) for the case of resistor mismatch.

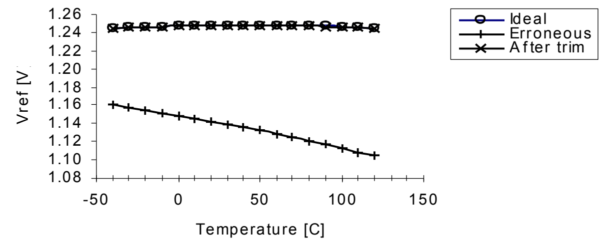

Figure 9. Ideal and erroneous reference voltage (before and after trimming) for the case of resistor tolerance.

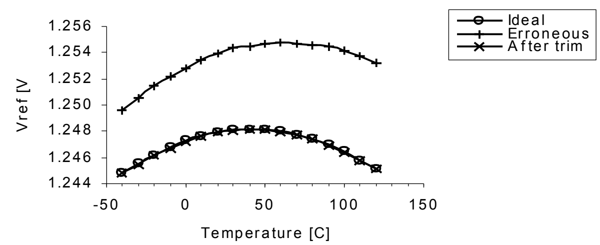

Figure 10. Ideal and erroneous reference voltage (before and after trimming) for the case of error due to transistor mismatch.

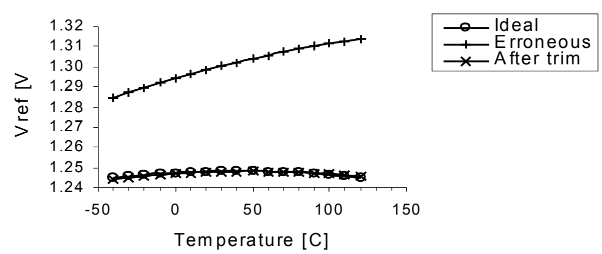

Figure 11. Ideal and erroneous reference voltage (before and after trimming) for the case of current-mirror mismatch.

Table 1 presents a comparison of the simulated and analytical values of the error in the reference voltage at 25 ºC (the reference voltage at room temperature is 1.248V). The trim range, using an RMS sum of the errors, is 4.4%. Table 2 presents a qualitative comparison of the various errors. Resistor's TC error, in spite of not being dominant, is not linear or trimmable, whereas current-mirror mismatch is dominant, linear, and trimmable.

5. CONCLUSIONS

Various sources of error that deteriorate the performance of a bandgap reference have been analyzed and the following conclusions have been reached:

- Resistor Tolerance and current-mirror mismatch are the largest sources of error in a bandgap circuit and, hence, close attention must be paid to maximize the accuracy of the resistors and to decrease the mismatch of mirror devices by appropriately designing device dimensions, layout geometries, and layout techniques (e.g. common-centroid configuration, use of dummy active devices on the periphery, etc.) and circuit techniques (e.g. cascodes and appropriate current densities).

- The characteristics and layout of the resistors in the circuit have a significant effect on the bandgap performance – the resistors must be laid out to maximize accuracy and matching, and their material should exhibit a low temperature coefficient.
- Transistor and resistor, mismatch and tolerance, errors can be "trimmed out" by tuning a PTAT trimming resistor. However, resistor TC errors cannot be trimmed.

Type of Error	Error in Devices	Analytical ΔV_{ref}[mv]	Simulated ΔV_{ref}[mv]	Diff. betn. Sim and Anal
Res. Mism.	2%	11.9	12.3	3.3 %
Res. Tol.	20%	-106.7	-107.5	0.7 %
Res. T.C.	TC1=500/ºC TC2=200/ºC^2	0.0	0.0	0.0 %
Trans. Mism.	2%	6.0	6.1	1.6 %
Current Mirror Mism.	10%	53.4	51.4	3.9 %

Table 1. Simulation/analytical comparison of error sources in the reference voltage (at room temperature).

Type of Error	Relative Magnitude	Trimmable	Temp. Dependence
Res. Mism.	Small	Yes	PTAT
Res. Tolerance	Large	Yes	CTAT
Res. T.C.	Small	No	Non-linear
Trans. Mism.	Very small	Yes	PTAT
Current Mirror Mism.	Large	Yes	PTAT

Table 2. Qualitative comparison of the various errors

APPENDIX

The base-emitter voltage of a transistor is given by

$$V_{BE} = V_T \ln\left(\frac{I_C}{J_S \cdot \text{Area}}\right), \tag{A1}$$

where I_C and J_S are the collector current and reverse saturation current per unit area of the transistor. The PTAT current is

$$I_{PTAT} \equiv I_{C2} = \frac{V_T}{R}\ln\left(C \cdot \frac{I_{C1}}{I_{C2}}\right), \tag{A2}$$

where C is the ratio of the areas of transistors Q_1 to Q_2, and I_{C1} and I_{C2} are their collector currents, respectively.

Resistor Tolerance: From Eqns. (A1) and (A2),

$$\Delta V_{BE2} = V_{BE2-x} - V_{BE2} = V_T \ln\left[\frac{R}{R(1+\delta_{RA})}\right] \approx V_T \ln(1-\delta_{RA})$$

$$\Rightarrow \Delta V_{BE2} \approx -V_T \delta_{RA}, \tag{A3}$$

$$I_{PTAT-x} = \frac{V_T \ln C}{R(1+\delta_{RA})} \approx \frac{V_T \ln C}{R}\left(1 - \delta_{RA} + \delta_{RA}^2 + \delta_{RA}^3\right) \tag{A4}$$

$$\Rightarrow \Delta I_{PTAT} \approx -\frac{V_T \ln C}{R}\left(\delta_{RA} - \delta_{RA}^2 + \delta_{RA}^3\right). \tag{A5}$$

Resistor Temperature Coefficient: Assuming A and B are the first- and second-order temperature coefficients, resistor R is

$$R(T) = R(T_r)[1+A(T-T_r)+B(T-T_r)^2], \tag{A6}$$

where T_r is room temperature. From Eqns. (A1) and (A2),

$$V_{BE2-x} = V_{BE2} + V_T \ln\left(\frac{R(T_r)}{R(T)}\right) \tag{A7}$$

$$\Rightarrow \Delta V_{BE2} = (-V_T)\ln[1+A(T-T_r)+B(T-T_r)^2]. \tag{A8}$$

Transistor Mismatch: For a fractional error of δ_{NPN} in the ratio of the areas of transistors Q_1 and Q_2,

$$I_{PTAT-x} = \frac{V_T}{R}\ln(C(1+\delta_{NPN})) = I_{PTAT} + \frac{V_T}{R}\ln(1+\delta_{NPN}) \tag{A9}$$

$$\Rightarrow \Delta I_{PTAT} \approx \frac{V_T}{R}\delta_{NPN}, \tag{A10}$$

$$\Delta V_{BE2} = V_{BE2-x} - V_{BE2} = V_T \ln\left(\frac{I_{PTAT-x}}{I_{PTAT}}\right)$$

$$= V_T \ln\left\{\frac{\ln[C(1+\delta_{NPN})]}{\ln C}\right\} \approx V_T \ln\left(1 + \frac{\delta_{NPN}}{\ln C}\right)$$

$$\Rightarrow \Delta V_{BE2} \approx \frac{V_T \delta_{NPN}}{\ln C}. \tag{A11}$$

Current Mirror Mismatch: A mismatch in any one of the transistors of the current mirror (M_{P1} or M_{P2}) changes the current in all the branches of the circuit. Assuming a mismatch of δ_M between transistors M_{P1} and M_{P2} ($I_{D-MP2}=(1+\delta_M)I_{D-MP1}$, where I_{D-MP1} and I_{D-MP2} are the drain currents of M_{P1} and M_{P2}, respectively) and using Eqn. (A2), the erroneous PTAT current is

$$I_{PTAT-x} = \frac{V_T}{R}\ln\left[\frac{I_{C2}(1+\delta_M)C}{I_{C2}}\right] = I_{PTAT} + \frac{V_T}{R}\delta_M \tag{A12}$$

$$\Rightarrow \Delta I_1 = \frac{V_T}{R}\delta_M, \tag{A13}$$

where ΔI_1 is the error in the current flowing through all three branches. The current through Q_2 has a further error due to the actual mismatch of the current mirror,

$$\Delta I_2 = I_{PTAT-x}\delta_M = \frac{V_T}{R}\ln[(1+\delta_M)C]\delta_M \approx \frac{V_T}{R}\ln C\left(1+\frac{\delta_M}{\ln C}\right)\delta_M, \tag{A14}$$

$$\Delta V_{BE2} = V_T \ln\left[\frac{I_{PTAT-x}(1+\delta_M)}{I_{PTAT}}\right] = V_T \ln\left[(1+\delta_M)\frac{\ln(1+\delta_M)C}{\ln C}\right]$$

$$\Rightarrow \Delta V_{BE2} \approx V_T \delta_M\left(1 + \frac{1}{\ln C}\right). \tag{A15}$$

Consequently,

$$\Delta V_{ref} = \Delta V_{BE2} + (3\Delta I_1 + \Delta I_2)R_{PTAT}. \tag{A16}$$

REFERENCES

[1] R.J. Widlar, "New Developments in IC Voltage Regulators", *IEEE J. Solid-State Circuits*, Vol. SC-6, pp. 2-7, Feb. 1971.

[2] K.E. Kujik, "A precision reference voltage source", *IEEE J. Solid-State Circuits*, Vol. SC-6, pp. 2-7, June 1973.

[3] A.P. Brokaw, "A Simple Three-Terminal IC bandgap Reference", *IEEE J. Solid-State Circuits*, Vol. SC-9, pp. 388-393, Dec. 1974.

[4] B.S. Song and P.R. Gray, "A Precision Curvature-Compensated CMOS Bandgap Reference," Vol. SC-18, pp. 634-643, Dec. 1983.

[5] P.R. Gray and R.G. Meyer, *Analysis and Design of Integrated Circuits*. New York: John Wiley & Sons, Inc. 1993

[6] G.A. Rincon-Mora and P.E. Allen, "1.1-V current-mode and piecewise-linear curvature-corrected bandgap reference," *IEEE. J. Solid-State Circuits*, vol. 33, pp. 1551-1554, Oct. 1998.

[7] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, "Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage", *IEEE. J. Solid-State Circuits*, vol. 36, pp. 1076-1081, July 2001.

[8] G.A. Rincon-Mora, *Voltage References*, IEEE Press, John Wiley & Sons, Inc., 2002.