TP11.4 A 1-Volt CMOS Op Amp Using Bulk-Driven MOSFETs

Phillip E. Allen, Benjamin J. Blalock and Gabriel A. Rincon

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250

IC technology trends suggest that future implementation of mixed analog digital circuits using standard CMOS will have power supplies of 1.5V or less [1-2]. Furthermore, it is anticipated that the threshold voltages will not significantly decrease below what is available today [3]. As a result, it is important to develop circuit techniques that permit existing CMOS technologies to implement analog circuits at power supply voltages as low as 1V. This paper describes some of these techniques and illustrates their application in the design of a CMOS op amp operating from a 1-Volt power supply. This op amp was fabricated using a digital, 2 micron CMOS technology having threshold voltages of 0.7 to 0.8V and demonstrated performance comparable with op amps using higher power supply voltages.

The most serious limitation of analog MOSFET circuits as the power supply voltage is reduced is the threshold voltage. It is easy to see that without using alternative techniques that the power supply must at least be equal to the sum of the magnitudes of the n-channel and p-channel thresholds. Techniques of circumventing this limitation include composite transistors, forward biasing the bulk-source junction and the use of MOSFETs in their own well driven from the bulk as the input devices with the gate at a constant voltage. These techniques all permit the transistor to operate in strong inversion and result in dc currents equivalent to higher voltage designs.

The composite transistor is an example of using multiple transistors to achieve transistor characteristics that are superior to a single transistor. A good example is the regulated cascode current sink/source [4]. This circuit has been used as the starting point for developing a composite transistor that maintains the saturation characteristics of a MOSFET at low values of drain-source voltage. It is also possible to slightly forward-bias the transistors in their own well to reduce the threshold effects and achieve better large signal performance. Figure 1 shows the schematic of a n-type composite transistor and its experimental output characteristics. The p-type composite transistor is similar. The concepts behind the composite transistor have been described in another publication [5]. The composite transistor offers superior performance over a single transistor at drain-source voltages down to 0.1V. The composite transistor is also useful for achieving better transistor characteristics for short-channel technology.

The third and most important circuit technique for low voltage analog circuits is to drive the MOSFET in its own well from the bulk rather than the gate. Figure 2 shows a cross-section of the bulk-driven MOSFET. The gate is taken to a fixed voltage which is sufficient to form a channel between the source

and drain. The current flowing between the source and drain is controlled by the bulk-source potential. Also shown is a vertical PNP transistor (QV), a lateral PNP transistor (QL) and a bulk JFET. The current flow in both BJTs is negligible because the base-emitter voltage is small. The primary current flow is unipolar current in the channel and is controlled by the equivalent bulk JFET.

The experimental drain current versus the bulk-source voltage for a fixed gate-source voltage of the bulk-driven MOSFET is shown in Figure 3. Also shown on this figure is the drain current versus the gate-source voltage for a zero bulk-source voltage. It is clear that the bulk-driven MOSFET is equivalent to a JFET where both IDSS and VP are dependent on the fixed gate-source voltage. Although it is not shown, the substrate current is less than 100fA for bulk-source voltages less than a forward bias of 0.4V.

The bulk-driven MOSFET or gate-controlled JFET can be modeled using a modified MOSFET large signal model [6] or by a JFET model. It can be shown that the small signal transconductance of the bulk-driven MOSFET can easily be as large as the transconductance of the gate-driven MOSFET. The gate-controlled JFET has identical characteristics to a normal JFET. Some exceptions are a larger shunt input capacitance and noise. The current flow is at the surface so that the 1/f noise is not as low as a normal JFET. The noise appears to be about 1.5 times that of a normal MOSFET. Both the noise and capacitance can be reduced by careful layout of the well. Matching characteristics are at least as good as a MOSFET in normal operation.

The three techniques described above were applied to the design of a CMOS op amp capable of operating with power supply voltages as low as 1V. The block diagram of the op amp is shown in Figure 4. It is a folded-cascode topology and uses a bulk-driven input PMOS pair to avoid the large values of gate-source voltage required to turn on the MOSFET. The tail current and current mirror are three p-type composite transistors. The two current source transistors are n-type composite transistors. The minimum voltage across the p-type and n-type composite transistors is slightly larger than 100mV as seen from Figure 1 for the n-type composite transistor.

The schematic of a 1V CMOS op amp is shown in Figure 5. Only transistors M1 and M2 are bulk-driven. The technology is n-well which allows the PMOS devices to be bulk-driven. In addition, the PMOS transistors of the various composite transistors are slightly forward biased by a dc current IBulk in order to decrease the threshold voltage of these transistors in the normal gate-driven operation. This allows the currents to be larger at low power supply voltages. The op amp of Figure 5 was fabricated and experimentally measured. The experimental results are summarized in Figure 6. The results are comparable with CMOS op amps operated at higher power supply voltages.

Acknowledgments

The authors acknowledge the contributions of Craig Petrie and MOSIS for fabrication of the circuits reported in this paper.

References

[1] A.P. Chandrakasan, S. Sheng, and R.W. Brodersen, "Low-Power CMOS Digital Design," *IEEE JSSC*, Vol. 27, No. 4, pp. 473-484, April 1992.

[2] M. Nagata, "Limitations, Innovations, and Challenges of Circuits and Devices into a Half Micrometer and Beyond," *IEEE JSSC*, Vol. 27, No. 4, pp. 465-472, April 1992.

[3] Chenming Hu, "Future CMOS Scaling and Reliability", *Proc. of the IEEE*, Vol. 81, No. 5, pp. 682-

652, May 1993.

[4] E. Sackinger and W. Guggenbuhl, "A High-Swing, High-Impedance MOS Cascode Circuit," *IEEE JSSC*, vol. 25, no.1, pp. 289-298, Feb. 1990.

[5] A. Coban and P. Allen, "A 1.75V rail-to-rail CMOS op amp," *Proc. ISCAS*, 1994, pp. 497-500, May 1994.

[6] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Inc., pp. 20-22, 1994.

FIGURE CAPTIONS

Figure 1 - NMOS composite transistor schematic and experimental output characteristics.

Figure 2 - Cross-section of the bulk-driven MOSFET.

Figure 3 - Linear drain current as a function of the bulk-source voltage and gate-source voltage for four different transistors.

Figure 4 - Block diagram of the 1-Volt op amp architecture.

Figure 5 - 1-Volt op amp schematic.

Figure 6 - Experimental performance of the 1-Volt CMOS op amp.

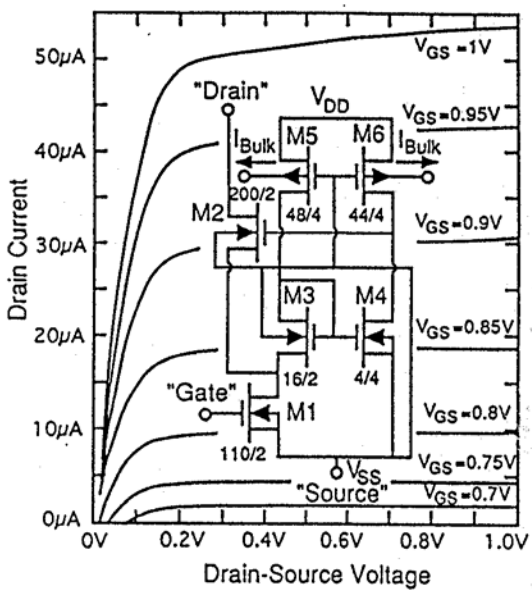

Figure 1: nMOS composite transistor schematic and experimental output characteristics

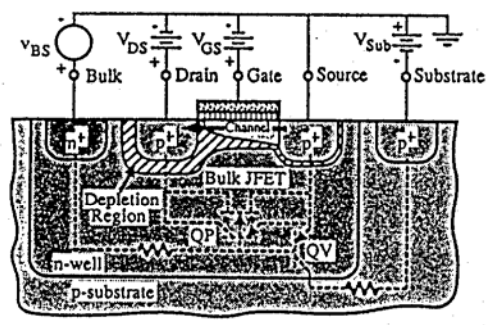

Figure 2: Cross-section of the bulk-driven MOSFET

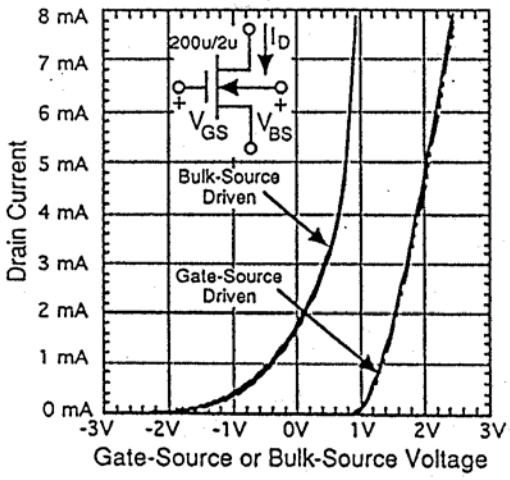

Figure 3: Linear drain current as a function of the bulk-source voltage and gate-source voltage for four different transistors.

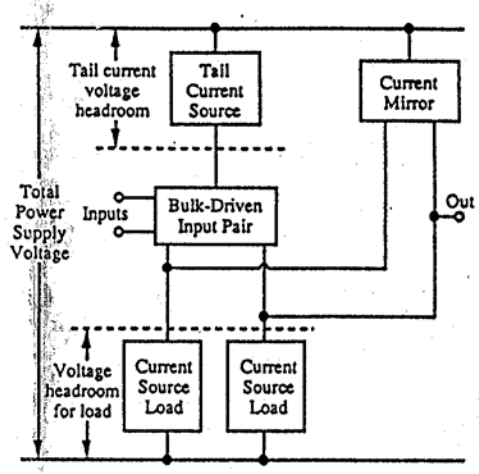

Figure 4: Block diagram of the 1V opamp architecture.

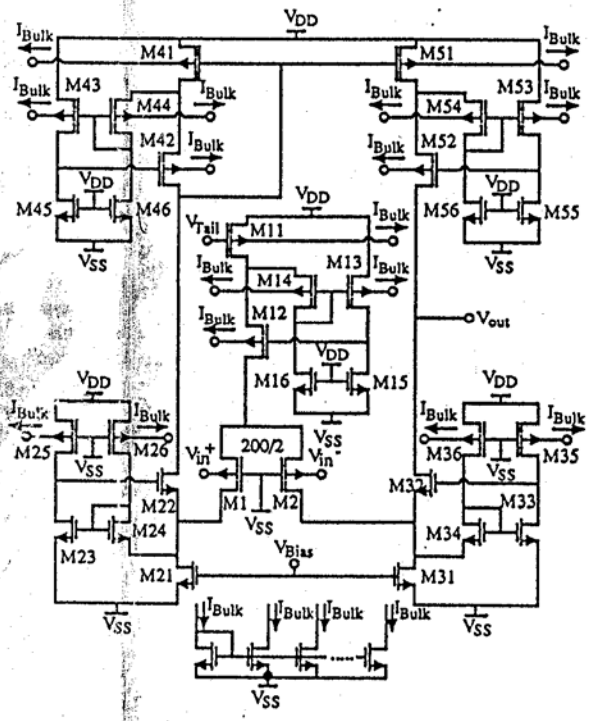

Figure 5: 1V opamp schematic.

Low-frequency gain	>500
Unity gain-bandwidth	0.6MHz
Power dissipation	45μW
Area (2μm technology)	0.35mm²
Input common-mode range	0.2 - 0.88V
Output swing	0.2 - 0.85V

Table 1: 1V CMOS opamp experimental performance. (1V power supply, 15pF load capacitance)