

# **A 5mA 0.6 $\mu$ m CMOS Miller-Compensated LDO Regulator with -27dB Worst Case Power Supply Rejection Using 60pF of On-Chip Capacitance**

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*A 0.6 $\mu$ m CMOS 1.8V 5mA Miller-compensated SoC LDO regulator that uses only 60pF of capacitance to achieve a worst case power supply rejection (PSR) of -27dB over 50MHz is proposed. The entire regulator is shielded from fluctuations in the supply using an NMOS cascode which is biased using a charge pump, voltage reference, and RC filter to maintain low dropout. The RC filter establishes a stable bias for the cascode without a significant impact on the efficiency or bandwidth of the LDO regulator.*

As dense digital circuitry is packed close to sensitive analog blocks for higher integration, SoC solutions are swamped in switching noise generated by digital circuits, RF blocks, and DC-DC converters. In this harsh environment, linear regulators have to protect noise-sensitive analog blocks like VCOs and ADCs from coupled supply noise that has amplitudes of the order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz [1]. Along with high PSR performance over a wide frequency range, these regulators need to exhibit low dropout to allow them to operate at the low supply voltages characteristic of state-of-the-art CMOS processes. Moreover, these LDOs need to be stable and reject noise without the aid of bulky external capacitors, using only on-chip capacitors that are constantly constrained in size by valuable silicon real estate [3-6]. Finally, these SoC LDOs are increasingly deployed at the point-of-load and hence need to supply currents in the range of 2 to 20mA [3-6].

Numerous techniques have been used to improve the PSR of linear regulators. The simplest solution is to place an RC filter in line with the power supply to filter out fluctuations before they reach the regulator [8]. However, for an integrated SoC solution, the high power losses and reduction in voltage headroom caused by this resistor would severely limit its size, thereby constraining the filter's effectiveness.

Fig. 1(a) presents a methodology that utilizes an NMOS device to cascode for the NMOS pass device of the linear regulator, thereby isolating it from the noisy power supply [3]. To maintain low dropout the gate of the cascoding NMOS and the supply of the error amplifier has been boosted using a charge pump. The error amplifier cannot be cascoded as conveniently as the pass device since the gate of its cascode would require a boosted voltage of two gate-source drops above the output, leading to higher complexity in the charge pump design. Hence, it uses an RC filter to suppress fluctuations in the power supply and the systematic fluctuations of the charge pump. Establishing a low RC filter pole for an SoC solution leads to critical tradeoffs: the capacitance can be increased with a significant increase in silicon real estate consumption or the resistance can be increased thereby limiting the bandwidth of the error amplifier which shall now need to operate at very low current levels to minimize the resistive drop and power dissipation in the filter.

In [4], a PSR of -40 dB over a wide frequency range is achieved using an NMOS device to cascode the PMOS pass device of a Miller-compensated linear regulator, as shown in Fig. 1(b). Due to relatively high voltage headroom (3.3V) the gate of the NMOS cascode is biased through the supply using a simple RC filter. The high voltage headroom also allows the error amplifier, which is powered directly from the supply (versus through a cascode), to use internal cascodes and gain boosting to improve its PSR performance, leading to higher dropout and power consumption. Moreover, the circuit uses 1.2nF of on-chip decoupling capacitance that occupies an area that is prohibitively large for many VLSI SoC systems.

The proposed regulator achieves a high PSR while exhibiting a lower dropout voltage and utilizing much lower on-chip capacitance, valuable for modern low-voltage environments with dense packing. Fig. 2 presents the simplified schematic of the proposed system to achieve high PSR performance over wideband frequencies [9]. The NMOS cascode, MNC, shields the entire regulator from fluctuations in the power supply. To maintain low dropout, the gate of the cascode needs to be biased at a voltage above the supply. This function is performed by the charge pump (CP), which powers a voltage reference, which, in turn, establishes a supply-independent bias for MNC. Since MNC acts like a voltage follower for noise at its gate, it is critical to shield the gate of MNC from supply fluctuations. The RC filter in series with the voltage reference achieves this by shunting supply ripple to ground. Notably, since the filter is placed in a path that does not carry any dc current, the filter pole can be reduced by designing as large a resistor as practically possible without a resulting loss in voltage headroom, efficiency, or bandwidth.

The proposed system was implemented in a 0.6 $\mu$ m CMOS technology ( $V_{TN}=0.7V$ ,  $V_{TP}=-0.9V$ ), measured, and evaluated. The die photograph is shown in Fig. 3. The charge pump is a simple voltage doubler [10] – its output is shown in Fig. 4. The voltage reference, that consumes a total current of 30 $\mu$ A, establishes a stable bias of 2.7V for the cascode by forcing a temperature-independent current of 10 $\mu$ A into a diode-connected NMOS and resistor. The RC filter, using a 500K resistor and 15pF capacitor, establishes a filter pole of roughly 20KHz to effectively attenuate supply noise. The core Miller-compensated SoC LDO uses a 3pF compensation capacitor along with a 10pF output capacitor (Fig. 2) and is capable of sourcing 5mA of load current. The error amplifier of the LDO consumes 40 $\mu$ A of quiescent current for meeting the transient specifications (and if the same RC filter were inserted in series with it for ripple rejection, the resistive drop across the filter would be 20V). The entire system utilizes 60pF of on-chip capacitance making it extremely compact.

The measured worst case PSR of the Miller-compensated LDO, as shown in Fig. 5, is 3dB and -27dB without and with the cascode strategy, respectively. It is seen that the PSR of the voltage reference is roughly 20dB and starts rolling off after 10MHz; the RC filter in series, however, ensures that the roll off takes place at a much lower frequency of 20KHz. When the supply of MNC and CP is decoupled and noise is introduced only in the latter (path ‘a’ in Fig. 2), the system rejects noise through the combined PSR of the voltage reference and core regulator. When noise is introduced only at the drain of MNC (path ‘b’ in Fig. 2), which is in saturation, its high drain-resistance shields the Miller-compensated core regulator ultimately leading to a 30dB improvement at the worst case. The cascode strategy impacts the transient response of the regulator and degrades the accuracy by approximately 171mV for a 5mA load step as shown in Fig. 6. The minimum voltage headroom required by the system is given by

$$V_{DD-\min} = \max\{V_{TP} + 4V_{DS-\text{sat}}, V_{OUT} + 2V_{DS-\text{sat}}\} \quad (1)$$

which, given a  $V_{TP}$  of 0.9V for this process, is approximately 1.8V.

A 5mA SoC LDO regulator utilizing 60pF of on-chip capacitance and having a worst-case PSR performance of -27dB over 50MHz has been designed. It utilizes a simple NMOS cascoding device to shield the entire regulator from fluctuations in the power supply. The gate of the NMOS cascode has been boosted to voltages above the supply rail using a charge pump and has been kept free of high frequency supply fluctuations using a simple RC filter voltage reference. The system has been implemented in a 0.6 $\mu$ m CMOS process. In conclusion, an

integrated LDO with high PSR over a large bandwidth for state-of-the-art SoC environments has been presented.

### **References**

- [1] S. Zhao, K. Roy, "Estimation of Switching Noise on Power Supply Lines in Deep Sub-Micron CMOS Circuits," *Proc. 13th Intl. Conf. VLSI Design*, Calcutta, 2000, pp. 168-173.
- [2] P. Larsson, "Power Supply Noise in Future ICs: A Crystal Ball Reading," *Proc. IEEE Custom Integrated Circuits Conf.*, San Diego, 1999, pp. 467-472.
- [3] C. Lee, K. McClellan, J. Choma Jr., "A Supply-Noise-Insensitive CMOS PLL with a Voltage Regulator Using DC-DC Capacitive Converter," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1453-1463, Oct. 2001.
- [4] J. M. Ingino, V.R. von Kaenel, "A 4-GHz Clock System for a High-Performance System-on-a-Chip Design," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1693-1698, Nov. 2001.
- [5] V.R. von Kaenel, "A High-Speed, Low-Power Clock Generator for a Microprocessor Application," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp.1634-1639, Nov. 1998.
- [6] G.W. den Besten, B. Nauta, "Embedded 5V-To-3.3V Voltage Regulator for Supplying Digital IC's in 3.3V CMOS Technology," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp. 956-962, July 1998.
- [7] H. Tanaka, et al., "A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme," *IEEE Jour. of Solid-State Circuits*, vol. 34, pp. 1084-1090, Aug. 1999.
- [8] Dallas Semiconductor/Maxim, Appl. Note 883, "Improved Power Supply Rejection for IC Linear Regulators." [Online] Available: [http://www.maxim-ic.com/appnotes.cfm/appnote\\_number/883](http://www.maxim-ic.com/appnotes.cfm/appnote_number/883)
- [9] V. Gupta, G.A. Rincón-Mora, "A Low Dropout, CMOS Regulator with High PSR over Wideband Frequencies," *Proc. IEEE Intl. Symp. Circuits Systems*, vol. 5, pp. 4245-4248, May, 2005.
- [10] P. Favrat, P. Deval, M. J. Declercq, "A High-Efficiency CMOS Voltage Doubler," *IEEE Jour. Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.

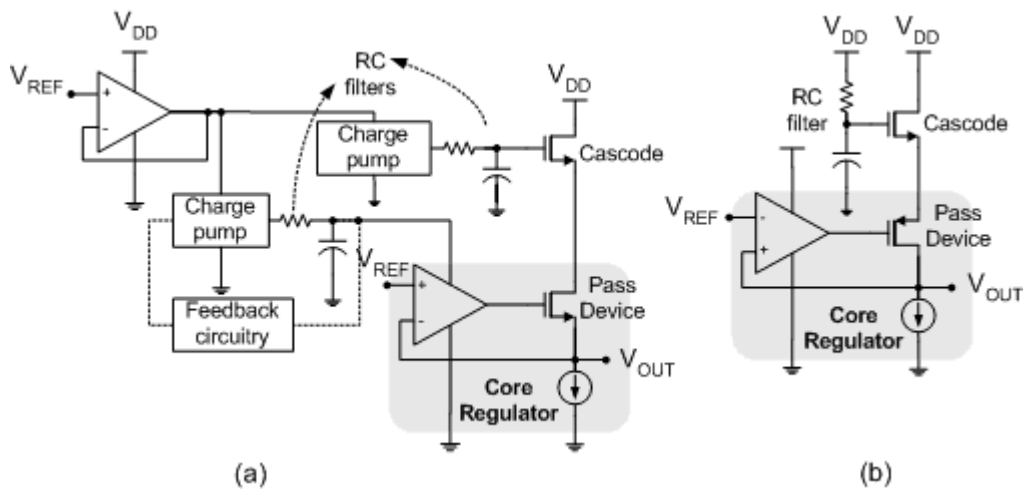


Fig. 1. Previously implement techniques to achieve high PSRR.

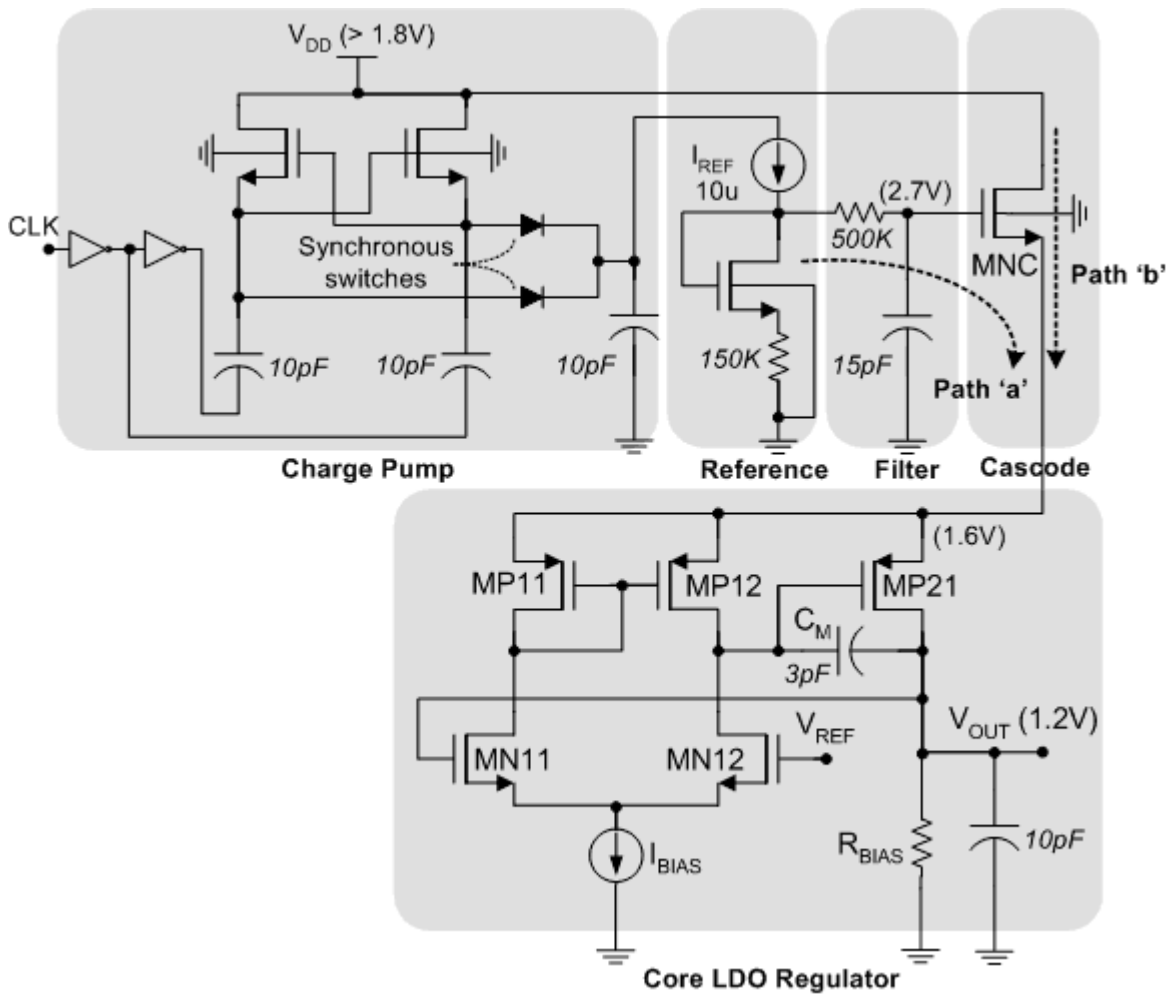


Fig. 2. Schematic of technique to enhance PSR over wideband frequencies.

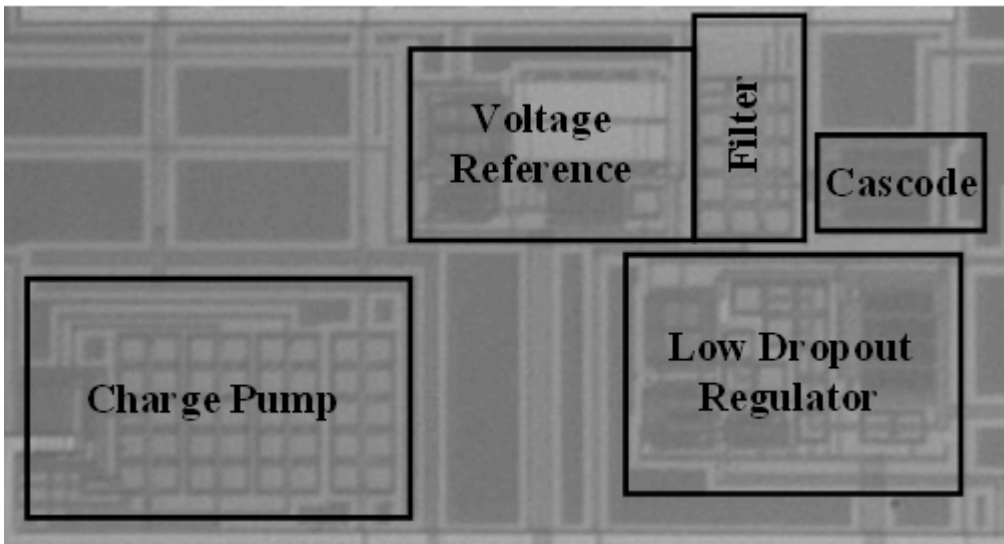


Fig. 3. Die photograph.

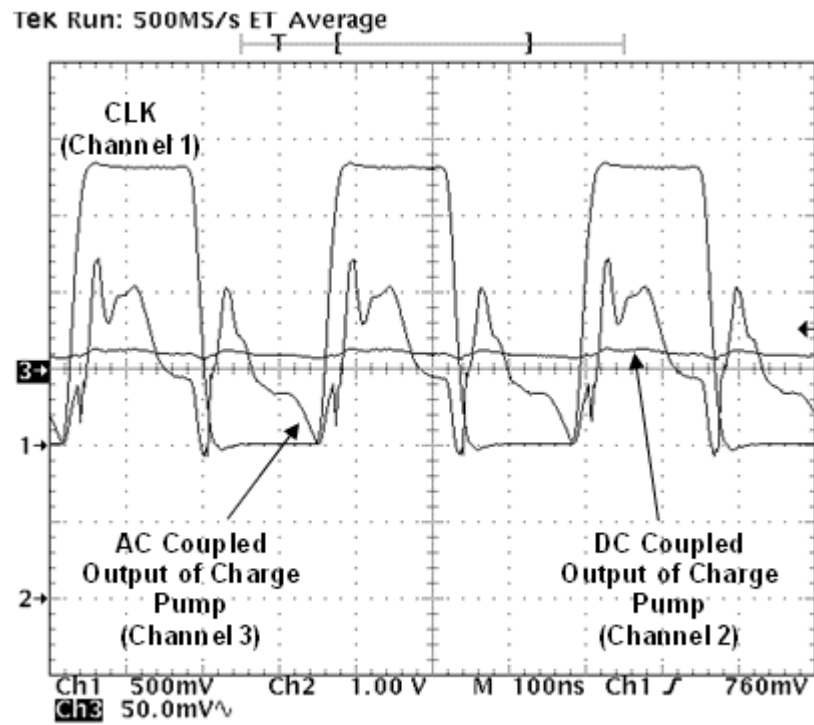


Fig. 4. DC- and AC-coupled output of charge pump.

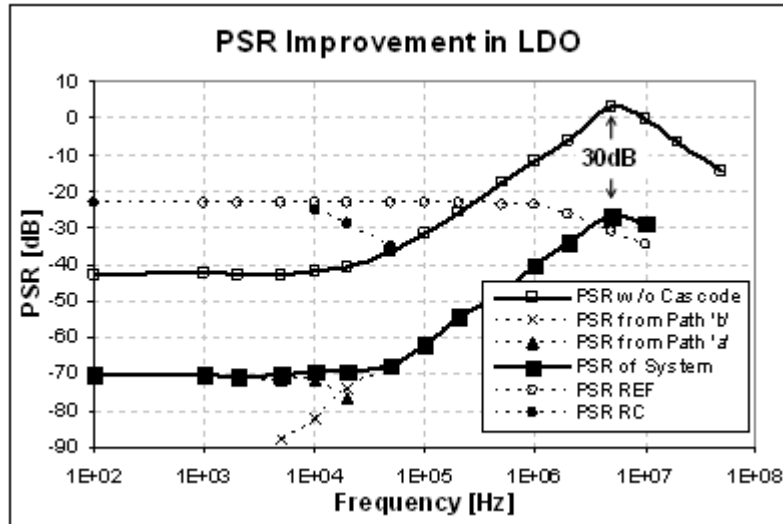


Fig. 5. Improvement in PSR of Miller-compensated LDO due to proposed strategy.

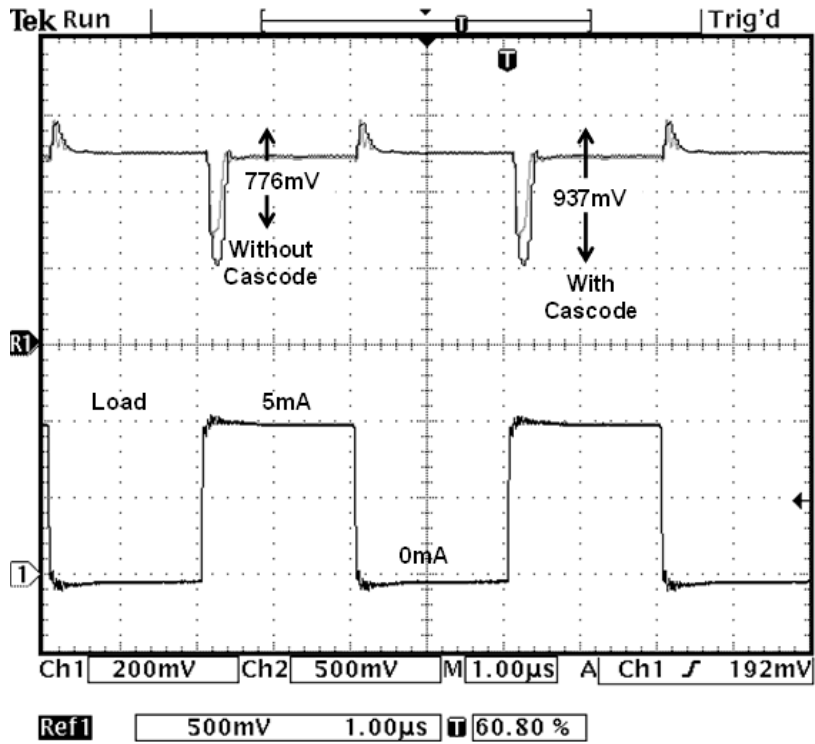


Fig. 6. Impact of cascode strategy on transient response.





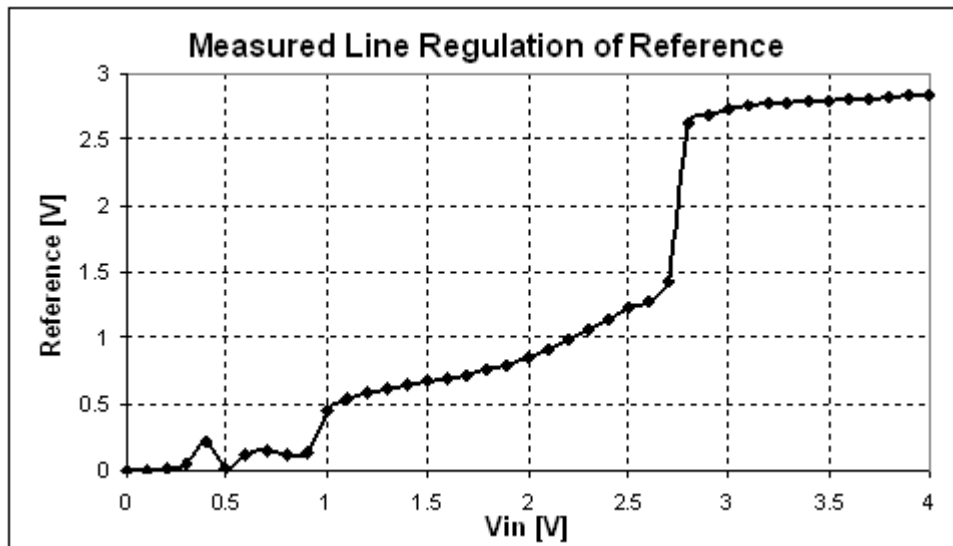


Fig. S3. Line regulation of voltage reference.