Predicting and Designing for the Impact of Process Variations and Mismatch on the Trim Range and Yield of Bandgap References

Abstract

Process tolerance and device mismatch produce significant random variations in bandgap voltage reference circuits. These variations lead to errors in the reference voltage and significantly impact manufacturing cost by increasing trimming requirements and decreasing yield. Current-mirror mismatch, followed by V_{BE} spread, package shift, and resistor mismatch are the dominant sources of random error in bandgap reference circuits. A folded-cascode topology, often used in low voltage applications, can be optimized to effectively alleviate the effects of a mismatch in the mirroring devices. By decreasing the ratio of the current in the cascode to that of the bandgap core circuit and ascertaining the best-matched devices for implementing current-mirrors and current sources, these mismatches can be significantly reduced.

1. Introduction

Bandgap references are high-performance analog circuits that find applications in a host of analog [1], digital [2], and mixed-signal [3] integrated systems. For all these applications, the accuracy of the bandgap reference voltage is crucial as it can severely limit system functionality. This is especially so in the case of sensitive blocks like sensors and A/D converters [3]. Considerable work has been done to protect the reference voltage from variations in supply [2], [4], [5] and temperature [1], [3], [4], [6], [7]. However, process variations, which arise from tolerance and mismatch, can degrade the accuracy of the most well-designed bandgap reference and hence need careful attention [1], [4], [8] which is why trim circuits are used. These process-induced errors in the reference voltage raise the required trim-range (number of trim bits) for a specified accuracy performance, thereby directly affecting cost by lowering yield and increasing test time. Hence, quantifying and designing for the effect of the various sources of error that degrade the accuracy of bandgap references is crucial to predict trim range and yield.

This work presents the bandgap reference designer with analytical expressions for the impact of process variations on the bandgap voltage, and their implications on bandgap reference design and trim range. The analysis presented is applicable to most bandgap-based circuits. For clarity and convenience, the analysis is performed within the context of the bandgap's basic building block (described in Section II). Given the conclusions drawn in Section II, a practical bandgap reference topology (described in Section III) is designed and optimized to minimize the critical error sources. The final conclusions are presented in Section IV.

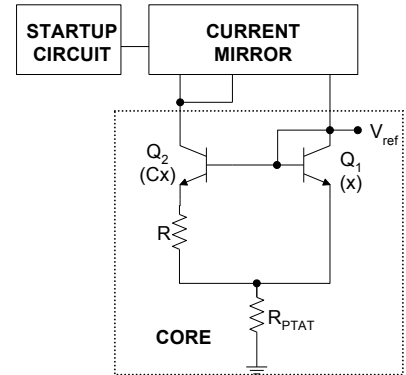## 2. Analysis of Process-Induced Errors

Fig. 1. Basic bandgap reference cell.

The basic topology of the circuit used for the analysis of error sources in bandgap references is shown in Fig. 1. This is the building block for most bandgap reference circuits [3], [4], [7], [8] and the expressions for the error in the reference voltage of this circuit can easily be applied to most practical bandgap implementations. Referring to Fig. 1, the reference voltage generated by the first-order bandgap reference is generally given by

$$V_{ref} = V_{BE1} + V_{PTAT} = V_{BE1} + 2I_{PTAT}R_{PTAT}$$

$$= V_{BE1} + 2\frac{V_t \ln C}{R}R_{PTAT}, \quad (1)$$

and, consequently,

$$\Delta V_{ref} = \Delta V_{BE1} + 2\Delta I_{PTAT}R_{PTAT}, \quad (2)$$

where V_{PTAT} is the Proportional to Absolute Temperature (PTAT) component of the reference voltage, I_{PTAT} is the PTAT current, and C is the ratio of the current densities of Q_1 and Q_2. A Δ symbol indicates a change in the variable that follows it. The factor of '2' arises since the current through R_{PTAT} is the sum of the PTAT currents flowing through Q_1 and Q_2 and this value will change from circuit to circuit. The magnitude of the error in the reference voltage (ΔV_{ref}) is obtained by comparing the reference voltage of an "ideal" bandgap circuit to that in which the particular error source being studied is artificially introduced. The mathematical analysis of the error

sources is presented in [8]. The analysis of current-mirror mismatch, a critical source of error, has been presented in the Appendix as an example of the analysis.

2.1 Sources of Errors

Current Mirror Mismatch: This error arises from the deviation in the required ratio of the mirror currents. This deviation may arise from various factors, like W/L mismatch, threshold voltage (V_T) mismatch, lambda effects of MOS devices, resistor mismatch, and area mismatch of bipolar devices. Using (A1)-(A8), for a mismatch of δ_M between the mirror currents,

$$\Delta V_{ref} = V_t \, \delta_M \left(1 + \frac{1}{\ln C} \right)$$
$$+ \frac{V_t}{R} \left[2\delta_M + \ln C \left(1 + \frac{\delta_M}{\ln C} \right) \delta_M \right] R_{PTAT}. \qquad (3)$$

Resistor Mismatch: Though resistors can be matched to a high degree of accuracy (typically 1%), resistor mismatch influences the PTAT voltage, which is a strong function of the ratio of the resistors R_{PTAT} and R. From [8], a δ_{RR} mismatch in these resistors leads to

$$\Delta V_{ref} = 2 \frac{V_t \ln C}{R} R_{PTAT} \delta_{RR} = V_{PTAT} \delta_{RR}. \qquad (4)$$

Resistor Tolerance: Process variations can lead to a large deviation of resistor values (often as large as 20%). This variation changes the V_{BE} component by altering the PTAT current flowing in the circuit. If δ_{RA} is the fractional deviation of the resistors from their nominal value, from [8], we can see that the expression for the error in V_{ref} is given by

$$\Delta V_{ref} = - V_t \delta_{RA}. \qquad (5)$$

Transistor Mismatch: These errors result from a deviation in the desired ratio of the areas of transistors Q_1 and Q_2. From [8], if δ_{NPN} is the fractional error in the ratio, the error in the reference voltage is given by

$$\Delta V_{ref} = \frac{V_t \delta_{NPN}}{\ln C} + 2 \frac{V_t}{R} R_{PTAT} \delta_{NPN}$$
$$= \frac{1}{\ln C} \left(V_t + V_{PTAT} \right) \delta_{NPN}. \qquad (6)$$

Other Error Sources: Other large sources of error are V_{BE} spread and package shift. The spread in the base-emitter voltage of the bipolar transistors is a considerable source of error and is critical because it directly translates to an error in the bandgap reference voltage. Package shift (a deviation in the reference voltage caused by the local and die-wide mechanical stresses of a package on its IC) is a post-package error that can only be effectively eliminated by post-package trimming techniques [1], [11]. Errors due to Early voltage effects between the two bipolar

devices have non-linear temperature dependence and, consequently, cannot be trimmed. However, they can be significantly mitigated through circuit design techniques whereby the collector voltages of the bipolar devices, Q_1 and Q_2, are forced to be equal [1]-[8].

2.2 Relative Magnitude

Table 1 presents a summary of the various sources of error in a bandgap reference circuit and their typical 3-σ magnitudes along with qualitative comparison. The application of the results of the error source analysis to a practical bandgap reference topology and its close agreement with simulated data over a wide temperature range can be obtained in [8]. In [8], the 3-σ offset in the reference voltage caused by current-mirror mismatch proved to be the dominant error in a bandgap reference. This is primarily due to the high mismatch characteristic of MOS transistors, which are often used to implement current-mirrors. In MOS devices, drain-current mismatch can be as high as 10% [9]. In general, MOS devices do not match as well as bipolar transistors (~2%), which in turn exhibit a higher mismatch than resistors (~1%) [10]. Hence, current-mirror mismatch, V_{BE} spread, package shift, and resistor mismatch have the largest impact on trim range.

Table 1. Principle features of the various error sources in bandgap references.

Error	Typical Value (3-σ)	Relative Magnitude of Effect	Trimmable	Temp. Dependence
Current-Mirror Mismatch	±1 % - 10 %	Very Large	Yes	Linear
Resistor Mismatch	±1 %	Large	Yes	Linear
Resistor Tolerance	±20 %	Small	Yes	Linear
Transistor Mismatch	±1%	Small	Yes	Linear
V_{BE} spread	±24 mV	Very Large	Yes	Linear
Package Shift	±5 – 7 mV	Large	No	Non-linear
Early voltage, lambda	50V, 0.1	Small	No	Non-linear

2.3 Discussion – Trimmability and Layout Implications of Errors

As (3)-(6) reveal, the errors due to resistor mismatch, resistor tolerance, and transistor mismatch, exhibit linear temperature dependence. Hence, they can be eliminated by trimming, which inherently cancels first order errors because it alters the PTAT voltage to account for their

effects. The error due to current-mirror mismatch is also trimmable if the current mismatch (δ_M) is not temperature dependent. However, trimming is an expensive and time-consuming process, and a reduction in the trim range required for a bandgap reference is desired for lower test times and higher yield.

Errors due to resistor mismatch and transistor mismatch can only be reduced through layout techniques (such as common centroid layout and dummy devices). Errors due to resistor tolerance can be reduced by choosing a material for the resistor that does not exhibit significant spread in resistivity over process, voltage, and temperature. Polysilicon resistors, for example, typically exhibit a smaller variation of resistance with voltage and temperature, than n-well resistors. Further, though current-mirror mismatch errors can be significantly mitigated through careful layout, they can also be attenuated through judicious circuit design practices. Section 3 describes one such design methodology.

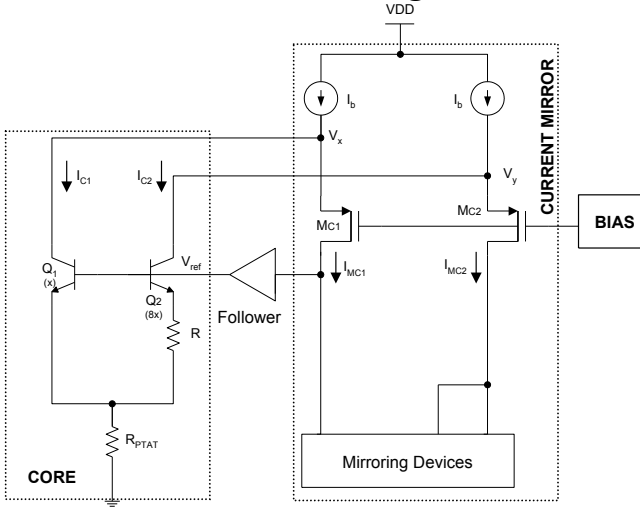# 3. Reducing the Effects of Current-Mirror Mismatch in a Practical Design

Fig. 2. Block diagram of bandgap reference.

The folded topology is a well-known structure that is often used in low-voltage circuits. Fig. 2 presents the basic architecture of the bandgap reference under discussion, where a folded-cascode is used as a feedback error amplifier. Here, the shunt feedback from the folded-cascode amplifier decreases the output impedance of the bandgap, a critical specification for load regulation and shunting noise. However, within the context of a bandgap circuit, the entire folded-cascode structure functions as the effective current-mirror of the bandgap core.

Due to emitter degeneration, the transconductance of

the bandgap cell (Q_1 and Q_2) is much lower than the transconductance of a conventional input differential pair. This makes the bandgap reference extremely vulnerable to current-mirror mismatch, which produces large voltage offsets in the core. Hence, although a folded-cascode or Norton amplifier topology is well known, its design constrictions and tradeoffs differ in bandgap circuits, which are extremely sensitive to mismatch of the collector currents of the bipolar transistors (Q_1 and Q_2). In other words, the folded-cascode amplifier has to be optimized for low offsets.

3.1 Designing for Current-Mirror Mismatch

Proportioning the Currents: In the circuit of Fig. 1, if the current mirror is simply implemented using PMOS devices connected to the supply, a mismatch in the mirror currents directly causes a mismatch in the core collector currents. Thus, to reduce current-mirror mismatch errors, a technique is needed to densensitize the mismatch in the core currents to those of the mirroring devices. In Fig. 2, consider a mismatch in the currents through cascodes, M_{C1} and M_{C2}, which will lead to a difference in their absolute values. This difference, or surplus current, will be reflected as the difference between the currents in the core, i.e., the collector currents of Q_1 and Q_2. Now, if these core currents are higher than the currents in the cascodes, the percentage mismatch of the core currents will be lower than the percentage mismatch in the cascode currents. Further, if the core currents are raised while keeping the cascode currents constant, the same absolute (and fractional) mismatch in the cascodes will now produce an even smaller fractional mismatch in the core. Mathematically,

$$I_b = I_{MC2} + I_{C2} = I_{MC1} + I_{C1}$$
$$\Rightarrow I_{MC2} + I_{C2} = I_{MC2}(1 + \delta_{mirr}) + I_{C2}(1 - \delta_M),$$
$$\Rightarrow \delta_M = \delta_{mirr}\frac{I_{MC2}}{I_{C2}} = \delta_{mirr}K_I, \quad (7)$$

where δ_M and δ_{mirr} are the fractional mismatches in the currents in the core bipolar devices and the mirror cascodes, respectively, and K_I is the ratio of the current in the cascode to that in the core. Thus, by lowering the ratio K_I, the same fractional mismatch between the currents in the cascodes (and hence the mirroring devices), δ_{mirr}, produces a smaller mismatch in the core, δ_M. Hence, through a folded topology, the mismatch between the current-mirror devices is effectively *attenuated*.

The benefits of the folded topology, and hence of (7), have costs and limits. Note that current-mirror mismatch in the circuit of Fig. 2 stems from a mismatch in three pairs of devices, namely, mismatch in the I_b-current sources (ΔV_{ref-Ib}), V_T mismatch between the cascoding

devices M_{C1} and M_{C2} (ΔV_{ref-VT}), and mismatch in defining mirroring devices themselves ($\Delta V_{ref-mir}$). It is reasonable to expect the total current-mirror mismatch error to approximately equal the root sum squared (RSS) of these individual random errors, i.e.,

$$\Delta V_{ref} \approx \sqrt{\left(\Delta V_{ref-Ib}\right)^2 + \left(\Delta V_{ref-VT}\right)^2 + \left(\Delta V_{ref-mir}\right)^2}. \quad (8)$$

Thus, a reduction in the error predicted by (7) would only prove effective if mismatch error of the mirroring devices is dominant. Fig. 3 shows how the total induced error decreases with the ratio K_I. The error reduces proportionally till it reaches the "floor" set by V_T mismatch errors.

Further, the cascodes and mirroring devices form a high-gain amplifier that equalizes the collector voltages of the bipolars through feedback. Hence, decreasing the cascode current to very low levels would decrease finite gain errors caused by this amplifier by increasing the loop gain, but would also increase δ_{mirr} and the V_T mismatch [9]. Thus, in order to obtain the attenuation predicted by (7), a sufficiently high current in the cascode would be required, with a correspondingly larger current in the core, leading to the tradeoff of larger power dissipation for improved accuracy.
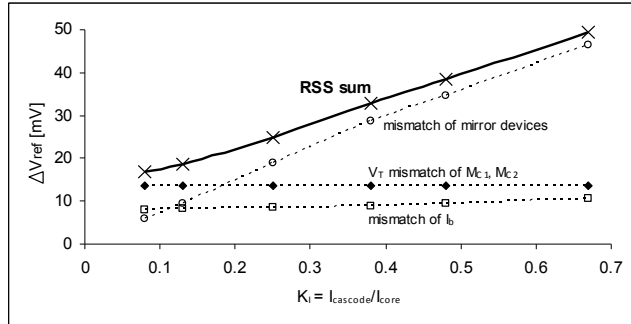

Fig. 3. Current-mirror mismatch error and its relation to the ratio of the current in the cascode to the core (K_I).

Implementing the I_b-current Sources: The I_b-current sources in Fig. 2 play a crucial role in the bandgap reference. The devices used to implement these sources should be extremely well matched to reduce current-mirror mismatch errors. A mismatch in these devices can decrease the effectiveness of folding the currents (shown in (7)) and can also cause its own current-mirror mismatch, even if the cascodes and mirroring devices are well-matched. On the other hand, increasing the output resistance of these current sources reduces the sensitivity of the bandgap core to V_T and K' mismatches of cascoding devices M_{C1} and M_{C2} (a higher output resistance increases the source-degenerating effects on M_{C1} and M_{C2}).

Resistors often exhibit superior matching properties to MOS devices. The latter, however, have higher output resistance. Thus, a delicate tradeoff exists in the design of the I_b-current sources, and the designer must therefore ascertain how these devices will match before making a design decision. For example, consider a 300 mV voltage drop across the I_b-current sources, a 1% resistor mismatch (R_{mis}), 2% transconductance parameter mismatch (K'$_{mis}$), 2% W/L mismatch (W/L$_{mis}$), and a 10 mV threshold voltage mismatch (V_{T-mis}). The current through the I_b-current sources implemented as resistors would depend on the magnitude of their resistance and the voltage across them. Hence, the mismatch between the I_b-current sources if they are implemented as resistors, ($I_{b-mis-R}$), would be a root sum squared (RSS) of the random mismatch in the resistor values and of the voltage across them. Thus,

$$I_{b-mis-R} \approx \sqrt{\left(R_{mis}\right)^2 + \left(V_{T-mis}\right)^2}$$
$$= \sqrt{\left(1\%\right)^2 + \left(\frac{10}{300} \times 100\right)^2} \approx 3\%. \quad (9)$$

Assuming MOS devices, the mismatch ($I_{b-mis-MOS}$) is given by the RSS of the mismatch between transconductance parameter, K', W/L ratio, and threshold voltage, V_T. Hence,

$$I_{b-mis-MOS} \approx \sqrt{\left(K'_{mis}\right)^2 + \left(W/L_{mis}\right)^2 + \left(2V_{T-mis}\right)^2}$$
$$\approx \sqrt{\left(2\%\right)^2 + \left(2\%\right)^2 + \left(2 \times \frac{10}{300} \times 100\right)^2} \approx 6\%. \quad (10)$$

The overdrive voltage can be increased to attenuate the effect of V_T mismatch [10], at the cost of voltage headroom and current consumption. The factor of "2" arises for the V_T mismatch term because it is assumed that the MOS devices used to implement the current sources are operating in the saturation regime, where the drain current is proportional to the square of the overdrive voltage, or difference between the gate-source and threshold voltage. Intuitively, this can be seen by viewing the square overdrive term as two terms, each depending on V_T, and thereby doubling its mismatch effect.

Mismatches due to lambda effects and other MOS parameters (that have been ignored in (10)) further degrade the matching performance of these devices. Consequently, resistors would be a better design choice in implementing the $I_{b-current}$ sources (balancing matching versus source-degenerating performance). Ultimately, mismatches between the I_{b}-current sources can be notably reduced through the use of dynamic element matching (DEM) techniques [12], [13], which have an implied cost of complexity, die size, and noise. This would significantly reduce the ΔV_{ref-Ib} and ΔV_{ref-VT} terms in (8).

Implementing the Current-Mirror: The implementation of the current-mirror itself is critical and careful attention must be paid to its accurate and robust implementation.

The designer must ascertain the best-matched devices available, in a manner similar to the procedure for choosing the I_b-current sources.

3.2 Complete Circuit Description and Simulation Results

Fig. 4 presents the complete schematic of the proposed bandgap reference. High-β NPN devices, Q_3 and Q_4, along with their degenerating resistors, R_3 and R_4, form a well-matched, high output impedance current-mirror. Transistors Q_{FN} and Q_{FP} create a super-beta voltage follower, i.e., unity-gain buffer which is used to close the feedback loop and prevent the bandgap core from loading the current-mirror. Transistor M_{FOLL} provides the bias current for the super-β buffer. Finally, capacitor C establishes the dominant pole and hence the loop bandwidth of the circuit. Table 2 presents the simulated functional specifications of the circuit. Standard models compatible with 1.5μm process obtained from MOSIS were used for the simulations.
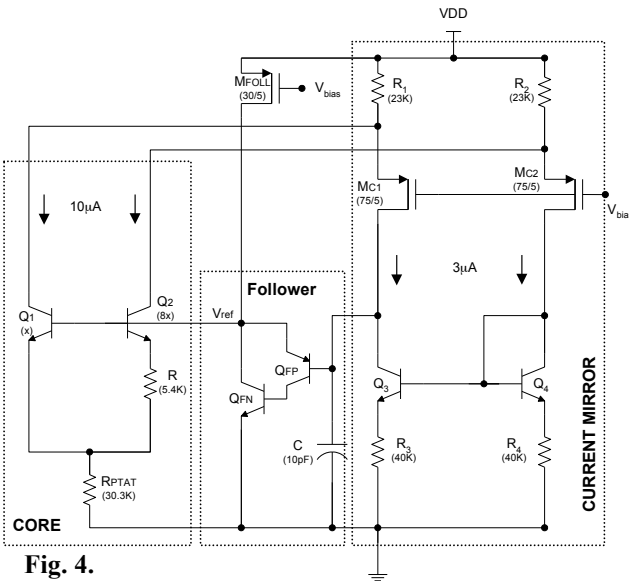

Fig. 4.
Circuit embodiment of a high-accuracy bandgap reference.

Table 3 presents a quantitative summary of the offsets induced by various random sources of error on the bandgap voltage and their comparison with their analytical counterparts. As can be seen, the two are in excellent agreement. The temperature drift of the current-mirror mismatch, now primarily caused by the V_T mismatch between the cascoding devices (since NPN devices and resistors can be matched to within 2%), depends on the temperature coefficient of the V_T mismatch, and hence this error is typically not trimmable. It can be minimized by increasing the flow of current

through the cascoding devices to minimize their mismatch, but that implies an increased current in the core to reduce mirror-imposed offsets. Further, 24 mV spread in the base-emitter voltage of the NPN devices is based on experience and takes into account worst-case process variations – it is now the primary factor that determines the trim range of the bandgap reference. The calculated trim-range is approximately ± 35 mV (70 mV full-scale).

Table. 2. Simulated circuit characteristics.

Circuit Parameter	Simulated Value
V_{ref} (@ T=27°C)	1.23 V
Minimum supply voltage	1.41 V
T.C. performance (after trim)	0.34 %
Quiescent Current	60 µA
Line regulation	1.27 mV/V
Power Supply Rejection (@100 Hz)	-55 dB

Table 3. Comparison of Simulated and Analytical Results for Error Sources (at 25 °C).

Type of Error	3-σ Error in Devices	Simulated ΔV_{ref} [mV]	Analytical ΔV_{ref} [mV]
Current Mirror Mismatch	±2% NPN mismatch, ±1% Resistor mismatch, ±5 mV V_T mismatch	±18.5	±16.9
Resistor Mismatch	±1%	±6.3	±6.4
Transistor Mismatch	±2%	±6.0	±6.0
Resistor Tolerance	±20%	±5.2	±5.1
ΔV_{be}		±24.0 mV	
Package Shift		±7 mV	
RMS Error	$\sqrt{\Delta V_{refi}^2}$ [mV]	±32.7	±31.8
Trim-range	Full-scale ≈ 2x RMS [mV]	65.4	63.6

4. Conclusions

The analytical expressions obtained for various sources of error allow a designer to quantitatively ascertain the impact of process variations on the trim range of a bandgap reference. Current-mirror mismatch, which causes a mismatch in the collector currents of the bipolar transistors in the core of the bandgap reference, is the dominant source of error. This mismatch is a combination of various errors, namely, Early voltage, lambda effects, W/L mismatch, resistor mismatch, and V_T mismatch. A folded topology is therefore used to decouple the biasing currents, and therefore the effects of the mirror devices,

from the bandgap core. Once decoupled, the design is optimized by reducing the ratio of the current in the cascode to that in the core. In general, current sources and mirrors must be implemented using best-matched devices available, after ascertaining the trade-offs between matching, output resistance, current consumption, and required voltage headroom. Hence, though process variations can significantly influence the trim range and yield of bandgap references, the analysis and circuit design principles presented allow the designer to predict and considerably attenuate their deleterious effects.

Appendix

In the analyses presented, the variable subscripted by 'x' represents the erroneous quantity. For example, I_{PTAT-x} represents the erroneous PTAT current. Further, the symbol Δ followed by a quantity represents the variation error in that quantity. For example, ΔV_{ref}, represents the variation of V_{ref} from ideality.

The base-emitter voltage of a transistor is given by

$$V_{BE} = V_t \ln\left(\frac{I_C}{J_S \cdot \text{Area}}\right), \qquad (A1)$$

where I_C and J_S is the collector current and reverse saturation current per unit area of the transistor. The PTAT current is

$$I_{PTAT} \equiv I_{C2} = \frac{V_t}{R} \ln\left(C \cdot \frac{I_{C1}}{I_{C2}}\right), \qquad (A2)$$

where C is the ratio of the areas of transistors Q_1 to Q_2, and I_{C1} and I_{C2} are their collector currents, respectively.

Current Mirror Mismatch: A mismatch in any one of the transistors of the current mirror changes the current in all the branches of the circuit. Assuming a mismatch of δ_M in the mirror currents ($I_{C1} = (1+\delta_M)I_{C2}$, where I_{C1} and I_{C2} are the mirror currents flowing in Q_1 and Q_2, respectively) and using (A2), the erroneous PTAT current is

$$I_{PTAT-x} = \frac{V_t}{R} \ln\left[\frac{I_{C2}(1+\delta_M)C}{I_{C2}}\right] = \frac{V_t}{R}\ln C + \frac{V_t}{R}\ln(1+\delta_M)$$
$$\approx I_{PTAT} + \frac{V_t}{R}\delta_M . \qquad (A3)$$

$$\Rightarrow \Delta I_1 = \frac{V_t}{R}\delta_M, \qquad (A4)$$

where ΔI_1 is the error in the current flowing through both branches. The current through Q_1 has a further error due to the actual mismatch of the current mirror,

$$\Delta I_1 = I_{PTAT-x}\delta_M = \frac{V_t}{R}\ln[(1+\delta_M)C]\delta_M$$

$$\approx \frac{V_t}{R}\ln C\left(1 + \frac{\delta_M}{\ln C}\right)\delta_M, \qquad (A5)$$

From (A1),

$$\Delta V_{BE1} = V_t \ln\left[\frac{I_{PTAT-x}(1+\delta_M)}{I_{PTAT}}\right]$$
$$= V_t \ln\left[(1+\delta_M)\frac{\ln(1+\delta_M)C}{\ln C}\right], \qquad (A6)$$

$$\Rightarrow \Delta V_{BE1} \approx V_T \delta_M\left(1 + \frac{1}{\ln C}\right). \qquad (A7)$$

Consequently,

$$\Delta V_{ref} = \Delta V_{BE1} + (2\Delta I_1 + \Delta I_2) R_{PTAT}. \qquad (A8)$$

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