Extracting the Frequency Response of Switching DC–DC Converters in CCM and DCM from Time-domain Simulations

Suhwan Kim, *Student Member, IEEE*, Gabriel A. Rincón-Mora, *Fellow, IEEE, and* Dongwon Kwon, *Student Member, IEEE*
School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA
E-mail: suhwan@gatech.edu, Rincon-Mora@gatech.edu, dkwon3@gatech.edu

Abstract—**Determining if a feedback loop is stable is crucial, and in the case of switching dc–dc converters, also considerably involved because some of the signals across the ac signal path are large signal and nonlinear. Today, designers rely on averaged and linearized small-signal models to approximate loop dynamics. This method is appropriate for well-tested dc–dc supplies like the buck and boost but less reliable and more difficult to apply to emerging non-conventional switchers used, for example, in energy harvesters. Overdesigning these circuits to overcome the uncertainty is often unacceptable because accuracy and efficiency, which are critical, normally suffer as a result. Extracting loop dynamics from actual time-domain waveforms is more accurate because, in averaging waveforms around a narrow bias point, conventional methods eliminate important loop information and constrain the model to small-signal variations – this paper proposes a way to extract small- and large-signal frequency response from time-domain simulations. The results from buck and boost converters under voltage- and current-mode control operating in CCM and DCM match theory well.**

Keywords—Switching dc–dc converters, loop dynamics, time-domain simulations, frequency response, nonlinear feedback

I. Stability Analysis of Switching Supplies

As portable electronics like cellular phones and wireless microsensors smarten and shrink, they demand more energy from smaller batteries, which means they suffer from shorter battery life [1]. Switched-inductor converters are the first line of defense against these degraded lifetimes because they transfer and condition higher power levels more efficiently than their switched-capacitor and linear low-dropout counterparts [2]–[3]. Unfortunately, switched circuits carry both linear and nonlinear signals through their feedback paths, so ensuring they remain stable across all possible operating conditions is as difficult as is critical [3].

Well-known linear techniques for determining stability, such as Bode, Nyquist, and root-locus plots, do not apply to nonlinear circuits without linearizing approximations. Testing the stability of switching converters therefore hinges on linearized models of nonlinear circuits. Programs like Saber [4]–[7], for example, average and linearize the behavior of switching circuits to build linear small-signal models with which to apply the aforementioned analytical methods. The limitation of this approach is accuracy because linearizing a signal this way removes ripple effects and applies only to small-signal variations [8]–[9].

Emerging applications, however, call for not only unique control schemes but also multiple intertwined feedback loops whose large-signal load-dump response is to traverse across operating regions [10]. Conventional voltage- and current-mode buck and boost ac models can neither describe the small-signal dynamics nor the large-signal transitions of these complicated nonlinear systems [9]–[10]. Eliminating the linearizing and averaging approximations that small-signal models impose both improves accuracy and extends the range over which the analysis is valid. Time-domain simulations forego these assumptions, but literature has yet to report how to use these simulations to extract the frequency response of nonlinear switching circuits, which is what this paper proposes. For this, while Section II briefly overviews switching dc–dc converter stability requirements, Sections III and IV introduce and apply the proposed simulation method to voltage- and current-mode buck and boost dc–dc switching converters operating in continuous and discontinuous conduction modes (CCM and DCM). Section V ends with conclusions.

Note: Lower case variables with upper case subscripts (e.g., s_O) describe signals entirely, upper–upper case combinations (e.g., S_O) only steady-state conditions, and lower–lower case combinations (e.g., s_o) only signal variations.

II. DC–DC Converter Stability Requirements

The objective of a switching dc–dc converter is to *regulate* one or several outputs by delivering only the power that the outputs require. For this, the system (in Fig. 1) senses the desired output (s_O) and feeds back a corresponding signal (s_{FB}) that a mixer compares against a reference input (s_I) to determine how much power to supply to s_O. The gain and delay through the feedback loop determine how close the system keeps s_{FB} to s_I, which is to say how well it regulates s_O [3] – higher loop gains ($A_{OL}\beta_{FB}$) and shorter delays reduce the error (s_E) between s_{FB} and s_I. To keep the system from oscillating uncontrallaby, s_{FB}'s phase and gain, once inverted by the mixer, should never match s_I's (to avoid positive feedback), so s_{FB}'s phase shift at the frequency when $A_{OL}\beta_{FB}$ is one (f_{0dB}) should be less than 180^O.

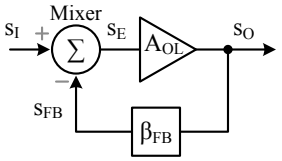

Fig. 1. Negative feedback loop.

As frequency increases, the impedance of a switching converter's inductor L_O, which connects the supply to the output v_O, rises, which means v_O receives less power from L_O at higher frequencies. As a result, L_O introduces a gain- and phase-reducing pole p_L to the system. The output capacitor C_O, which is across v_O and ground, shunts v_O's energy to ground, so C_O introduces another pole p_C. C_O's equivalent series resistance R_{ESR}, however, limits how much

energy C_O shunts, offsetting the effect of a pole with a gain- and phase-increasing (left-half-plane LHP) zero z_{ESR}. As L_O energizes in boost and boost-derived circuits (when L_O's current i_L rises in Fig. 2), a diode D_O disconnects v_O from L_O, so v_O droops, which means D_O introduces an out-of-phase feed-forward (right-half-plane RHP) zero z_D that increases gain but reduces phase shift. Interestingly, when i_L is discontinuous (in Fig. 2b), L_O has enough time to deliver all its energy to v_O, so both p_L and z_{RHP} disappear [11].

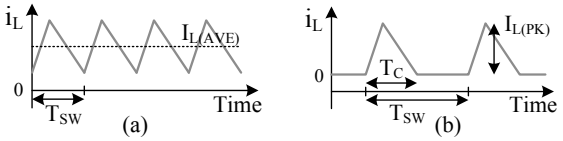

Fig. 2. Inductor current i_L in (a) CCM and (b) DCM.

The feedback circuit that senses v_O and controls the connectivity of L_O, C_O, and D_O must therefore introduce poles and/or zeros to ensure $A_{OL}\beta_{FB}$'s phase shift at f_{0dB} remains below 180^O. Because a single-pole response reaches f_{0dB} with 90^O of phase margin, adding a dominant low-frequency pole or a phase-saving LHP zero at or below f_{0dB} (i.e., voltage-mode control) is popular [12]. Other converters regulate i_L (i.e., current-mode control) to ensure the energy L_O delivers to v_O does not subside below f_{0dB} [3], [12]–[13], thereby eliminating p_L and leaving p_C as the dominant pole.

III. Extracting Frequency Response from Time-domain Simulations

As in other methods, determining how a circuit responds across frequency amounts to (*i*) opening the loop, (*ii*) injecting a sinusoid into the input side of the opening, (*iii*) monitoring the output side to determine loop gain $A_{OL}\beta_{FB}$, and (*iv*) repeating steps (*ii*) and (*iii*) at other frequencies. The key to avoiding averaged and linearized models of digital signals is knowing where and how to break the loop. For this, realizing that the steady state of a digital signal is not dc is crucial. In dc–dc converters, for example, the steady-state components of a switching node are the frequency, duty-cycle, and phase components that do not change with time.

The motivation for averaging digital blocks in the first place is to convert digital signals into the analog domain. A switching converter, however, already does this in the circuit in real time (via A_{OL}) by converting analog error signal s_E into a digital pulse train that determines the connectivity of L_O, C_O, and when used, D_O, whose filtering action generates analog output s_O. Accordingly, the best locations for opening the loop and injecting an analog sinusoid are the analog nodes: s_{FB}, s_E, and s_O. The challenge is breaking the loop while keeping loading and steady-state conditions intact.

One way to overcome this hurdle is to duplicate the entire circuit and use synchronized replica signals unaffected by the injected sinusoid (S_{FB}' in Fig. 3 because S_I is only dc) to establish steady-state conditions. Notice S_{FB}' in switching converters is a ripple whose frequency, duty cycle, and phase components do not vary with time. Duplicating the loading effects on the output side of the opening (s_{FB}) is also important because they affect frequency response. This is why Fig. 3 breaks the loop at the mixer, because the mixer presents minimal loading to s_{FB}, which if necessary, a capacitor can emulate. The next step is injecting the sinusoid into the opening: into the mixer by way of s_I, which without sinusoid s_i is only a dc reference S_I.

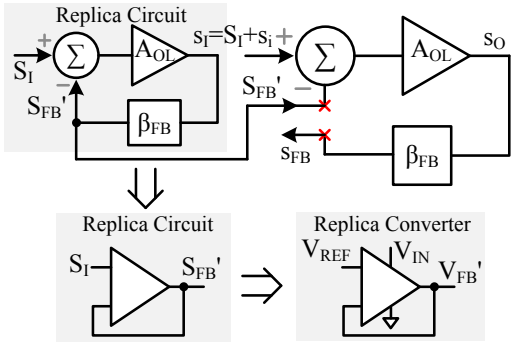

Fig. 3. Breaking the feedback loop at the mixer and using a synchronized replica circuit's signal (S_{FB}') to establish steady-state conditions.

Step (*iii*) is to measure the magnitude and phase of variations in s_{FB} (i.e., s_{fb}) with respect to s_i. As is, s_{FB} includes steady-state components so isolating s_{FB}'s behavior at s_i's frequency is necessary. A Fast-Fourier Transform (FFT) on s_{FB} well past the initialization process of the time-domain simulation extracts this data: $|s_{fb}/s_i|$ and s_{fb} and s_i's phase difference at s_i's frequency f_i, which describe $A_{OL}\beta_{FB}$'s magnitude and phase shift at f_i. Repeating steps (*ii*) and (*iii*) at different f_i's and compiling all the data into a Bode plot provides the information necessary to determine the system's proneness to oscillations by way of phase margin (PM).

IV. Method Execution and Validation

This section illustrates how to apply the proposed methodology through examples. Along the way, citing well-known topologies and comparing their results against well-established relationships validates the proposed process. The approach is therefore to start with a simple voltage-mode buck in CCM and DCM and gradually increase circuit complexity with a peak-current-mode topology and then a current-mode boost circuit in CCM, which incorporates p_L, p_C, z_{ESR}, and z_D plus the effects of a current loop.

A. Voltage-mode Buck Converter in CCM

A voltage-mode controller introduces a dominant low-frequency pole p_{EA} (e.g., with R_{EA} and C_{EA} in Fig. 4) to ensure $A_{OL}\beta_{FB}$ reaches f_{0dB} before any other pole or zero in the system. A comparator compares this slow-moving signal (v_{EA}) with a sawtooth (V_{SAW}) to generate a pulse whose width v_{EA} sets when v_{EA} crosses V_{SAW} and whose period V_{SAW} sets when V_{SAW} resets. The pulse-width modulated (PWM) signal then defines how long L_O energizes from input supply V_{IN} and de-energizes into the load.

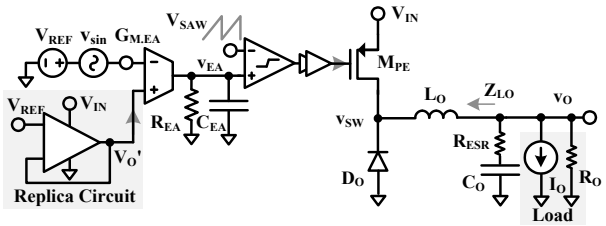

Fig. 4. Voltage-mode PWM buck converter.

The circuit normally compares v_O with V_{REF} to generate error control signal v_{EA}, but in breaking the loop, a replica circuit generates the steady-state signal V_O' (which V_{SAW} synchronizes) that biases the loop. Superimposing a sine wave with v_{sin} to V_{REF} then injects the input against which to compare v_O to extract $A_{OL}\beta_{FB}$. Performing time-domain simulations and FFTs to determine $A_{OL}\beta_{FB}$'s magnitude and phase across frequency when switching at 1 MHz generates the response in Fig. 5, which follows theory (in Eq. 1 [11]–

[14]) closely: a dominant p_{EA}, a complex pole pair $p_{L/C}$ above f_{0dB}, and a high-frequency z_{ESR}, as Table I summarizes.

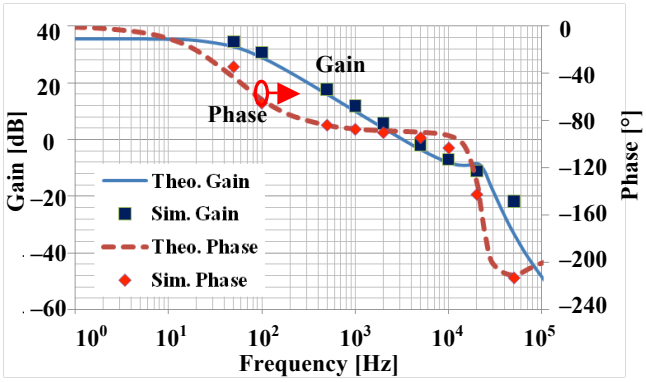

Fig. 5. Bode plot for the voltage-mode buck in CCM.

B. *Voltage-mode Buck Converter in DCM*

In DCM, L_O does not present a pole (p_L). Instead, L_O loads v_O across L_O's conduction time T_C (from Fig. 2b) with an impedance Z_{LO} that is equivalent to $(2L_O/T_C)(T_{SW}/T_C)$ [11]. So, removing C_{EA} to shift p_{EA} to high frequency (because p_{EA} is no longer necessary) and simulating the circuit in DCM (with lower load current) generates the response in Fig. 6. As before, time-domain simulation results follow theory (from Eq. 2) closely: a dominant p_C that C_O, R_O, and Z_{LO} establish with p_{EA} and z_{ESR} near f_{0dB}, as Table I summarizes.

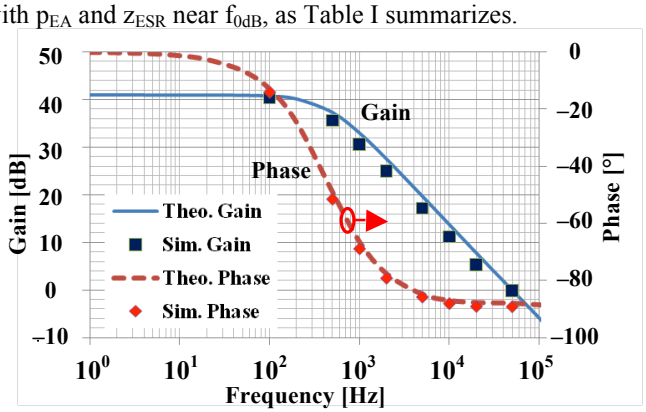

Fig. 6. Bode plot for the voltage-mode buck in DCM.

C. *Peak-current-mode Buck Converter in CCM*

In current-mode control, an internal feedback loop, as Fig. 7 illustrates, senses and converts i_L into a voltage v_I to compare and regulate i_L (via v_I) against a reference that slow-moving error voltage v_{EA} establishes with the outer loop (the one that senses v_O). Accordingly, if the internal loop's bandwidth exceeds f_{0dB}, L_O operates like a current source up to f_{0dB}, which means L_O's pole (p_L) disappears. Operationally, in the particular case of peak-current control, clock f_{CLK} starts L_O's energizing time and i_L's peak ends it.

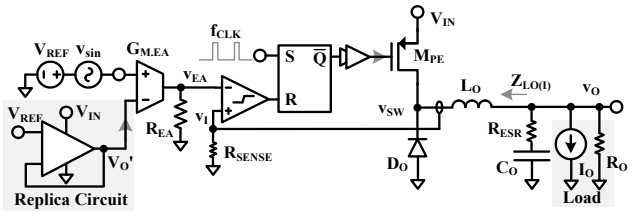

Fig. 7. Peak-current-mode PWM buck converter.

As before, a replica circuit generates the steady-state signal V_O' that biases the loop and sine wave v_{sin} sources the input with which to compare v_O to extract $A_{OL}\beta_{FB}$. As a current source, L_O now loads v_O with an impedance $Z_{LO(I)}$ that is equivalent to $2L_O/(1-D_L)^2T_{SW}$. With this in mind, the time-domain simulations of this circuit generate a response (in Fig. 8) that corresponds well with theory (from Eq. 3): a dominant p_C that C_O, R_O, and $Z_{LO(I)}$ establish with p_{EA} and z_{ESR} near but below f_{0dB}, as Table I details.

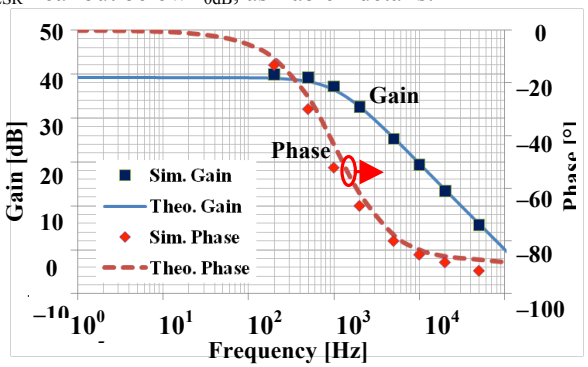

Fig. 8. Bode plot for the peak-current-mode buck in CCM.

D. *Peak-current-mode Buck Converter in DCM*

Operating in DCM, as in voltage mode, means L_O loads v_O across conduction time T_C with an impedance $Z_{LO(I.DCM)}$ that is equivalent to $2T_{SW}(V_O+V_D)^2/(I_{L(PK)}{}^2L_O)$. So, simulating the circuit in Fig. 7 in DCM (with lower load current I_O) produces the frequency response in Fig. 9 and Table I. As before, the results match theory (Eq. 4) closely: a dominant p_C from C_O, R_O, and $Z_{LO(I.DCM)}$ with p_{EA} and z_{ESR} above f_{0dB}.

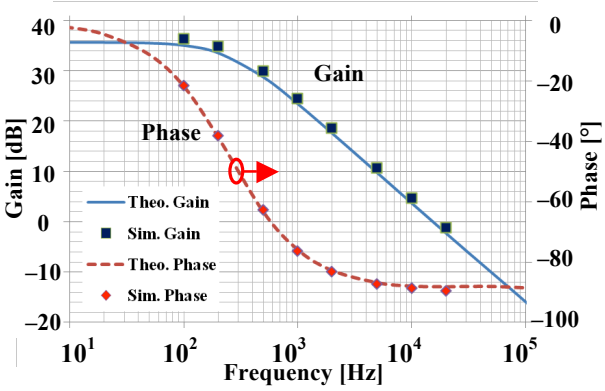

Fig. 9. Bode plot for the peak-current-mode buck in DCM.

E. *Peak-current-mode Boost Converter in CCM*

As in the buck case, the current-mode boost senses and regulates i_L (with R_{SENSE} in Fig. 10) to eliminate L_O's pole p_L. The difference is D_O disconnects L_O from v_O when L_O energizes, so D_O introduces RHP zero z_D at $(1-D_L)^2R_O/2\pi L_O$ [12]. To avoid sub-harmonic oscillations and the complexity that slope compensation introduces, the system regulates v_O to 2 V (when V_{REF} is 2 V) from a 1.6-V input supply V_{IN}.

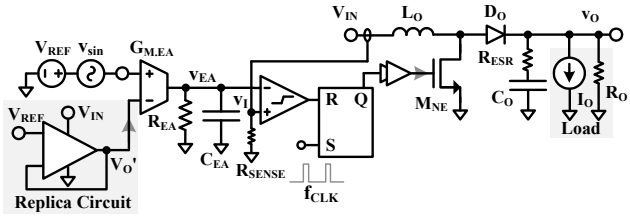

Fig. 10. Peak-current-mode PWM boost converter.

Because z_D in the case designed (as Table I shows) is at moderate frequencies, p_C is not low enough to ensure f_{0dB} falls below z_D, so a large C_{EA} now ensures this by introducing a considerably lower pole p_{EA}. Accordingly,

time-domain simulations produce the frequency response in Fig. 11, which closely follows theory (from Eq. 5). Here, p_{EA} is dominant, p_C is near f_{0dB}, and z_D and z_{ESR} follow.

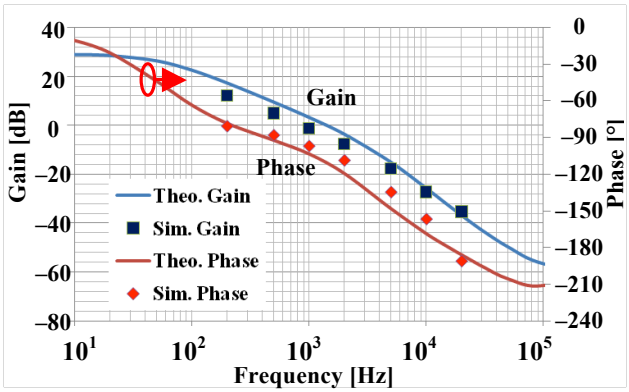

Fig. 11. Bode plot of peak-current-mode boost converter in CCM.

V. CONCLUSIONS

Extracting the loop dynamics of voltage- and current-mode buck and boost dc–dc converters operating in continuous and discontinuous conduction modes from time-domain simulations is possible. The technique presented and validated here is to break the loop at an analog point in the feedback path, bias the loop at the opening with the steady-state signal that a synchronized replica circuit generates, and inject a sinusoid with which to compare the output to extract loop-gain information. Realizing that frequency, duty cycle, and phase carry steady-state bias information is key here. The importance of extracting the frequency response this way is accuracy (i.e., reliability), because conventional methods average and linearize switching signals about a narrow region of operation, not only approximating dynamics but also limiting the range for which they are valid. Although conventional schemes work well for standard topologies, emerging applications, like hybrid fuel-cell–lithium-ion supplies and energy harvesters, incorporate more loops, switches, and operating modes, the impact of which conventional small-signal models cannot fully comprehend. Even if time-domain simulations require more time, fabricating system-on-chip (SoC) supplies without fully validating their loop dynamics with time-domain simulations is risky and therefore costly (with lower yield).

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$$A_{BUCK(V.CCM)} \equiv \frac{v_o}{v_{sin}} = \left(\frac{v_{ea}}{v_{sin}}\right)\left(\frac{v_o}{v_{ea}}\right) = \left(\frac{G_{EA}R_{EA}}{1+R_{EA}C_{EA}s}\right)\left[\frac{\left(\frac{1}{C_O s}+R_{ESR}\right)\|R_O}{L_O s+\left(\frac{1}{C_O s}+R_{ESR}\right)\|R_O}\right] \quad (1)$$

$$A_{BUCK(V.DCM)} \equiv \frac{v_o}{v_{sin}} = \left(\frac{v_{ea}}{v_{sin}}\right)\left(\frac{d_1}{v_{ea}}\right)\left(\frac{t_c}{d_1}\right)\left(\frac{i_1}{t_c}\right)\left(\frac{v_o}{i_1}\right) = \left(G_{EA}R_{EA}\right)\left(\frac{1}{V_{IN}}\right)\left(\frac{T_{SW}}{D_L}\right)\left(\frac{I_{L(PEAK)}}{T_{SW}}\right)\left[\left(\frac{1}{C_O s}+R_{ESR}\right)\|Z_{LO}\|R_O\right] \quad (2)$$

$$A_{BUCK(I.CCM)} \equiv \frac{v_o}{v_{sin}} = \left(\frac{v_{ea}}{v_{sin}}\right)\left(\frac{i_{l(peak)}}{v_{ea}}\right)\left(\frac{v_o}{i_{l(peak)}}\right) = \left(G_{EA}R_{EA}\right)\left(\frac{1}{R_{SENSE}}\right)\left[\left(\frac{1}{C_O s}+R_{ESR}\right)\|Z_{LO(I)}\|R_O\right] \quad (3)$$

$$A_{BUCK(I.DCM)} \equiv \frac{v_o}{v_{sin}} = \left(\frac{v_{ea}}{v_{sin}}\right)\left(\frac{i_{l(peak)}}{v_{ea}}\right)\left(\frac{i_1}{i_{l(peak)}}\right)\left(\frac{v_o}{i_1}\right) = \left(G_{EA}R_{EA}\right)\left(\frac{1}{R_{SENSE}}\right)\left(\frac{T_C}{T_{SW}}\right)\left[\left(\frac{1}{C_O s}+R_{ESR}\right)\|Z_{LO(I.DCM)}\|R_O\right] \quad (4)$$

$$A_{BOOST(I.CCM)} \equiv \frac{v_o}{v_{sin}} = \left(\frac{v_{ea}}{v_{sin}}\right)\left(\frac{i_{l(peak)}}{v_{ea}}\right)\left(\frac{v_o}{i_{l(peak)}}\right) = \left(\frac{G_{EA}R_{EA}}{1+R_{EA}C_{EA}s}\right)\left(\frac{1}{R_{SENSE}}\right)\left[\left(\frac{1}{C_O s}+R_{ESR}\right)\|Z_{LO(I)}\|R_O\right]D_L\left(1-\frac{L_O s}{D_L{}^2 R_O}\right) \quad (5)$$

TABLE I. SIMULATED SYSTEM PARAMETERS AND POLE–ZERO LOCATIONS.

		Ckt	Mode	I_O	R_{ESR}	R_O	C_{EA}	V_{IN}/V_O	f_{0dB}	$p_{L/C}$ or p_C	p_{EA}	z_{ESR}	z_D
L_O	5µH	Buck	V-CCM	200mA	318mΩ	100Ω	10nF	4V/1V	3kHz	22.5kHz	53Hz	50kHz	N/A
C_O	10µF		V-DCM	10mA			10pF		50kHz	436Hz	53kHz	50kHz	
G_{EA}	200µS		I-CCM	200mA			10pF		100kHz	1.05kHz	53kHz	50kHz	
R_{EA}	300kΩ		I-DCM	10mA			10pF		15kHz	436Hz	53kHz	50kHz	
f_{SW}	1MHz	Boost	I-CCM	10mA	100mΩ	5Ω	10nF	1.6V/2V	1.3kHz	3.56kHz	53Hz	160kHz	46kHz