Minimizing MOSFET Power Losses in Near-field Electromagnetic Energy-harnessing ICs

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Abstract—The value of distributed sensors, embedded biomedical implants, and other wireless microsystems is the information they collect, process, and transmit over time. Unfortunately, powering such tiny devices for extended periods is a major challenge because miniaturized batteries cannot store sufficient energy and connecting wires to recharge the batteries demands considerable space overhead. Electromagnetically coupling energy to recharge these devices wirelessly is possible, but practical only if power losses are low enough for sufficient energy to reach the batteries. Because small inductors capture little energy, minimizing the power that switches dissipate to energize and de-energize an inductor is critical. This paper presents how transmitted power changes with distance and, as a result, with inductive coupling factor $k_C$, and shows how to use that information to minimize the power lost in the interconnecting MOSFETs. This way, a 0.18-µm near-field electromagnetic energy-harnessing IC loses on average (in simulations) 3 µW across $k_C$’s ranging from 0.01 to 0.1, which roughly represents 3.9% of the total power transferred.

Keywords—Inductive (Electromagnetic) Coupling, Inductive Power Transfer, Wireless Power Transfer, Contactless Charging

I. POWERING MICROSYSTEMS WIRELESSLY

The power that modern wireless microsensors require to collect, store, process, transmit, and receive data [1]–[3] taxes a tiny battery to such an extent that lifetime is relatively short [4]–[5]. Functional and size requirements are the fundamental limits in this regard, because the implied energy demands of the former exceed the imposed supply capabilities of the latter. Harvesting energy from heat, vibrations, light, and/or radiation is therefore appealing, but not yet a reality for many applications because miniaturized state-of-the-art transducers cannot convert sufficient ambient energy into the electrical domain to energize a microsystem across extended periods [6].

Coupling electromagnetic (EM) energy wirelessly from a highly energized (i.e., "hot") source across a few centimeters, as Fig. 1 illustrates, can supply more power than tiny modern-day transducers generate because hand-held products are sufficiently large to house and radiate considerably more energy. The near-field EM link established, in fact, can also sustain data transmission via backscattered signals. What is more, if power losses are sufficiently low, not only can the link energize the device but also recharge its battery so the system can continue to operate between interrogations (i.e., recharge cycles). This way, a microsensor on a carton of milk can track and report temperature history collected during transport and storage to ensure the cashier does not sell spoiled milk.

Unfortunately, geometric reductions in the receiving coil ($L_S$ in Fig. 1) decrease the magnetic flux $L_S$ perceives, which means EM coupling factor $k_C$ also decreases [7]. In other words, when placed across the same distance ($d_X$) and compared to a larger device, a smaller $L_S$ receives less power [8]. As a result, as transmitted near-field EM power decreases with miniaturization, the power that switches dissipate to transfer and condition power become more significant. To understand this, Sections II – IV describe how (i) a circuit harnesses coupled EM energy, (ii) switches dissipate power, and (iii) $k_C$ affects switch losses. Section V then shows and validates (with simulations) how to size MOSFETs to minimize switch losses. Section VI ends with conclusions.

II. HARNESSING ELECTROMAGNETIC ENERGY

As Fig. 2 illustrates, an ac (primary) source $v_P$ in the interrogator of Fig. 1 drives alternating current through a coupling capacitor $C_P$ and into an emanating (primary) coil $L_P$ so $L_P$ can generate an EM field from which the receiving (secondary) coil $L_S$ can draw power. The changing magnetic flux induces a secondary EM force voltage $v_{EMF_S}$ in $L_S$ that

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increases with coupling factor $k_C$ (i.e., decreasing coil distance), inductances $L_P$ and $L_S$, and the energy supplied by the ac source in the form of changes in current. The power conditioner then establishes the circuit paths necessary to energize (from $v_{EMF.S}$) and de-energize $L_S$ into battery $V_{BAT}$.  

As an example, the power-conditioning charger in Fig. 3 energizes $L_S$ from $v_{EMF.S}$ across its positive half-cycle by engaging switches $M_{END}$ and $M_{EPD}$. Once the half-cycle ends, $M_{END}$ opens and diode-switch $S_{PD}$ conducts $i_L$ into $V_{BAT}$. At this point, $v_{SW}$ is a diode above $V_{BAT}$, so comparator $C_{PPD}$ quickly closes $MPD$ to steer all of $i_L$ through $M_{PD}$ into $V_{BAT}$.

Fig. 3. Near-field electromagnetic energy-harnessing charger IC.

Similarly, $M_{END}$ and $M_{EPD}$ close through the negative half-cycle, $L_S$ energizes to $0.5L_S$ across $V_{EMF.S}$'s peak-peak voltage and $f_0$ is $v_P$'s oscillating frequency, which for maximum power transfer, should match $C_P$–$L_S$'s resonant frequency.  

III. MOS SWITCH LOSSES

Power conditioners consume (i) conduction power $P_C$, across series resistances and diodes in $i_L$'s conduction path, (ii) gate-drive power $P_G$ to charge and discharge gate and other parasitic capacitances, and (iii) quiescent power $P_Q$ to operate functional circuits in the system. The circuit in Fig. 3, for example, loses $P_C$ in $M_{END}$, $M_{PD}$, $D_{PD}$, $M_{EPD}$, $M_{ND}$, $D_{ND}$, and $R_S$; $P_G$ in charging and discharging the gates of $M_{END}$, $M_{PD}$, $M_{EPD}$, and $M_{ND}$; and $P_Q$ in $C_{PD}$ and $C_{ND}$. For one, depends on how frequent the circuit switches state, which means $P_C$ increases with $f_0$. Only power lost in the conduction path ($P_C$) depends on the energy transferred across the coils, so $P_C$ rises with $k_C$. And because power switches consume $P_C$ and $P_G$, $P_C$ and $P_G$ vary with MOS width and length dimensions $W$ and $L$. As a result, minimizing power in the power stage amounts to choosing $W$ and $L$ values that optimally balance $P_C$ and $P_G$ in light of a wide-ranging $k_C$.  

A. Conduction Losses $P_C$

Inductor current $i_L$ in Fig. 3 flows to either energize or de-energize $L_S$. $L_S$'s $R_S$, $M_{END}$, and $M_{EPD}$ conduct $i_L$ when $L_S$ energizes across the majority of the positive and negative half-cycles (i.e., $2\tau_{EN}$ in Fig. 4a–b), so $R_S$ and two n-type channel resistances $2R_{MN}$ consume energizing conduction power $P_{C\cdot EN}$:

$$P_{C\cdot EN} = i_L\cdot\left(\frac{R_S}{2} + R_{MN}\right),$$

where $R_{MN}$ decreases with increasing gate width-to-length aspect ratios $W/L$. Because period $T_O$ is normally $4 – 10 \mu$s and de-energizing $L_S$ only requires a fraction of a microsecond ($\tau_{DE}$), the de-energizing events are, for all practical purposes, instantaneous (i.e., $\tau_{DE}$ is zero) and $T_O$ is just the sum of the two energizing times ($2\tau_{EN}$). As such, $i_L$ can decompose into the $90^\circ$ out-of-phase, $\Delta i_L$ peak-peak square and sinusoidal waveforms of Fig. 4c: $i_{SQ}$ and $i_{SIN}$, so $i_{LEN\cdot RMS}$ reduces to (3/8)$\Delta i_L^2$:

$$i_{LEN\cdot RMS}^2 = i_{SQR\cdot RMS}^2 + i_{SIN\cdot RMS}^2 = \left(\frac{\Delta i_L}{2}\right)^2 + \left(\frac{\Delta i_L}{\sqrt{8}}\right)^2. \tag{3}$$

The circuit has two de-energizing paths into $V_{BAT}$: $M_{EPD}$–$M_{PD}$ for the positive half-cycle and $M_{END}$–$M_{ND}$ for the negative half. Together, both paths dissipate de-energizing power $P_{C\cdot DE}$:

$$P_{C\cdot DE} = i_L\cdot\left(\frac{R_S}{2} + R_{AV} + R_{MP}\right),$$

where $R_{MP}$ is the resistance of a p-type switch, which decreases with increasing $W/L$ aspect ratios, and $i_L\cdot DE\cdot RMS$ is $i_L$'s RMS current across both de-energizing times $2\tau_{DE}$, while $i_L$ traverses rises to and falls from $\Delta i_L$ in triangular fashion:

$$i_{L\cdot DE\cdot RMS}^2 = i_{TR\cdot RMS}^2 = \left(\frac{2\tau_{DE}}{T_O}\right) \cdot \left(\frac{\Delta i_L}{2}\right)^2 \cdot \left(\frac{2\tau_{DE}}{T_O}\right). \tag{5}$$

Note that, while $R_S$ appears in both $P_{C\cdot EN}$ and $P_{C\cdot DE}$, $R_S$ is independent of $W$ and $L$ values, so minimizing MOSFET losses need not account for $R_S$. 

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As explained in Section II, \( CP_{PD} \) and \( CP_{ND} \) require time (\( \tau_{CP} \)) to respond, so \( M_{PD} \) and \( M_{ND} \) do not close until a \( \tau_{CP} \) after \( V_{SW} \) and \( V_{SW} \) rise above \( V_{BAT} \). As a result, \( i_L \) rises \( V_{SW} \) and \( V_{SW} \) at the beginning of their respective de-energizing periods (\( \tau_{DE} \)) to the point \( CP_{PD} \) and \( CP_{ND} \) forward-bias and conduct \( i_L \) into \( V_{BAT} \) across \( \tau_{CP} \). Since \( \tau_{CP} \) is, by design, a small fraction of \( \tau_{DE} \), \( i_L \) is roughly constant across \( \tau_{CP} \) at \( |\Delta i_L| \) and diode power \( P_{CD} \) is

\[
P_{CD} = \Delta i_L V_D \left( \frac{2 \tau_{CP}}{T_o} \right) = \Delta i_D V'_{D} (\tau_{CP} f_o),
\]

where \( V_D \) is \( D_{PD} \) and \( D_{ND} \)'s averaged forward-bias voltage. Note that \( \tau_{CP} \) also includes the delay across \( M_{PD} \) and \( M_{ND} \)'s respective gate drivers, except that portion is negligibly short with respect to \( CP_{PD} \) and \( CP_{ND} \)'s delay. So, because driver delay is both weakly dependent on (i.e., proportional to the logarithm of) gate area [9] and a negligible portion of \( \tau_{CP} \), \( \tau_{CP} \) is practically independent of \( W \) and \( L \) values. Optimally sizing MOSFETs for minimum losses is therefore insensitive to \( P_{CD} \).

\section{Gate-drive Losses \( P_G \)}

Through \( T_{DP} \), each MOSFET in Fig. 3 opens and closes once, so the power the drivers draw from \( V_{BAT} \) to charge their collective gate-load capacitances \( C_G \) across \( V_{BAT} \) is

\[
P_G = C_G V_{D} i_L f_o = 2 W_N L_N + 2 W_P L_P \frac{K_{V_{EMF}} V_{BAT}}{f_o} i_L f_o,
\]

where the \( n \) - and \( p \)-type FETs that comprise \( C_G \) have aspect ratios \( W_N / L_N \) and \( W_P / L_P \). Charging stray capacitances at \( V_{SW} \) also requires energy, which \( L_S \) sources almost losslessly (in resonant fashion). Later, \( L_S \) similarly absorbs the energy supplied to discharge these capacitances. In this process, \( R_S \) is the only component that consumes power, and because these capacitances are relatively small and their energy is correspondingly low, a small \( R_S \) loses negligible power with respect to \( P_G \). Note that charging and discharging this way allow FETs to switch with close to zero voltages across their drain–source terminals, which is why FETs in the circuit incur insignificant \( i_D^2 V_D \) overlap losses.

\section{Effects of Inductive Coupling Factor \( k_C \)}

Since conduction losses \( P_C \), as Section III demonstrates, increase with \( |\Delta i_L| \), which in turn rises with transmitted power \( P_T \) and, as a result, with \( k_C \), balancing \( P_C \) and gate-drive losses \( P_G \) in the FETs must account for \( k_C \). To relate them, consider that, with \( P_T \), \( V_{EMF}^P \) supplies the power \( L_S \) receives as \( P_L \):

\[
P_L = E_s (2 f_o) = 0.5 L_S |\Delta i_L| (2 f_o),
\]

plus the conduction power lost through the energizing process \( P_{CEN} \). \( P_L \) and \( P_{CEN} \)'s dependence on \( |\Delta i_L| \) means \( P_L \) is proportional to \( |\Delta i_L| \) as \( P_T \) would be to \( V_{EMF(SRMS)}^2 \) across an equivalent resistance \( R_{EQ} \) (from Fig. 5):

\[
P_T = P_L + P_{CEN} = \frac{V_{EMF(SRMS)}^2}{R_{EQ}},
\]

where \( V_{EMF(SRMS)}^2 \), as a sinusoid, is

\[
V_{EMF(SRMS)}^2 = \left( \frac{\Delta V_{EMF}}{\sqrt{8}} \right)^2 = \left( \frac{\Delta i_L L_S}{\sqrt{8}} \right)^2 = \left( \frac{2 \pi f_o |\Delta i_L|}{\sqrt{8}} \right)^2
\]

and \( P_T \) combines to

\[
P_T = P_L + P_{CEN} = \left( \frac{1}{2} \right) L_S |\Delta i_L| (2 f_o) + \left( \frac{3}{8} \right) (R_s + 2 R_{MN}) |\Delta i_L|^2, \tag{11}
\]

so \( R_{EQ} \) reduces to

\[
R_{EQ} = \frac{V_{EMF(SRMS)}^2}{P_T} = \frac{(2 \pi f_o L_S)^2}{8 L_S f_o^4 + 3 (R_s + 2 R_{MN})}. \tag{12}
\]

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Fig5.png}
\caption{Circuit with equivalent secondary load resistance \( R_{EQ} \).}
\end{figure}

Because \( C_P \) and \( L_P \), by design, resonate at \( f_o \), their impedances cancel and primary source voltage \( v_p \) drops entirely across source (primary) resistance \( R_P \) and reflected equivalent load resistance \( R_{EQ} \):

\[
R_{EQ} = \frac{v_{EMF(P)} \Delta V_{EMF}}{i_p} = k_L^2 L_P L_S \frac{(2 \pi f_o)^2}{R_{EQ}},
\]

which means

\[
v_{EMF(S)} = k_L \sqrt{L_P L_S} \left( \frac{\Delta i_L}{R_{P} + R_{EQ}} \right) s \tag{14}
\]

and

\[
|\Delta i_L| = \frac{\Delta V_{EMF}}{2 \pi f_o L_S} = \frac{k_c}{\sqrt{L_P L_S}} \frac{\Delta d}{R_P + R_{EQ}}. \tag{15}
\]

where \( s \) is \( j(2 \pi f_o) \) because, even if \( v_p \) were to source power at frequencies other than \( f_o \), \( C_P \) and \( L_P \) would filter that energy, which is why no other power than what \( f_o \) carries reaches \( L_S \). So, substituting this \( \Delta i_L \) back in \( P_{CEN} \) and \( P_{CDE} \) relate these losses to \( k_c \) and since \( L_S \) supplies de-energizing losses \( P_{CDE} \) and \( P_{CDD} \), \( P_L \) already includes \( P_{CDE} \) and \( P_{CDD} \). \( P_T \) does not account for gate-drive losses \( P_{G} \), however, because \( V_{BAT} \) (not \( L_S \)) supplies \( P_G \) to the gate drivers.

\section{Minimizing MOSFET Losses}

As in most switching converters, \( P_T \) and \( P_G \) rise with longer gate lengths because both MOS channel resistance \( R_M \) and gate capacitance \( C_G \) increase. Accordingly, selecting the shortest possible \( L \) that the process and application allow (i.e., \( L_{MIN} \)) is usually the first step in reducing switch losses. Since wider gates lower \( R_M \) (and therefore \( P_C \)) and raise \( C_G \) (and \( P_G \)), the next step in the design process is selecting optimum width dimensions (i.e., \( W_{OPT} \)) with which to minimize \( P_C \) and \( P_G \)'s collective sum. However, just as \( P_C \) changes across loads (i.e., \( \Delta i_L \)) in typical regulators, \( P_G \) varies across \( k_C \) (via \( i_L \) values) in EM-harnessing chargers, which means \( W_{OPT} \) changes with \( k_C \).

Unfortunately, while \( d_k \) is mostly short and \( k_C \) is therefore consistently high in wirelessly powered biomedical implants [3], \( d_k \) is not for most other EM-powered microsystems [1]. As a result, the ideal solution is for MOS widths to vary dynamically according to \( k_C \). However, sensing \( k_C \) (via \( i_L \), for example) and changing widths (by selecting one of several transistor options), require additional power, counteracting and, in
microsystems, oftentimes overwhelming the benefits of $W_{OPT}$. The next best option is to use the most frequent value of $k_C$ to set gate widths, but the approximation is only reasonable with narrow probability distributions, which most applications do not exhibit. A more practical approach is to assume a uniform distribution and choose a width $W_{OPT}$ that optimally minimizes the average power lost in the switches ($P_{AVG}$) across $k_C$:

$$P_{AVG} = \frac{1}{k_{C(MIN)}} \int_{k_{C(MIN)}}^{k_{C(MAX)}} P_{FET} PDF_{FET} dk_C = \frac{1}{\Delta k_C} \int_{k_{C(MIN)}}^{k_{C(MAX)}} P_{FET} dk_C,$$  \hfill (16)

where $P_{FET}$ represents switch losses and $PDF_{FET}$ the corresponding probability-density function, which for a uniform distribution, is constant. When balanced this way, FETs are wider than optimal (i.e., $P_G$ exceeds $P_C$) when $k_C$ is low, optimal (i.e., $P_C$ equals $P_G$) at mid-range, and narrower than optimal (i.e., $P_C$ exceeds $P_G$) when $k_C$ is high, as Fig. 6 shows. In the case of biomedical implants, where $k_C$ is higher more often, widths should favor the high-coupling region, so $P_G$’s crossing point in Fig. 6 should shift to the right.

Since only one n- and one p-type transistor conduct at a time, minimizing $P_{AVG}$ reduces to simultaneously setting $P_{AVG}$’s two first partial derivatives with respect to $W_N$ and $W_P$ to zero:

$$\frac{\partial P_{AVG}}{\partial W_N} = 0 = \frac{\partial P_{AVG}}{\partial W_P}.$$  \hfill (17)

Assuming $k_C$ spans from 0.01 to 0.1 and using 0.18-µm FETs (i.e., $L_{MIN}$ is 0.18 µm) to harness energy from a 4513TC Coilcraft 400-µH secondary coil (L_s) with 9.66 Ω of series resistance ($R_s$) that draws power from a ZXC Coilcraft 14.8-mH primary coil (L_p) to ultimately charge a 0.9 – 1.6-V NiCd from a 0.5-Vpp ac source at 125 kHz ($v_p$), $P_{AVG}$ is lowest when $R_{MIN}$ is 1.02 Ω and $R_{MP}$ is 13.2 Ω, which happens when $W_N$ is 1108 µm and $W_P$ is 368 µm, as Fig. 7 shows. At this point, $P_{AVG}$ is 2.97 µW: 3.91% of the total power transferred (at 3 µW). Ensuring these losses are low is important because microsystems couple only a diminutive fraction of the EM power sourced. Plus, maximizing the energy an embedded battery receives allows the microsystem to function longer between recharge cycles, when there is no EM source.

VI. CONCLUSIONS

As in typical switching converters, minimizing switch losses in near-field EM-harnessing integrated circuits (ICs) reduces to selecting optimal gate widths that balance conduction and gate-drive losses. Unfortunately, this balancing point changes with the distance between the coupling coils and, as a result, with inductive coupling factor $k_C$. Choosing optimal widths must therefore account for $k_C$ and $k_C$’s probability distribution across time. This paper shows how $P_C$ in EM coupling switches depends on $k_C$ and how considering $k_C$’s probability distribution keeps average losses across 0.01 and 0.1 $k_C$ values in 0.18-µm MOSFETs below 4% of the total power transferred.

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