Minimizing MOSFET Power Losses in Near-field Electromagnetic Energy-harnessing ICs

Orlando Lazaro, *Graduate Student Member*, *IEEE*
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, USA
Orlando.Lazaro@ece.gatech.edu

Gabriel Alfonso Rincón-Mora, *Fellow*, *IEEE*
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, USA
Rincon-Mora@gatech.edu

Abstract—**The value of distributed sensors, embedded biomedical implants, and other wireless microsystems is the information they collect, process, and transmit over time. Unfortunately, powering such tiny devices for extended periods is a major challenge because miniaturized batteries cannot store sufficient energy and connecting wires to recharge the batteries demands considerable space overhead. Electromagnetically coupling energy to recharge these devices wirelessly is possible, but practical only if power losses are low enough for sufficient energy to reach the batteries. Because small inductors capture little energy, minimizing the power that switches dissipate to energize and de-energize an inductor is critical. This paper presents how transmitted power changes with distance and, as a result, with inductive coupling factor k_C, and shows how to use that information to minimize the power lost in the interconnecting MOSFETs. This way, a 0.18-µm near-field electromagnetic energy-harnessing IC loses on average (in simulations) 3 µW across k_C's ranging from 0.01 to 0.1, which roughly represents 3.9% of the total power transferred.**

Keywords–Inductive (Electromagnetic) Coupling, Inductive Power Transfer, Wireless Power Transfer, Contactless Charging

I. POWERING MICROSYSTEMS WIRELESSLY

The power that modern wireless microsensors require to collect, store, process, transmit, and receive data [1]–[3] taxes a tiny battery to such an extent that lifetime is relatively short [4]–[5]. Functional and size requirements are the fundamental limits in this regard, because the implied energy demands of the former exceed the imposed supply capabilities of the latter. Harvesting energy from heat, vibrations, light, and/or radiation is therefore appealing, but not yet a reality for many applications because miniaturized state-of-the-art transducers cannot convert sufficient ambient energy into the electrical domain to energize a microsystem across extended periods [6].

Coupling electromagnetic (EM) energy wirelessly from a highly energized (i.e., "hot") source across a few centimeters, as Fig. 1 illustrates, can supply more power than tiny modern-day transducers generate because hand-held products are sufficiently large to house and radiate considerably more energy. The near-field EM link established, in fact, can also sustain data transmission via backscattered signals. What is more, if power losses are sufficiently low, not only can the link energize the device but also recharge its battery so the system can continue to operate between interrogations (i.e., recharge cycles). This way, a microsensor on a carton of milk can track and report temperature history collected during transport and storage to ensure the cashier does not sell spoiled milk.

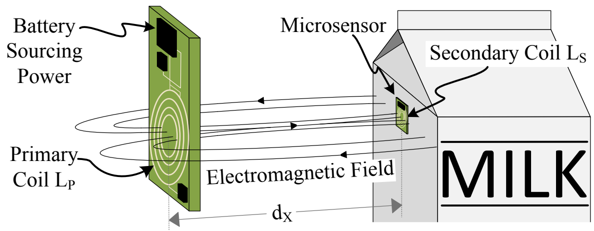
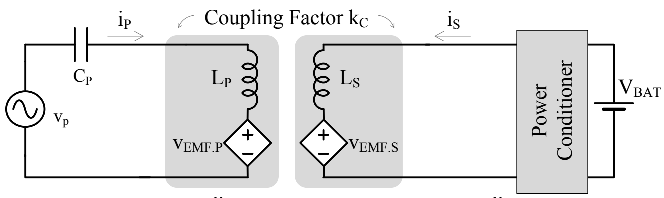


Fig. 1. Coupling electromagnetic energy to power a microsensor wirelessly and recharge its tiny on-board battery.

Unfortunately, geometric reductions in the receiving coil (L_S in Fig. 1) decrease the magnetic flux L_S perceives, which means EM coupling factor k_C also decreases [7]. In other words, when placed across the same distance (d_X) and compared to a larger device, a smaller L_S receives less power [8]. As a result, as transmitted near-field EM power decreases with miniaturization, the power that switches dissipate to transfer and condition power become more significant. To understand this, Sections II – IV describe how (*i*) a circuit harnesses coupled EM energy, (*ii*) switches dissipate power, and (*iii*) k_C affects switch losses. Section V then shows and validates (with simulations) how to size MOSFETs to minimize switch losses. Section VI ends with conclusions.



$$v_{EMF.P} = k_C \sqrt{L_P L_S}\frac{di_S}{dt} \qquad v_{EMF.S} = k_C \sqrt{L_P L_S}\frac{di_P}{dt}$$

Fig. 2. Equivalent circuit model for coupling energy electromagnetically.

II. HARNESSING ELECTROMAGNETIC ENERGY

As Fig. 2 illustrates, an ac (primary) source v_P in the interrogator of Fig. 1 drives alternating current through a coupling capacitor C_P and into an emanating (primary) coil L_P so L_P can generate an EM field from which the receiving (secondary) coil L_S can draw power. The changing magnetic flux induces a secondary EM force voltage $v_{EMF.S}$ in L_S that

Texas Instruments sponsors this research.

increases with coupling factor k_C (i.e., decreasing coil distance), inductances L_P and L_S, and the energy supplied by the ac source in the form of changes in current. The power conditioner then establishes the circuit paths necessary to energize (from $v_{EMF.S}$) and de-energize L_S into battery V_{BAT}.

As an example, the power-conditioning charger in Fig. 3 energizes L_S from $v_{EMF.S}$ across its positive half-cycle by engaging switches M_{END} and M_{EPD}. Once the half-cycle ends, M_{END} opens and diode-switch S_{PD} conducts L_S's energy (via current i_L) into V_{BAT}. This happens because i_L charges the parasitic capacitance at v_{SW}^+ until body diode D_{PD} forward-biases and conducts i_L into V_{BAT}. At this point, v_{SW} is a diode above V_{BAT}, so comparator CP_{PD} quickly closes M_{PD} to steer all of i_L through M_{PD} into V_{BAT}.

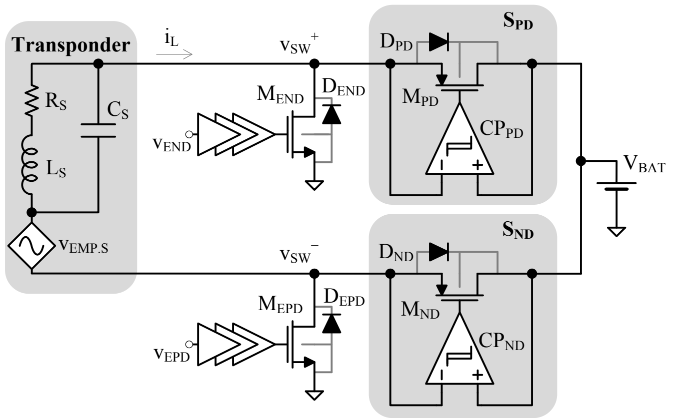


Fig. 3. Near-field electromagnetic energy-harnessing charger IC.

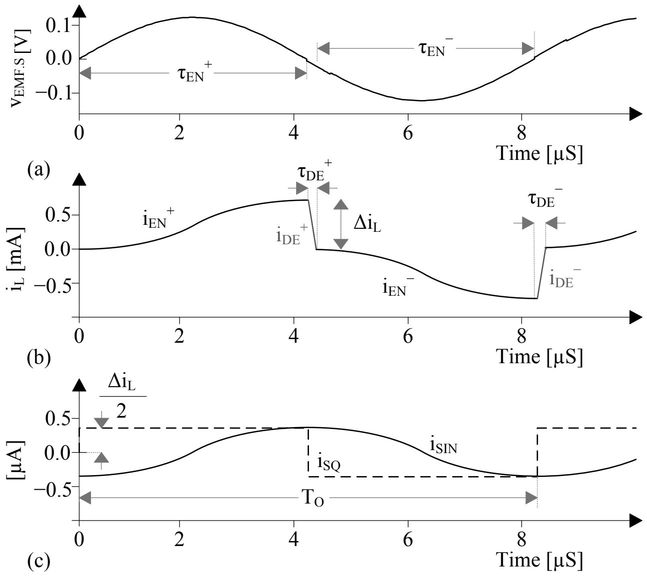


Fig. 4. Simulated (a) $v_{EMF.S}$ and (b) i_L waveforms and (c) i_L's equivalent decomposition into square and sinusoidal currents i_{SQ} and i_{SIN}.

Similarly, M_{END} and M_{EPD} close through the negative half-cycle and M_{EPD} then opens to direct i_L, which now flows in the opposite direction, through diode-switch S_{ND} into V_{BAT}. This way, L_S energizes to $0.5L_S\Delta i_L^2$ through $v_{EMF.S}$'s positive and negative half-cycles (across energizing time τ_{EN} in Fig. 4a), which is to say L_S's current i_L (in Fig. 4b) rises and falls from zero to Δi_L:

$$\Delta i_L = \int_0^{\tau_{EN}} \frac{0.5\Delta v_{EMF.S}\sin(2\pi f_O t)}{L_S}dt \approx \frac{\Delta v_{EMF.S}}{2\pi f_O L_S}. \quad (1)$$

Here, $\Delta v_{EMF.S}$ is $v_{EMF.S}$'s peak-peak voltage and f_O is v_P's oscillating frequency, which for maximum power transfer, should match C_P–L_P's resonant frequency.

III. MOS Switch Losses

Power conditioners consume (*i*) conduction power P_C across series resistances and diodes in i_L's conduction path, (*ii*) gate-drive power P_G to charge and discharge gate and other parasitic capacitances, and (*iii*) quiescent power P_Q to operate functional circuits in the system. The circuit in Fig. 3, for example, loses P_C in M_{END}, M_{PD}, D_{PD}, M_{EPD}, M_{ND}, D_{ND}, and R_S; P_G in charging and discharging the gates of M_{END}, M_{PD}, M_{EPD}, and M_{ND}; and P_Q in CP_{PD} and CP_{ND}. P_G, for one, depends on how frequent the circuit switches state, which means P_G increases with f_O. Only power lost in the conduction path (P_C) depends on the energy transferred across the coils, so P_C rises with k_C. And because power switches consume P_C and P_G, P_C and P_G vary with MOS width and length dimensions W and L. As a result, minimizing power in the power stage amounts to choosing W and L values that optimally balance P_C and P_G in light of a wide-ranging k_C.

A. Conduction Losses P_C

Inductor current i_L in Fig. 3 flows to either energize or de-energize L_S. L_S's R_S, M_{END}, and M_{EPD} conduct i_L when L_S energizes across the majority of the positive and negative half-cycles (i.e., $2\tau_{EN}$ in Fig. 4a–b), so R_S and two n-type channel resistances $2R_{MN}$ consume energizing conduction power $P_{C.EN}$:

$$P_{C.EN} = i_{L.EN(RMS)}{}^2(R_S + 2R_{MN}), \quad (2)$$

where R_{MN} decreases with increasing gate width-to-length aspect ratios W_N/L_N. Because period T_O is normally 4 – 10 μs and de-energizing L_S only requires a fraction of a microsecond (τ_{DE}), the de-energizing events are, for all practical purposes, instantaneous (i.e., τ_{DE} is zero) and T_O is just the sum of the two energizing times ($2\tau_{EN}$). As such, i_L can decompose into the 90° out-of-phase, Δi_L peak-peak square and sinusoidal waveforms of Fig. 4c: i_{SQ} and i_{SIN}, so $i_{L.EN(RMS)}$ reduces to $(3/8)\Delta i_L^2$:

$$i_{L.EN(RMS)}{}^2 \approx i_{SQ(RMS)}{}^2 + i_{SIN(RMS)}{}^2 = \left(\frac{\Delta i_L}{2}\right)^2 + \left(\frac{\Delta i_L}{\sqrt{8}}\right)^2. \quad (3)$$

The circuit has two de-energizing paths into V_{BAT}: M_{EPD}–M_{PD} for the positive half-cycle and M_{END}–M_{ND} for the negative half. Together, both paths dissipate de-energizing power $P_{C.DE}$:

$$P_{C.DE} = i_{L.DE(RMS)}{}^2(R_S + R_{MN} + R_{MP}), \quad (4)$$

where R_{MP} is the resistance of a p-type switch, which decreases with increasing W_P/L_P aspect ratios, and $i_{L.DE(RMS)}$ is i_L's RMS current across both de-energizing times $2\tau_{DE}$, while i_L traverses rises to and falls from Δi_L in triangular fashion:

$$i_{L.DE(RMS)}{}^2 \approx i_{TRI(RMS)}{}^2\left(\frac{2\tau_{DE}}{T_O}\right) = \left(\frac{\Delta i_L}{\sqrt{3}}\right)^2\left(\frac{2\tau_{DE}}{T_O}\right). \quad (5)$$

Note that, while R_S appears in both $P_{C.EN}$ and $P_{C.DE}$, R_S is independent of W and L values, so minimizing MOSFET losses need not account for R_S.

As explained in Section II, CP_{PD} and CP_{ND} require time (τ_{CP}) to respond, so M_{PD} and M_{ND} do not close until a τ_{CP} after v_{SW}^+ and v_{SW}^- rise above V_{BAT}. As a result, i_L raises v_{SW}^+ and v_{SW}^- at the beginning of their respective de-energizing periods (τ_{DE}) to the point D_{PD} and D_{ND} forward-bias and conduct i_L into V_{BAT} across τ_{CP}. Since τ_{CP} is, by design, a small fraction of τ_{DE}, i_L is roughly constant across τ_{CP} at $|\Delta i_L|$ and diode power $P_{C.D}$ is

$$P_{C.D} \approx \Delta i_L V_D\left(\frac{2\tau_{CP}}{T_O}\right) = 2\Delta i_L V_D\left(\tau_{CP} f_O\right), \qquad (6)$$

where V_D is D_{PD} and D_{ND}'s averaged forward-bias voltage. Note that τ_{CP} also includes the delay across M_{PD} and M_{ND}'s respective gate drivers, except that portion is negligibly short with respect to CP_{PD} and CP_{ND}'s delay. So, because driver delay is both weakly dependent on (i.e., proportional to the logarithm of) gate area [9] and a negligible portion of τ_{CP}, τ_{CP} is practically independent of W and L values. Optimally sizing MOSFETs for minimum losses is therefore insensitive to $P_{C.D}$.

B. Gate-drive Losses P_G

Through T_O, each MOSFET in Fig. 3 opens and closes once, so the power the drivers draw from V_{BAT} to charge their collective gate-load capacitances C_G across V_{BAT} is

$$P_G = C_G \Delta v_G f_O = \left(2W_N L_N + 2W_P L_P\right) C_{OX}'' V_{BAT}^2 f_O, \qquad (7)$$

where the n- and p-type FETs that comprise C_G have aspect ratios W_N/L_N and W_P/L_P. Charging stray capacitances at v_{SW}^+ and v_{SW}^- also requires energy, which L_S sources almost losslessly (in resonant fashion). Later, L_S similarly absorbs the energy supplied to discharge these capacitances. In this process, R_S is the only component that consumes power, and because these capacitances are relatively small and their energy is correspondingly low, a small R_S loses negligible power with respect to P_G. Note that charging and discharging this way allow FETs to switch with close to zero voltages across their drain–source terminals, which is why FETs in the circuit incur insignificant i_D–v_{DS} overlap losses.

IV. EFFECTS OF INDUCTIVE COUPLING FACTOR k_C

Since conduction losses P_C, as Section III demonstrates, increase with Δi_L, which in turn rises with transmitted power P_T and, as a result, with k_C, balancing P_C and gate-drive losses P_G in the FETs must account for k_C. To relate them, consider that, with P_T, $v_{EMF.S}$ supplies the power L_S receives as P_L:

$$P_L = E_L\left(2f_O\right) = 0.5 L_S \Delta i_L^2 \left(2f_O\right) \qquad (8)$$

plus the conduction power lost through the energizing process $P_{C.EN}$. P_L and $P_{C.EN}$'s dependence on Δi_L^2 means P_T is proportional to Δi_L^2 as P_T would be to $v_{EMF.S(RMS)}^2$ across an equivalent resistance R_{EQ} (from Fig. 5):

$$P_T = P_L + P_{C.EN} \equiv \frac{v_{EMF.S(RMS)}^2}{R_{EQ}}, \qquad (9)$$

where $v_{EMF.S(RMS)}^2$, as a sinusoid, is

$$v_{EMF.S(RMS)}^2 = \left(\frac{\Delta v_{EMF.S}}{\sqrt{8}}\right)^2 = \left(\frac{\Delta i_L L_S s}{\sqrt{8}}\right)^2 = \left(\frac{2\pi f_O \Delta i_L L_S}{\sqrt{8}}\right)^2 \qquad (10)$$

and P_T combines to

$$P_T = P_L + P_{C.EN} = \left(\frac{1}{2}\right) L_S \Delta i_L^2 \left(2f_O\right) + \left(\frac{3}{8}\right)\left(R_S + 2R_{MN}\right)\Delta i_L^2, \qquad (11)$$

so R_{EQ} reduces to

$$R_{EQ} \equiv \frac{v_{EMF.S(RMS)}^2}{P_T} = \frac{\left(2\pi f_O L_S\right)^2}{8L_S f_O + 3\left(R_S + 2R_{MN}\right)}. \qquad (12)$$

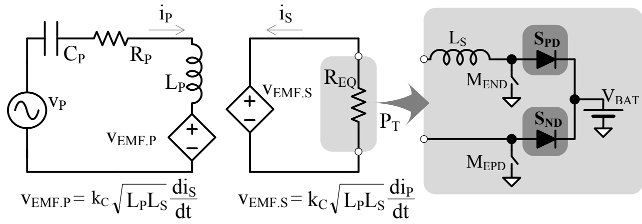


Fig. 5. Circuit with equivalent secondary load resistance R_{EQ}.

Because C_P and L_P, by design, resonate at f_O, their impedances cancel and primary source voltage v_P drops entirely across source (primary) resistance R_P and reflected equivalent load resistance R_{EQ}':

$$R_{EQ}' = \frac{v_{EMF.P}}{i_P} = \frac{k_C^2 L_P L_S \left(2\pi f_O\right)^2}{R_{EQ}}, \qquad (13)$$

which means

$$v_{EMF.S} = k_C\sqrt{L_P L_S}\left(\frac{di_P}{dt}\right) = k_C\sqrt{L_P L_S}\left(\frac{v_P}{R_P + R_{EQ}'}\right)s \qquad (14)$$

and

$$\Delta i_L = \frac{\Delta v_{EMF.S}}{2\pi f_O L_S} = k_C\sqrt{\frac{L_P}{L_S}}\left(\frac{\Delta v_P}{R_P + R_{EQ}'}\right), \qquad (15)$$

where s is $j(2\pi f_O)$ because, even if v_P were to source power at frequencies other than f_O, C_P and L_P would filter that energy, which is why no other power than what f_O carries reaches L_S. So, substituting this Δi_L back in $P_{C.EN}$ and $P_{C.DE}$ relate these losses to k_C; and since L_S supplies de-energizing losses $P_{C.DE}$ and $P_{C.D}$, P_L already includes $P_{C.DE}$ and $P_{C.D}$. P_T does not account for gate-drive losses P_G, however, because V_{BAT} (not L_S) supplies P_G to the gate drivers.

V. MINIMIZING MOSFET LOSSES

As in most switching converters, P_C and P_G rise with longer gate lengths because both MOS channel resistance R_M and gate capacitance C_G increase. Accordingly, selecting the shortest possible L that the process and application allow (i.e., L_{MIN}) is usually the first step in reducing switch losses. Since wider gates lower R_M (and therefore P_C) and raise C_G (and P_G), the next step in the design process is selecting optimum width dimensions (i.e., W_{OPT}) with which to minimize P_C and P_G's collective sum. However, just as P_C changes across loads (i.e., i_L values) in typical regulators, P_C varies across k_C (via Δi_L) in EM-harnessing chargers, which means W_{OPT} changes with k_C.

Unfortunately, while d_X is mostly short and k_C is therefore consistently high in wirelessly powered biomedical implants [3], d_X is not for most other EM-powered microsystems [1]. As a result, the ideal solution is for MOS widths to vary dynamically according to k_C. However, sensing k_C (via i_L, for example) and changing widths (by selecting one of several transistor options), require additional power, countering and, in microsystems, oftentimes overwhelming the benefits of W_{OPT}. The next best option is to use the most frequent value of k_C to set gate widths, but the approximation is only reasonable with narrow probability distributions, which most applications do not exhibit. A more practical approach is to assume a uniform distribution and choose a width W_{OPT}' that optimally minimizes the average power lost in the switches (P_{AVG}) across k_C:

$$P_{AVG} = \int_{k_{C(MIN)}}^{k_{C(MAX)}} P_{FET} PDF_{FET} dk_C \approx \frac{1}{\Delta k_C} \int_{k_{C(MIN)}}^{k_{C(MAX)}} P_{FET} dk_C , \quad (16)$$

where P_{FET} represents switch losses and PDF_{FET} the corresponding probability-density function, which for a uniform distribution, is constant. When balanced this way, FETs are wider than optimal (i.e., P_G exceeds P_C) when k_C is low, optimal (i.e., P_C equals P_G) at mid-range, and narrower than optimal (i.e., P_C exceeds P_G) when k_C is high, as Fig. 6 shows. In the case of biomedical implants, where k_C is higher more often, widths should favor the high-coupling region, so P_C and P_G's crossing point in Fig. 6 should shift to the right.

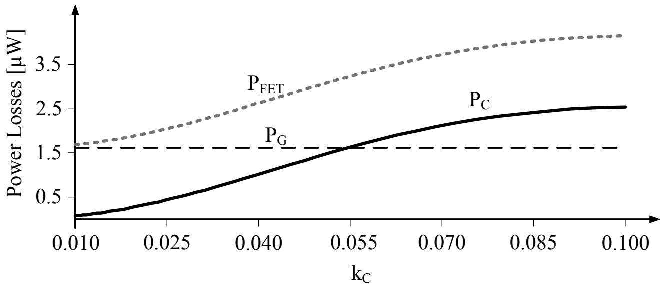


Fig. 6. Simulated conduction and gate-drive losses across coupling factor k_C.

Since only one n- and one p-type transistor conduct at a time, minimizing P_{AVG} reduces to simultaneously setting P_{AVG}'s two first partial derivatives with respect to W_N and W_P to zero:

$$\frac{\partial P_{AVG}}{\partial W_N} \equiv 0 \equiv \frac{\partial P_{AVG}}{\partial W_P}. \quad (17)$$

Assuming k_C spans from 0.01 to 0.1 and using 0.18-µm FETs (i.e., L_{MIN} is 0.18 µm) to harness energy from a 4513TC Coilcraft 400-µH secondary coil (L_S) with 9.66 Ω of series resistance (R_S) that draws power from a ZXC Coilcraft 14.8-mH primary coil (L_P) to ultimately charge a 0.9 – 1.6-V NiCd from a 0.5-V_{PP} ac source at 125 kHz (v_P), P_{AVG} is lowest when R_{MN} is 1.02 Ω and R_{MP} is 13.2 Ω, which happens when W_N is 1108 µm and W_P is 368 µm, as Fig. 7 shows. At this point, P_{AVG} is 2.97 µW: 3.91% of the total power transferred P_T.

VI. CONCLUSIONS

As in typical switching converters, minimizing switch losses in near-field EM-harnessing integrated circuits (ICs) reduces to selecting optimal gate widths that balance conduction and gate-drive losses. Unfortunately, this balancing point changes with the distance between the coupling coils and, as a result, with inductive coupling factor k_C. Choosing optimal widths must therefore account for k_C and k_C's probability distribution across time. This paper shows how P_C in EM coupling switchers depends on k_C and how considering k_C's probability distribution keeps average losses across 0.01 and 0.1 k_C values in 0.18-µm MOSFETs below 4% of the total power transferred (at 3 µW). Ensuring these losses are low is important because microsystems couple only a diminutive fraction of the EM power sourced. Plus, maximizing the energy an embedded battery receives allows the microsystem to function longer between recharge cycles, when there is no EM source.

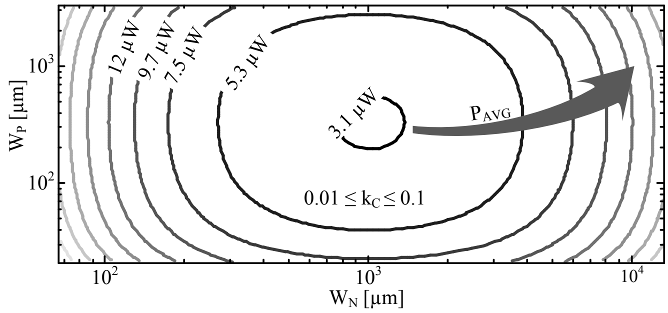


Fig. 7. Simulated k_C-averaged FET losses across W_N and W_P values.

REFERENCES

[1] M.W. Baker and R. Sarpeshkar, "Feedback Analysis and Design of RF Power Links for Low-Power Bionic Systems," *IEEE Trans. Biomed. Circuits and Syst.*, vol. 1, pp. 28-38, 2007.

[2] M. Kiani and M. Ghovanloo, "An RFID-Based Closed-Loop Wireless Power Transmission System for Biomedical Applications," *IEEE Trans. Circuits and Syst. II*, vol. 57, pp. 260-264, 2010.

[3] W. Guoxing, L. Wentai, M. Sivaprakasam, and G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *IEEE Trans. Circuits and Syst. I*, vol. 52, pp. 2109-2117, 2005.

[4] G. Chen, *et al.*, "Circuit Design Advances for Wireless Sensing Applications," *Proc. of the IEEE*, vol. 98, pp. 1808-1827, 2010.

[5] B.H. Calhoun, *et. al.*, "Design considerations for ultra-low energy wireless microsensor nodes," *IEEE Trans. Comput.*, vol. 54, pp. 727-740, 2005.

[6] G. Chen *et al.,* "A cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *in Solid-State Circuits Conf. Dig. of Tech. Papers (ISSCC), 2011 IEEE Int.*, 2011, pp. 310-312.

[7] Y.P. Su, X. Liu, and S.Y.R. Hui, "Mutual Inductance Calculation of Movable Planar Coils on Parallel Surfaces," *IEEE Trans. Power Electron.*, vol. 24, pp. 1115-1123, 2009.

[8] C.-J. Chen, T.-H. Chu, C.-L. Lin, and Z.-C. Jou, "A Study of Loosely Coupled Coils for Wireless Power Transfer," *IEEE Trans. Circuits and Syst. II*, vol. 57, pp. 536-540, 2010.

[9] J. Rabaey, A. Chandrakasan, and B. Nikolic´. *Digital Integrated Circuits.* Upper Saddle River, NJ: Prentice Hill, 2002.

[10] X. Liu and S.Y. Hui, "Simulation study and experimental verification of a universal contactless battery charging platform with localized charging features," *IEEE Trans. Power Electron.*, vol. 22, pp. 2202-2210, Nov. 2007.

[11] H. L. Li, *et al.*, "Optimal coupling condition of IPT system for achieving maximum power transfer," *Electron. Letters,* vol. 45, pp. 76-77, 2009.

[12] S. Guo and H. Lee, "An Efficiency-Enhanced CMOS Rectifier With Unbalanced-Biased Comparators for Transcutaneous-Powered High-Current Implants," *IEEE J. Solid-State Circuits,* vol. 44, pp. 1796-1804, 2009.

[13] P. Li and R. Bashirullah, "A Wireless Power Interface for Rechargeable Battery Operated Medical Implants," *IEEE Trans. Circuits and Syst. II,* vol. 54, pp. 912-916, 2007.

[14] Q. Chen, *et al.*, "Analysis, Design, and Control of a Transcutaneous Power Regulator for Artificial Hearts," *IEEE Trans. Biomed. Circuits and Syst.,* vol. 3, pp. 23-31, 2009.

[15] G. Wang, *et al.*, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 52, pp. 2109-2117, 2005.