LOW VOLTAGE ANALOG CIRCUITS USING STANDARD CMOS TECHNOLOGY

Phillip E. Allen, Benjamin J. Blalock, and
Gabriel A. Rincon
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA 30332-0250

INTRODUCTION

There are many factors that are driving the need to have lower power supply voltages in CMOS integrated circuits. As the channel lengths of CMOS technology decrease, the maximum allowable voltage will decrease. Also, as more components are included in the same area on integrated circuits, the power dissipation increases. Finally, the requirement for portable electronics implies battery operation which favors low voltage and low power circuits. These factors and others have caused many to suggest that future implementation of mixed analog digital circuits using standard CMOS will have power supplies of 1.5V or less [1-2].

An important factor concerning analog circuits is that the threshold voltages of future standard CMOS technologies are not anticipated to decrease much below what is available today [3]. It is necessary that the analog power supply be at least equal to the sum of the magnitudes of the n-channel and p-channel thresholds [4]. This implies that low voltage analog circuits are incompatible with the CMOS technology trends of the future. Ways to circumvent this conflict are to develop technologies with lower thresholds, increase the lower voltage power supply by on-chip dc-dc converter, or develop circuit techniques that are compatible with future standard CMOS technology trends.

This paper focuses on the third approach, developing analog circuit techniques that are compatible with future CMOS technologies. There are several important advantages of this approach. First, the need to develop expensive CMOS technologies with lower threshold voltages is avoided. Secondly, high efficiency dc-dc converters are not required. Thirdly, circuit techniques that permit low voltage operation with large thresholds offer the potential for more fully utilizing the technology at higher voltages and at lower voltages if, in fact, low threshold technologies do become standard technologies.

This paper will briefly review some of the limitations of analog circuits at low voltage. Next, circuit methods of using existing CMOS technology will be described that permit analog circuit operation at low voltages. Each of these methods alone cannot solve the problem but together they offer attractive solutions. One of these methods which is unique with this paper is the channel JFET and its operation and characterization are presented in detail. Next, it is shown how to use these methods to implement analog circuit building blocks such as current sinks/sources, differential amplifiers, and current mirrors. Finally, the blocks are used to build 1V op amps that have been fabricated in standard CMOS technologies having threshold voltages of ±0.8V.

LIMITATIONS OF ANALOG CIRCUITS AT LOW VOLTAGE

There are three key limitations to implementing analog circuits at low voltage. The first and most important is the threshold voltage. The MOSFET must be turned on to be able to perform any type of signal processing. This implies that for CMOS technology that the power supplies must satisfy the following requirement

$$V_{DD} + |V_{SS}| \geq V_{tN} + |V_{tP}| \quad (1)$$

where V_{DD} is the positive power supply, V_{SS} is the negative power supply, and V_{tN} and V_{tP} are the threshold voltages of the NMOS and PMOS transistors, respectively. The threshold voltage limitation also causes a problem in transmission switches. It results in a decreased ON/OFF resistance ratio, particularly in the middle of the power supply range which would normally correspond to analog ground.

The second two limitations are related to the decreased channel length of today and future submicron CMOS technologies. One limitation of submicron technologies is a much larger channel length modulation effect. This results in poor signal gains because the small signal output resistance of the MOSFETs has decreased. The other limitation is lack of good analog models for submicron technology and for low voltage operation. This limitation often causes analog designers to use longer channel lengths than necessary in order to have more reliable models. As a result, the full performance of submicron technologies is not utilized.

The above limitations are summarized below for convenience.

1. Threshold voltage limitations.
2. Channel length modulation caused by submicron technologies.
3. Poor analog modeling of submicron technologies.

In the following section, we will show solutions to the first two limitations. Solutions for the third limitation are beyond the scope of this paper.

METHODS OF ACHIEVING LOW VOLTAGE ANALOG CIRCUITS

Solutions to the Threshold Limitation

The Lateral BJT - The solution to the threshold limitation must remove or circumvent the requirement to provide at least V_t volts to turn on the MOSFET. One possible solution is the lateral BJT [5]. This solution has the added advantage of much less 1/f noise because current flow is in the bulk of the material. However, the lateral BJT requires turn on voltages of 0.6 to 0.7V which do not provide that much advantage over the MOSFET. However, an additional advantage of the lateral BJT is that it has a low

value of $v_{CE}(sat)$ which is also important for low voltage analog circuits.

Subthreshold Operation - A second solution is subthreshold operation of the MOSFET. In this realm of operation, the MOSFET conducts currents at voltages less than the threshold voltage. In addition, the value of $v_{DS}(sat)$ is extremely small. The primary disadvantage of subthreshold operation is small currents and very low frequency response. There does appear to be an important area in which subthreshold operation may provide an impact in low voltage and low power circuits. This area is called *analog VLSI* and uses parallelism to perform cognitive analog signal processing operations [6].

Forward-Biased Bulk-Source - The real solutions to the threshold voltage problem come from an intimate knowledge of the technology, a general principle that has been consistent throughout the history of electronics. Although, the technology cannot be changed, there are ways to use existing technology that provide the desired results on a reliable basis. For example, it is well known that a reverse bias on the well-source junction will cause the threshold voltage to increase. Similarly, a forward bias on this junction will cause the threshold voltage to decrease. The standard relationship used to predict the reverse bias influence is given as

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi - V_{BS}} - \sqrt{2\phi}\right] \qquad (2)$$

where V_{t0} is the value of V_t with $V_{BS} = 0V$, γ is the bulk threshold parameter (volts$^{1/2}$), and ϕ is the strong inversion surface potential (volts) of the MOSFET in the well.

Figure 1 shows the cross-section of an NMOS transistor in a p-well (bulk). The forward biasing of the bulk-source junction can be accomplished by the current source I_B shown in Fig. 1a. This permits floating operation of the MOSFET. Fig. 1b shows the cross-section of the forward-biased bulk-source NMOS and the parasitic vertical BJTs which must be included.

The experimental performance of Fig. 1a is shown in Fig. 2a for an NMOS transistor with W/L = 25µm/2µm. For bulk-source voltages of as much as 0.4V, the threshold voltage can be decreased from 0.75V to around 0.5V. Unfortunately, the bulk current, I_B, is the base current of the vertical NPN BJTs and appears at the drain or source (whichever is at the lower potential) as $(1+ß_F)I_B$ where $ß_F$ is the forward current gain of the vertical NPNs. In addition, a substrate current flows of $ß_F I_B$. Although these currents are dc and $ß_F$ is generally small, they are undesirable. The bulk current remains below 100nA for bulk-source voltages as high as 0.5V

Several observations on the forward-biased, bulk-source operation are important. First, because the threshold is reduced, the value of v_{GS} for the same current is less. Secondly, the noise characteristics are identical whether the bulk-source is forward-biased or not.

The Channel JFET - Probably the most significant solution to the threshold voltage limitation is the channel JFET. Figure 3 illustrates a cross-section of the channel JFET. In this figure a p-well process is assumed. The gate-source potential is taken to a dc voltage that is sufficient to turn the MOSFET on. The drain is connected normally and the signal is applied between the bulk and the source. The current flowing from the source to drain is modulated by the reverse bias on the bulk-channel junction. The result is a junction field-effect transistor with the bulk as the signal input (gate). Consequently, a high-input impedance depletion device that requires no dc bulk-source voltage for current flow results. The impact of this solution is important and discussed in more detail in the next section.

Solutions to the Increasing Channel Length Modulation

The Composite Transistor - One solution that has been successful in alleviating the large channel length modulation and still permit low voltage operation is the composite transistor [7]. The composite transistor is based on the regulated-cascode current sink/source [8]. It consists of a cascode configuration and a series feedback loop that increases the small signal output resistance and yet minimizes the voltage drop across the output of the current sink/source. An NMOS composite transistor schematic and experimental output characteristics are shown elsewhere [14].

Other Approaches - There are other circuit approaches to solving the problem of a large channel length modulation parameter. Most of these approaches use cascoding and require special considerations to avoid a large $v_{DS}(sat)$ [9].

THE CHANNEL JFET

Transconductance Characteristics of the Channel JFET

The channel JFET was introduced briefly above. It was seen to be a MOSFET that is driven from the bulk with a fixed gate-source potential. To understand the channel JFET better, consider the experimental transconductance characteristics shown in Fig. 4. Here we have plotted the drain current versus the bulk-source voltage ($V_{GS} = 1V$) and drain current versus the gate-source voltage ($V_{BS} = 0V$) for four identical transistors located at the same physical location on the chip. Although the W/L is large, smaller values of W/L simply reduce the value of I_{DSS} for the JFET. The channel JFET has the desired reliability because it is not strongly dependent on the parameters of the technology such as diffusion depths and doping levels.

Performance of the Channel JFET

The channel JFET has several important advantages and disadvantages that need to be considered. The obvious advantage is the depletion characteristic which allows zero and even negative values of bias voltage to achieve the desired dc currents. This will lead to larger input common mode ranges that could not otherwise be

achieved. Another advantage of the channel JFET is floating current sources by connecting the bulk to the source resulting in a current of I_{DSS} (V_{GS} will modulate this current which is a disadvantage). Another interesting advantage of the channel JFET is the use of the gate to modulate the channel JFET. Because the gate can totally shut the channel off, the ON/OFF ratio of the channel JFET modulated by the gate is very large. Latch-up does not appear to be a problem as long as the power supply voltages or the currents are low.

The matching of individual channel JFETs is similar to the matching of the MOSFET. Experimental data shows that I_{DSS} varies by ±4.2% and V_P by ±1% amount for the same transistors that K varies by ±2.4% and V_t by ±2.9%. A potential advantage of the channel JFET is that the small signal transconductance, g_{mbs}, can be larger than the MOSFETs transconductance, g_{ms}. This is demonstrated as follows using Eq. (2).

$$g_{mbs} = \frac{di_D}{dv_{BS}} = \left(\frac{di_D}{dv_{GS}}\right)\left(\frac{dv_{GS}}{v_{BS}}\right) = -\left(\frac{di_D}{dv_{GS}}\right)\left(\frac{dV_t}{dv_{BS}}\right) = \frac{\gamma g_{ms}}{2\sqrt{2\phi_F - V_{BS}}} \tag{3}$$

If

$$V_{BS} \geq 2\phi_F - 0.25\gamma^2 \tag{4}$$

then the channel JFET transconductance exceeds the MOSFET transconductance.

Some of the observed disadvantages of the channel JFET are a larger input capacitance because of the well-substrate capacitance. Note that normal MOSFET geometries do not favor an optimum channel JFET from the viewpoint of noise and pinchoff voltage. Also, the bulk-drain and bulk-source capacitance are larger than the gate-drain and gate-source implying that the frequency response will be worse. The output current noise of the channel JFET and MOSFET are identical. Unfortunately, the current flow in the channel JFET is at the surface and does not have the low 1/f noise characteristic of bulk JFETs. Optimum geometrical structures may reduce the excess noise. Another disadvantage is that if the source voltage is not fixed, then the value of gate-source voltage changes and will modulate the characteristics of the channel JFET. In a differential amplifier configuration, this is not a serious problem if the dc value of V_{BS} can change slightly to accommodate V_{GS} changes and maintain the dc current constant.

Modeling the Channel JFET

First-order theory [10] gives the dependence of the drain current, i_D, of a MOSFET as

$$i_D = \frac{K'W}{L}\left(v_{GS} - V_T - \frac{n}{2}v_{DS}\right)v_{DS}\ ,$$

$$v_{DS} \leq v_{DS}(sat) \tag{6}$$

and

$$i_D = \frac{K'W}{2nL}(v_{GS} - V_T)^2\ (1 + \lambda\, v_{DS})\ ,$$

$$v_{DS} \geq v_{DS}(sat) \tag{7}$$

where

$$n = 1 + \frac{C_{BC}}{C_{ox}} + \frac{qNFS}{C_{ox}} = 1 + \frac{g}{2\sqrt{\phi_j - V_{BS}}} \tag{8}$$

and

$$v_{DS}(sat) = \frac{v_{GS} - V_T}{n}\ . \tag{9}$$

The parameters in Eq. (8) are identical with standard SPICE parameters for MOSFETs. However, in bulk-source operation, the gate-source voltage becomes a constant and Eqs. (6) and (7) are re-expressed as

$$i_D = \frac{K'W}{L}\left(v_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - v_{BS}} + \gamma\sqrt{2\phi_F}\,] - \frac{n}{2}v_{DS}\right)v_{DS},$$

$$v_{DS} \leq v_{DS}(sat) \tag{10}$$

and

$$i_D = \frac{K'W}{2nL}\left(v_{GS} - V_{T0} - \gamma\sqrt{2\phi_F - v_{BS}} + \gamma\sqrt{2\phi_F}\right)^2(1+\lambda v_{DS})\ ,$$

$$v_{DS} \geq v_{DS}(sat)\ . \tag{11}$$

These equations have been used for the theoretical predictions of the bulk-driven MOSFET but preliminary indications suggest that they need to be re-examined to permit better correlation between experimental and theoretical results. We have found that the BSIM model [11] can modeling forward-biased bulk-source operation but that one must be extremely careful with other models. The small signal model parameters can be found Eq. (3) for g_{mbs} and the standard formula for g_{ds} of the MOSFET.

LOW VOLTAGE CIRCUITS

Current Sinks/Sources

The composite transistor makes an ideal implementation of a low voltage current sink or source. It can provide dc currents of up to 100µA with a $v_{DS}(sat)$ of 0.2V. Of course, lateral BJTs would also provide an excellent current sink or source. The channel JFET can implement a floating source as long as the requirement of $V_{GS} > V_t$ is satisfied. We will illustrate these sinks/sources in the implementation of a low voltage CMOS opamp.

Current Mirrors

One of the problems with MOSFET or BJT current mirrors is that a significant voltage must be dropped across the input device. If we design the channel JFET so that it is operating with the bulk-source junction slightly forward biased, we can avoid the requirement for this voltage drop.

A n-type version of the proposed low-voltage current mirror is shown in Figure 5 [12]. Note that instead of the gate-drain diode connection used in the standard simple current mirror, this new current mirror has a bulk-drain connection. Also, the bulks of M1 and M2 are tied together rather than the gates. Instead, the gates of M1 and M2 for the n-type version go to the most positive voltage available, V_{DD}. This n-type current mirror can be implemented in CMOS p-well technology.

The small signal input resistance and output resistance of Fig. 5 can be found as

$$r_{in} = \frac{1}{g_{mbs}} = \frac{2\sqrt{2\phi_F - V_{BS}}}{g_{ms}\gamma} \tag{12}$$

and

$$r_{out} \approx \frac{1}{\lambda I_{DS}(sat)} \tag{13}$$

where $I_{DS}(sat)$ is proportional to $V_{GS2} - V_t$. These values are in the same range as gate-driven mirrors.

Current mirrors using both bulk-driven and gate-driven MOSFETs have been designed and fabricated [12]. The results show that the input voltage drop for the bulk-driven mirrors can be much less. For example, at 100µA input current, the value of V_{DS1} for the gate-driven mirror was 1.1V and for the bulk-driven mirror it was 0.1V. The small signal output resistances are approximately the same. The input-output current linearity of the gate-driven mirrors is absent in the bulk-driven mirrors because the input transistor is operating in saturation. However, equations have been derived [12] that permit the prediction of the output current of the bulk-driven MOSFET to within ±15%.

Differential Amplifiers

One of the key building blocks in analog circuits is the differential amplifier. Figure 6 shows the general block diagram with emphasis on low voltage operation. In this case a p-channel differential input pair is assumed. The differential input pair requires a dc current source and the loads are assumed to be dc current sinks. The total power supply voltage, $V_{DD} - |V_{SS}|$ must satisfy

$$V_{DD} - |V_{SS}| \geq \text{ICMR} + V_{DS}(\text{tail}) + V_{ON}(\text{diff. pair}) + V_{DS}(\text{load}) \tag{14}$$

where ICMR is the desired input common mode range (ICMR), V_{DS}(tail) is the tail current voltage headroom, V_{ON} is the turn-on voltage of the differential pair, and V_{DS}(load) is the voltage headroom for the load current sources. If V_{ON} is 0.6V and V_{DS}(tail) and V_{DS}(load) are each 0.2V, the input common mode range would be zero for a 1V power supply. The use of the channel JFET as the differential input pair allows V_{ON} to be 0V allowing an input common mode range of 0.8V for a 1V power supply. Use of the lateral BJTs (PNP in this case) could be used to replace the tail current.

Switches

At low voltages, the transmission gate experiences a "dead zone" in the middle of the power supply range. This dead zone results in higher values of on resistance. Figure 7 shows the experimental switch on resistance as a function of various power supply voltages from 5V to 1.5V. Solutions to the increasing on resistance as the power supply decreases include larger values of W/L, gate overdrive, and forward biasing the bulk-source junction of the switch in the well. Larger values of W/L have limited ability to solve the threshold voltage limitation and increase the feedthrough. Gate overdrives are a practical solution but are difficult to implement at low voltages. Forward biasing the bulk-source junction of the switch in the well during the on state of the switch has some interesting possibilities. From Fig. 1, we know that a current $(ß_F+1)I_B$ will flow in or out of the switch terminals. It turns out that it flows in the terminal that behaves as the source. If this dc current does not influence the operation of the switch, then the solution has merit. It turns out that the dc current does not influence the switch if one of the terminals of the switch is connected to a low impedance point during the on state. If this is the case, then the transmission switches have the potential to function successfully at power supply voltages as low as 1V.

LOW VOLTAGE OP AMPS

All the elements necessary to build CMOS opamps at low voltages have been discussed above. The differential amplifier of Fig. 6 using the channel JFET as the differential input pair and the composite transistors as the tail current source and the current sink loads was used as the input stage. It was found that because of the low output resistance of the output (approximately 300k?), due to the low voltage across the current sinks and sources, that the open loop gain was about 150 under the best conditions.

Characteristics†	Value
Low frequency gain	1000V/V
Unity Gainbandwidth	0.6MHz
Power Dissipation	90µW
Area (2µm Technology)	0.7mm^2
Input Common Mode Range	0.2V to 0.88V
Output Voltage Swing	0.2V to 0.85V
† 1V power supply and 15pF load capacitance.	

Table 1 - Summary of the experimental 1V CMOS op amp performance.

At low power supply voltages, the realizable gain significantly decreases because the high output resistance at higher power supply voltages cannot be achieved. Thus it is necessary to consider a two-stage architecture. Figure 8 shows a classical two-stage architecture. It uses the differential amplifier of Fig. 6 as the input stage with a p-type current mirror to recover the differential gain. The second stage is a class-A amplifier consisting of a p-type composite transistor as the input device and an n-type composite transistor as the current sink load. The Miller compensation capacitor C_C and the nulling resistor R_Z are designed as normal although the lower output resistances of the stage require larger values of C_C.

The current sources of the op amp of Fig. 8 are implemented by composite transistors. The current sink loads actually connect the outputs of the differential-input pair to an internal node of the composite transistor so that the cascode behavior is implemented. The current mirror could be implemented by composite transistors, channel JFETs, or lateral PNP transistors. Composite transistors were selected for simplicity of identical blocks. Several versions of Fig. 8 were implemented in a 2µm n-well and a 2µm p-well process [13]. The experimental performance of this opamp is summarized in Table 1.

CONCLUSIONS AND SUMMARY

This paper has focused on circuit design techniques that would permit the implementation of analog circuits at low power supply voltages in standard CMOS technology. The primary limitations of analog circuits at low voltage are a large threshold voltage, large channel length modulation, and poor analog modeling. The last two limitations are caused by short-channel technology. The best solution to the large channel length modulation problem is the composite transistor or other circuit techniques. The threshold voltage limitation is solved by the lateral BJT, subthreshold operation, forward biasing the bulk-source junction and the channel JFET.

The channel JFET was introduced and seen to be the result of driving the MOSFET from the bulk with the gate-source potential held constant at a value that formed a channel. The depletion characteristics of the channel JFET offered a practical solution for enhancing the input common mode range. The channel JFET has both advantages and disadvantages and has yet to be fully explored. A reality check shows that this behavior could be achieved by one additional mask level in the standard CMOS process. However, the premise of this paper was that the technology would not be modified in any way to accomodate the analog circuits.

The above ideas were applied to low voltage analog circuit building blocks which were used to design a 1V CMOS op amp. This op amp was implemented in a standard CMOS technology having a 2µm minimum channel length and threshold voltages of ±0.8V. The techniques illustrated in this paper have shown how to build analog circuits whose power supply can be as low as 1.25 the threshold voltage of the MOSFETs.

A problem that has not been addressed is the dynamic range. As the power supply is reduced, the noise floor must also be reduced or the dynamic range will be decreased. For these ideas to be useful, ways must be found to maintain the dynamic range as the power supply is reduced.

REFERENCES

[1] A.P. Chandrakasan, S. Sheng, and R.W. Brodersen, "Low-Power CMOS Digital Design," *IEEE JSSC*, Vol. 27, No. 4, pp. 473-484, April 1992.

[2] M. Nagata, "Limitations, Innovations, and Challenges of Circuits and Devices into a Half Micrometer and Beyond," *IEEE JSSC*, Vol. 27, No. 4, pp. 465-472, April 1992.

[3] Chenming Hu, "Future CMOS Scaling and Reliability", *Proc. of the IEEE*, Vol. 81, No. 5, pp. 682-652, May 1993.

[4] P.E. Allen, B.J. Blalock, and G.A. Rincon, "A 1V CMOS Opamp Using Bulk-Driven MOSFET's,," *Proc. 1995 IEEE ISSCC*, Feb. 1995, pp. 192-193.

[5] E. A. Vittoz, "MOS transistors operated in the lateral bipolar mode and their application in CMOS technology, "*IEEE J. Solid-State Circuits*, vol. vol. SC-18, pp. 273-279, April 1983.

[6] E. Vittoz, "Analog VSLI for Perceptive Computing," Plenary talk, Inter. Symposium on Circuits and Systems, Tuesday, May 31, 1994, London.

[7] A. Coban and P. Allen, "A 1.75V rail-to-rail CMOS op amp," *Proc. ISCAS*, 1994, pp. 497-500, May 1994.

[8] E. Sackinger and W. Guggenbuhl, "A High-Swing, High-Impedance MOS Cascode Circuit," *IEEE JSSC*, vol. 25, no.1, pp. 289-298, Feb. 1990.

[9] R. Geiger, P. Allen, and N. Strader, *VLSI - Design Techniques for Analog and Digital Circuits*, McGraw-Hill, New York, NY, 1990.

[10] K. Laker and W. Sansen, *Design of Analog Integrated Circuits and Systems*, McGraw-Hill, Inc., pp. 20-22, 1994.

[11] B.J. Sheu, D.L. Scharfetter and P.K. Ko, "SPICE2 Implementation of BSIM", UCB/ERL M85/42, Engineering Rsearch Laboratory, Univ. of CA, Berkeley, CA.

[12] B.J. Blalock and P.E. Allen, "A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology," submitted to the *Proc. of 1995 ISCAS*, Oct. 1994.

[13] "MOSIS User's Manual," USC Information Sciences Institute, Marina del Rey, CA.

[14] P.E. Allen, B.J. Blalock, and G.A. Rincon, "A "A 1-Volt CMOS op amp using standard CMOS technology,"

Proceedings of the International Solid-State Circuits Conference, pp. , Feb. 1995.

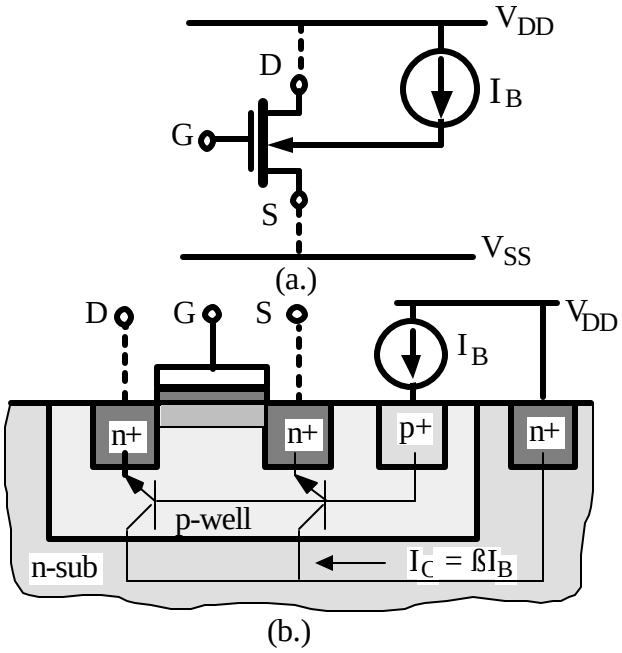

Figure 1 - (a.) Schematic of a forward-biased NMOS transistor. (b.) Cross-section of (a.).

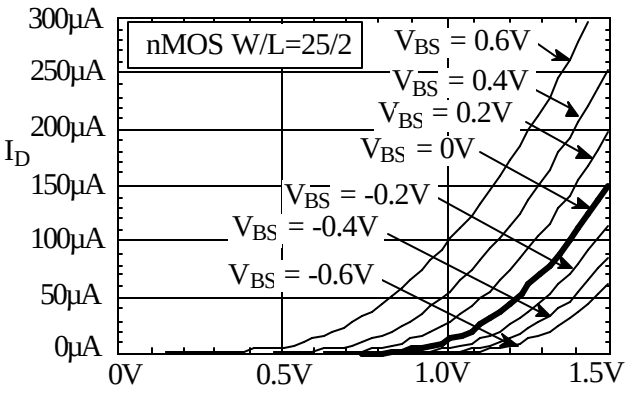

Figure 2 - Influence of a forward bias bulk-source voltage on the transconductance characteristics of a MOSFET.

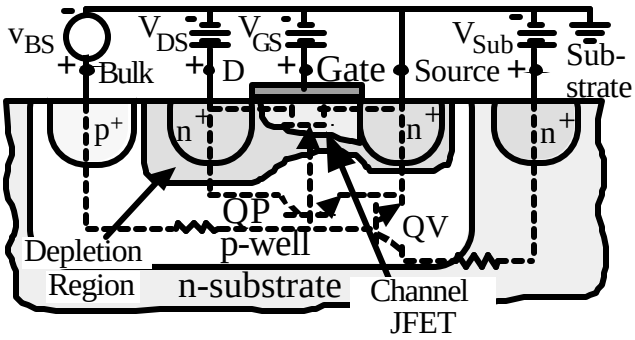

Figure 3 - Cross-section of the channel JFET.

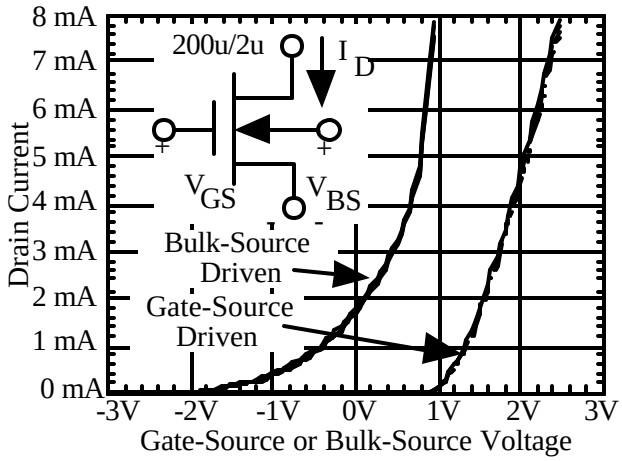

Figure 4 - Experimental linear I_D versus V_{BS} for the channel JFET.

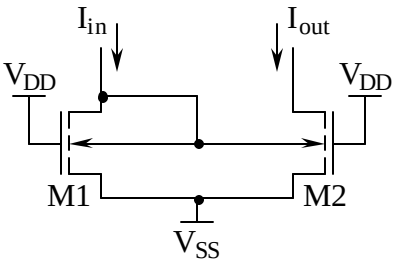

Figure 5 - Simple NMOS, bulk-driven current mirror.

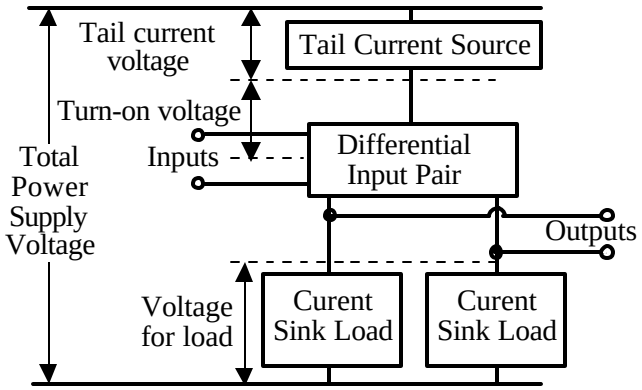

Figure 6 - Block diagram of a low-voltage CMOS differential amplifier.

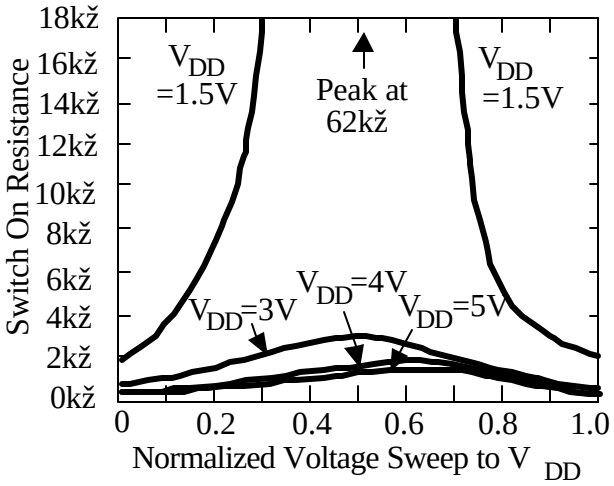

Figure 7 - Experimental switch on resistance as the power supply is decreased.

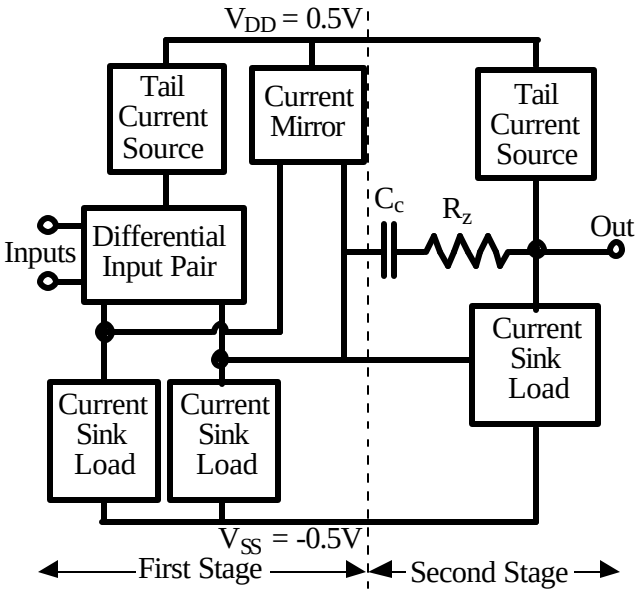

Figure 8 - Block diagram of a two-stage, 1V CMOS op amp.