Fast & Efficient Hysteretic Power Supplies for IoT Microsensors: Analysis & Design with Insight

Tianyu Chang
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, U.S.A.
tchang78@gatech.edu

Gabriel A. Rincón-Mora
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, U.S.A.
Rincon-Mora@gatech.edu

***Abstract*—Integrating and conforming emerging wireless IoT microsensors into tiny form factors is challenging in many ways. To conserve energy, for example, the system should idle whenever possible, activating functional blocks on demand only. Internal power circuits must therefore supply and cut-off power quickly. In the interim, as these react, capacitors supply and sink the mismatch in power. The low capacitance that small capacitors afford, however, cannot supply or sink much power for long. Hysteretic power supplies are appealing in this respect because they respond quickly. But how fast and reliably they respond depends on design, which hinges on understanding. This paper uses and develops insight to explain and analyze the feedback dynamics and stability requirements of hysteretic current-mode dc-dc switched-inductor converters, which are largely abstract and algebraic in literature today. Moreover, this paper also outlines and analyzes possible practical design issues related to IC implementations. To this end, the paper derives accurate and insightful expressions, uses and applies them to a design, and validates them with SPICE simulations.**

Keywords—Hysteretic, switched inductor, dc-dc, power supplies, analysis, design, feedback control, stability, relaxation oscillator, load transient, bandwidth, voltage regulators.

I. Power Supplies for IoT Microsensors

Internet-of-Things (IoT) wireless microsensors can help increase security, convenience, and quality-of-life of our society [1–5]. To save energy, wireless IoT sensors idle mostly, and only execute sensing and transmitting tasks on demand. So, the currents such sensors draw from power supplies soar drastically when they change from idle to full-power mode in microseconds [6–8]. This challenges the power supply in Fig. 1 to respond quickly to any load-dump events.

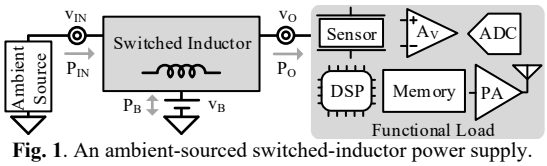

Fig. 1. An ambient-sourced switched-inductor power supply.

Secondly, since wireless IoT sensors idle mostly, they mostly present as very light loads as seen by the power supplies. This challenges a power supply's controller to consume very low quiescent power P_Q to improve light-load efficiency [9–11].

These challenges make hysteretic switched-inductor (SL) power supplies especially appealing, since hysteretic control is fast [9], and may require as little as only one comparator (as this paper will later show), which leads to very little P_Q.

Unfortunately, state-of-the-art (SoA) analyses for hysteretic power supplies are largely abstract and algebraic [12–19]. Moreover, some SoA analyses are established on case-by-case bases [20–21], which means it is usually difficult to extend the same analysis to different converter and control architectures. Lastly, SoA analyses often exclude practical issues in integrated circuit (IC) implementation such as hysteretic comparator propagation delay t_P, offset v_{OS}, and load regulation [12–21].

This work, on the contrary, presents an accurate & insightful analysis on hysteretic current-mode SL dc-dc power supplies. This paper provides expressions on inductor and capacitor selection, and expressions on feedback control design. This proposed analysis can be readily extended to different hysteretic control schemes. It also incorporates t_P, predicts v_{OS} and load regulation, which is crucial for practical IC implementations.

II. Hysteretic Current Mode Control

A. Hysteretic Current Loop

Current Mode: Current mode controls inductor current i_L by the error voltage, so that i_L behaves like a transconductor A_G which is not inductive. Because there is no inductive effect, current mode control removes the complex pole p_{LC} created by L_X and C_O. Hysteretic control sets i_L using the error voltage and removes its inductive effect. Thus, hysteretic control is current mode. The remaining of this section explains how hysteretic control sets i_L and how it could be modeled as an A_G.

Oscillator: A hysteretic loop is a relaxation oscillator. Current sensor β_{IFB} in Fig. 2 senses and translates i_L into voltage v_{IFB}. Hysteretic comparator CP_{HYS} generates gate-drive signal v_G (active-high in Fig. 3) with duty cycle d_E that energizes and drains L_X periodically. During energize time t_E in Fig. 3, CP_{HYS} waits until i_L slews up and v_{IFB} reaches the higher hysteretic bound $v_{T(HI)}$. Once v_{IFB} reaches $v_{T(HI)}$, CP_{HYS} trips so the SL drains i_L into v_O. During drain time t_D, CP_{HYS} relaxes as i_L slews down, until v_{IFB} hits the lower hysteretic bound $v_{T(LO)}$.

Then, CP_{HYS} trips again so the SL energizes i_L again and v_{IFB} once more slews toward $v_{T(HI)}$. v_{IFB}, therefore, oscillates between $v_{T(LO)}$ and $v_{T(HI)}$. Hysteretic window Δv_{HYS} limits the amplitude of v_{IFB} oscillation. This achieves Automatic Gain Control and regulates the oscillator's large-signal positive

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feedback gain to 1 [31]. As a result, the oscillation is stable. Thus, v_{IFB}'s $1/\beta_{IFB}$ translation i_L, also oscillates stably. In ideal scenarios, v_{IR} in Fig. 2 sets $i_{L(AVG)}$, and Δv_{HYS} sets Δi_L.

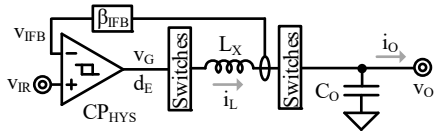

Fig. 2. Hysteretic relaxation oscillator.

Simply put, the hysteretic oscillator forces L_X to conduct an $i_{L(AVG)}$ that is a $1/\beta_{IFB}$ translation of v_{IR}. So, forced by the hysteretic oscillator, i_L behaves likes a transconductanor $A_G = 1/\beta_{IFB}$. Thus, hysteretic control a type of current-mode control.

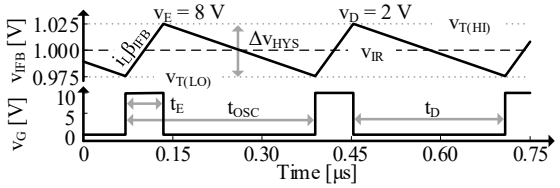

Fig. 3. Simulated hysteretic waveforms without delays.

Offset: Practical comparators have propagation delay t_P [22–23]. As Fig. 4 shows, CP_{HYS} trips a rising delay t_P^+ after v_{IFB} hits $v_{T(HI)}$. CP_{HYS} also trips a falling delay t_P^- after v_{IFB} hits $v_{T(LO)}$. t_P^+ and t_P^- into v_{IFB}'s rate of change incur rising & falling offsets v_{IOS}^+ and v_{IOS}^-. This deviates v_{IFB}'s peak & valley from $v_{T(HI)}$ & $v_{T(LO)}$, as (1) shows.

$$v_{IOS}^{\pm} = t_P^{\pm}\left(\frac{dv_{IFB}}{dt_{E/D}}\right) = t_P^{\pm}\left(\frac{di_L}{dt_{E/D}}\right)\beta_{IFB} = t_P^{\pm}\left(\frac{v_{E/D}}{L_X}\right)\beta_{IFB}, \quad (1)$$

where $v_{E/D}$ is the energize/drain voltage of L_X.

Since t_P^+ and t_P^- offsets i_L and v_{IFB} in opposite directions, half of the difference between v_{IOS}^+ & v_{IOS}^- deviates $v_{IFB(AVG)}$ from v_{IR} as Fig. 4 shows, which consequently, dictates v_{IOS}:

$$v_{IOS} = v_{IFB(AVG)} - v_{IR} = \frac{v_{IOS}^+ - v_{IOS}^-}{2} \approx t_P\left(\frac{v_E - v_D}{2L_X}\right)\beta_{IFB}, \quad (2)$$

where t_P is the propagation delay assuming t_P^+ equals t_P^-, and v_E and v_D are L_X's energize and drain voltages, respectively.

Oscillation Period: t_P alters Δv_{IFB} and thus alters oscillation period t_{OSC}. Since v_{IOS}^+ & v_{IOS}^- stretches Δv_{HYS} in opposite directions, Δv_{IFB} is $(v_{IOS}^+ + v_{IOS}^-)$ larger than Δv_{HYS}, as in (3):

$$\begin{aligned}\Delta v_{IFB} &= v_{IFB(HI)} - v_{IFB(LO)} = \left(v_{T(HI)} + v_{IOS}^+\right) - \left(v_{T(LO)} - v_{IOS}^-\right) \\ &= \Delta v_{HYS} + v_{IOS}^+ + v_{IOS}^- \approx \Delta v_{HYS} + t_P\left(\frac{v_E + v_D}{L_X}\right)\beta_{IFB}\end{aligned}. \quad (3)$$

Since t_E is an energize duty-cycle d_E fraction of t_{OSC}, so t_{OSC} is a reverse d_E translation of t_E. t_E, as Fig. 4 shows, is the time v_{IFB} takes to slew up across Δv_{IFB}, whose slew rate is i_L's slew rate times β_{IFB}. The d_E of an SL can be found in [3], so t_{OSC} is:

$$\begin{aligned}t_{OSC} &= \frac{t_E}{d_E} = \left(\frac{\Delta v_{IFB}}{dv_{IFB}/dt_E}\right)\frac{1}{d_E} = \left[\frac{\Delta v_{IFB}}{\beta_{IFB}(di_L/dt_E)}\right]\frac{1}{d_E} \\ &= \left(\frac{\Delta v_{IFB}}{\beta_{IFB}}\right)\left(\frac{L_X}{v_E}\right)\left(\frac{v_E + v_D}{v_D}\right) = \left(\frac{\Delta v_{IFB}}{\beta_{IFB}}\right)\left(\frac{L_X}{v_E \parallel v_D}\right)\end{aligned}, \quad (4)$$

. The notation $v_E \parallel v_D$ shows that v_E and v_D combine like parallel impedances. As a result, v_E's and v_D's combined voltage is lower than the smaller one between v_E and v_D.

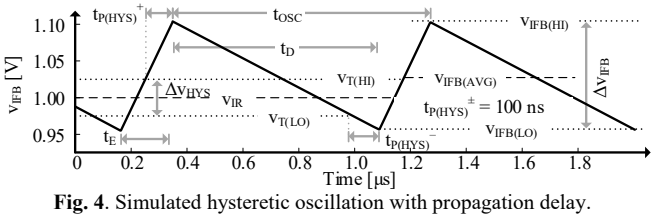

Fig. 4. Simulated hysteretic oscillation with propagation delay.

B. Response Time

When v_{IR} changes abruptly as Fig. 5 shows, $i_{L(AVG)}$ is not able to track v_{IR} since i_L cannot change instantaneously. Therefore, the hysteretic relaxation oscillator should be modeled as a transconductor A_G with delay.

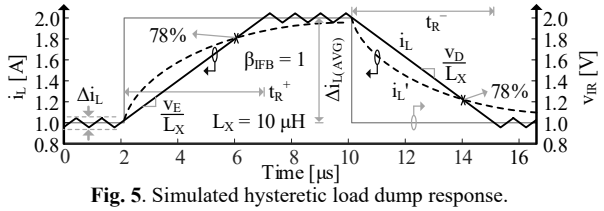

Fig. 5. Simulated hysteretic load dump response.

When v_{IR} steps up, CP_{HYS} trips so the SL keeps energizing L_X and i_L slews up until v_{IFB} rises to the new v_{IR}. The time it takes for i_L to slew up/down across $\Delta i_{L(AVG)} = \Delta v_{IR}/\beta_{IFB}$ sets the rising/falling response time t_R^+ and t_R^- in Fig. 5. $t_R^{\pm}$ is:

$$t_R^{\pm} = \frac{\Delta i_{L(AVG)}}{di_L/dt_{E/D}} = \Delta i_{L(AVG)}\left(\frac{L_X}{v_{E/D}}\right) = \left(\frac{\Delta v_{IR}}{\beta_{IFB}}\right)\left(\frac{L_X}{v_{E/D}}\right). \quad (5)$$

Exponential model i_L' (dashed line in Fig. 5) approximates the delay of i_L from v_{IR}. So based on the approximated i_L', a hysteretic pole p_{HYS} with a time constant τ_{HYS} models the actual $t_R^{\pm}$ in A_G's frequency response as (6) shows:

$$A_G \equiv \frac{i_{L(AVG)}}{v_{IR}} = \frac{A_{G0}}{1 + s/2\pi p_{HYS}} = \frac{1/\beta_{IFB}}{1 + s\tau_{HYS}}. \quad (6)$$

τ_{HYS} is chosen to set i_L' to cross i_L when i_L reaches 78% of its target as Fig. 5 shows. Thus, positive and negative errors between i_L' and i_L match. (7) & (8) calculate τ_{HYS}. $\tau_{HYS}^{\pm}$ are the τ_{HYS} of rising/falling transition, which, may not be equal:

$$78\%\Delta i_{L(AVG)} = \Delta i_{L(AVG)}\left(1 - \exp\frac{-78\%t_R^{\pm}}{\tau_{HYS}^{\pm}}\right), \quad (7)$$

$$\tau_{HYS}^{\pm} = \frac{78\%t_R^{\pm}}{\ln(1 - 78\%)} = \frac{t_R^{\pm}}{1.9} = 52\%t_R^{\pm}. \quad (8)$$

Consequently, the p_{HYS} that produces the response τ_{HYS} sets is:

$$p_{HYS}^{\pm} = \frac{1}{2\pi\tau_{HYS}^{\pm}} \approx \frac{1}{2\pi}\left(\frac{1.9}{t_R^{\pm}}\right) = \frac{1.9}{2\pi}\left(\frac{\beta_{IFB}}{\Delta v_{IR}}\right)\left(\frac{v_{E/D}}{L_X}\right), \quad (9)$$

where $p_{HYS}^{\pm}$ are the p_{HYS} of rising/falling transition, which also, may not be equal.

C. Voltage Loop

Hysteretic current loop (modeled by the A_G) is embedded in the voltage loop formed by error amplifier A_E and voltage feedback β_{VFB} as Fig. 6 shows. A_E sets error voltage v_{EO}. v_{EO} serves the same function as v_{IR} in Fig. 2, which sets $i_{L(AVG)}$ & the average output current $i_{O(AVG)}$, so that v_{FB} nears v_R and v_O nears v_R/β_{VFB}.

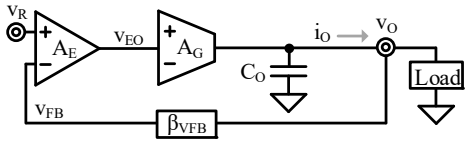

Fig. 6. Hysteretic voltage loop.

Tracing the signal flow around the voltage loop, loop gain A_{LG} is:

$$A_{LG}=\left(\frac{v_{fb}}{v_o'}\right)\left(\frac{v_{eo}}{v_{fb}}\right)\left(\frac{i_{l(avg)}}{v_{eo}}\right)\left(\frac{i_{o(avg)}}{i_{l(avg)}}\right)\left(\frac{v_o}{i_{o(avg)}}\right)=\beta_{VFB}A_EA_GD_OZ_O$$
$$=\beta_{VFB}\left(\frac{A_{E0}}{1+s/2\pi p_{AE}}\right)\left(\frac{1/\beta_{IFB}}{1+s/2\pi p_{HYS}}\right)D_O(R_O\|C_O) \quad ,(10)$$

where A_{E0} and p_{AE} are A_E's dc gain and pole, D_O is the duty-cycle when L_X is connected to output [3], R_O is load resistance and C_O is SL's output capacitor. DC loop gain A_{LG0} is:

$$A_{LG0}=\beta_{VFB}A_{E0}\left(\frac{1}{\beta_{IFB}}\right)D_OR_O\,. \quad (11)$$

Because the L_X-C_O double pole disappears, output pole p_C becomes the dominant pole, and unity gain frequency f_{0dB} is:

$$f_{0dB}\approx A_{LG0}p_C=\frac{A_{LG0}}{2\pi R_OC_O}\,. \quad (12)$$

Placing secondary pole p_{HYS} at f_{0dB} stabilizes the feedback with 45° phase margin. Fig. 7 shows an example with R_O = 100 Ω, C_O = 8.2 µF, & a load dump Δi_O = 500 mA within 1 ns.

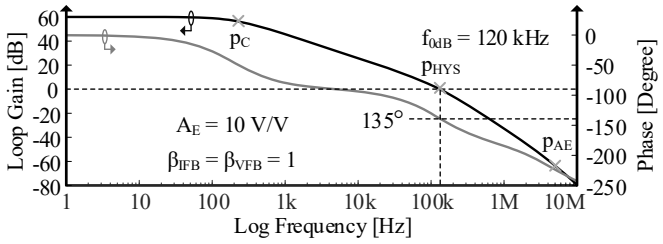

Fig. 7. Calculated voltage loop gain.

Finite A_E offsets v_{FB} from v_R by offset v_{VOS}. So, v_{VOS} is a reverse A_E translation from v_{EO}, as Fig. 6 indicates. Also, non-zero v_{IOS} offsets $v_{IFB(AVG)}$ from v_{EO}, so v_{EO} is a v_{IOS} less than $v_{IFB(AVG)}$. $v_{IFB(AVG)}$ carries information about $i_{L(AVG)}$, which loads the SL and creates load regulation. Therefore, $v_{IFB(AVG)}$ is also called loading effect v_{LD} in this paper, as (13) shows:

$$v_{IFB(AVG)}=i_{L(AVG)}\beta_{IFB}=v_{LD}\,. \quad (13)$$

Consequently, v_{VOS} is:

$$v_{VOS}=\frac{v_{EO}}{A_E}=\frac{v_{LD}-v_{IOS}}{A_E}=\left[i_{L(AVG)}-t_P\left(\frac{v_E-v_D}{2L_X}\right)\right]\left(\frac{\beta_{IFB}}{A_E}\right). \quad (14)$$

D. Contraction

Contracted Loop: Fast A_E adds significant P_Q [24–25] & degrades light-load efficiency. A_E feeds an amplified version of $v_R - v_{FB}$ to CP_{HYS}. So, feeding v_R and v_{FB} directly to CP_{HYS} to form a contracted loop as Fig. 8 shows is the same as setting A_E to 1 since there is no amplification. Since A_E is the only change, this means previous theory still applies.

The benefit of contraction is less P_Q since there is one less amplifier. The drawback is worse load regulation since A_E, which equals one, no longer suppresses v_{IOS} and v_{LD}.

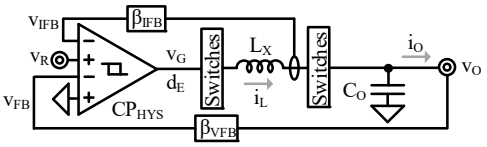

Fig. 8. Contracted hysteretic current-mode voltage loop.

Load Compensation: Canceling the effect of v_{LD} in the voltage loop compensates load regulation of a contracted loop. R_{LD} & C_{LD} in Fig. 9 average v_{IFB} to v_{LD}', so v_{LD}' mimics v_{LD}. So, feeding v_{LD}' and v_{IFB} to the loop with opposite polarity subtracts v_{LD}' from v_{IFB}, which effectively cancels the effect of v_{LD}.

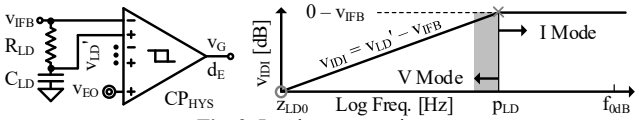

Fig. 9. Load compensation.

For load-compensated hysteretic power supplies, v_{EO} sets $i_{L(AVG)}$. Only the Δi_L information is enough to let CP_{HYS} sustain oscillation such that i_L behaves like A_G. $v_{LD}' - v_{IFB}$, which is called the differential current mode voltage v_{IDI} in this paper, is 0 at dc and rises as frequency rises. Its amplitude flattens out past load-compensation pole p_{LD} as Fig. 9 shows. v_{IDI} only feeds high-frequency Δi_L information to CP_{HYS}, which sustains oscillation, so the i_L behaves like A_G passed p_{LD}. p_{LD} is:

$$p_{LD}=\frac{1}{2\pi R_{LD}C_{LD}}<<f_{0dB}\,. \quad (15)$$

To stabilize the voltage loop, i_L must behave like a trans-conductor before reaching f_{0dB}. This guarantees that p_{LC} never surfaces, & the voltage loop reaches f_{0dB} with one pole. So, p_{LD} must be much less than f_{0dB}. Fig. 10 shows a load compensated contracted loop. Since v_{LD}'s effect is removed, v_{VOS} equals v_{IOS}.

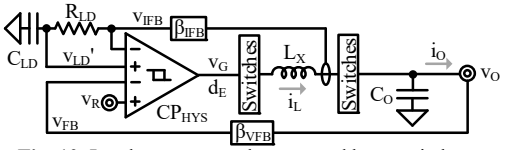

Fig. 10. Load-compensated contracted hysteretic loop.

III. Compact Li-Ion 5-V Design

A. IoT Wireless Microsensors

IoT sensors demand 4.5–5.5 V supply voltage v_O [26–27]. Li-Ion batteries provide SL supplies with 2.7–4.2 V input voltage v_{IN} [28]. The duration t_{XFER} of sensor transfer events is 7–360 ms [6, 29]. IoT sensors can source up to 480 mA from the supply (LL-RXR-27 Transceiver). Maximum response time $t_{R(MAX)}$ is set to 0.1% of $t_{XFER(MIN)}$. Table I lists constraints.

Table I: Design Constraints

Parameter	Value	Parameter	Value	Parameter	Value
$v_{IN(MIN)}$	2.7 V	$v_{IN(MAX)}$	4.2 V	v_R	1.2 V
$v_{O(MIN)}$	4.5 V	v_O	5.0 V	$v_{O(MAX)}$	5.5 V
$t_{XFER(MIN)}$	7 ms	$t_{XFER(MAX)}$	360 ms	$t_{R(MAX)}$	*7 µs
Δv_{HYS}	50 mV	t_P±	20 ns	$i_{O(MAX)}$	480 mA

*Targeting $t_{R(MAX)} = 0.1\% t_{XFER(MIN)}$.

B. Power Stage

Transfer Inductor: The power stage must be a boost since $v_{IN(MAX)}$ is less than $v_{O(MIN)}$. L_X is selected to meet t_R constraints. Worst-case t_R occurs with max $\Delta i_{L(AVG)}$ and

slowest i_L slew. Since $i_{L(AVG)}$ is a reverse D_O translation of i_O, worst-case t_R also occurs with $D_{O(MIN)}$ & $v_{IN(MIN)}$, as in (17).

$$t_R \le \frac{\Delta i_{L(AVG,MAX)}}{\left(di_L/dt_E\right)_{(MIN)}} = \left(\frac{i_{O(MAX)}-0}{D_{O(MIN)}}\right)\left(\frac{L_X}{v_{IN(MIN)}}\right) \le t_{R(MAX)}. \quad (17)$$

Solving (17) gives $L_X < 21$ µH. For miniaturization, the design uses a 3.3-µH 1.0 × 0.6 × 0.6 mm³ L_X (Murata LQ Series).

Output Capacitor: C_O is selected to meet $v_{O(MIN)}$ constraint. Max load dump $\Delta i_{O(MAX)}$ occurs when i_O steps from 0 to $i_{O(MAX)}$. With $t_{R(MAX)}$ and $\Delta i_{O(MAX)}$, v_O should never drop blow $v_{O(MIN)}$. This means C_O's voltage drop Δv_{CO} must be less than:

$$\Delta v_{CO} \le \left(\frac{i_{O(MAX)}-0}{C_O}\right) t_{R(MAX)} \le v_O - v_{O(MIN)}. \quad (18)$$

Solving (18) gives $C_O > 6.7$ µF. For design margin, this work uses a 10-µF 1.0 × 0.5 × 0.5 mm³ C_O (Samsung CL05 Series).

C. Control Design

Frequency Response: in addition to p_C, p_{HYS}, p_{AE}, p_{LD}, and z_{LD0}, SL boost carries right-half-plane (RHP) zero z_{RHP} at [9]:

$$z_{RHP} = \frac{V_O D_O}{2\pi L_X i_{L(HI)}} = \frac{V_O D_O}{2\pi L_X \left(i_{L(AVG)} + 0.5\Delta i_L\right)}. \quad (19)$$

Duty-cycled output is the cause of z_{RHP} [30, 32]. z_{RHP} loses 90° phase, which makes stabilizing the voltage loop challenging.

Stability: $D_{O(MIN)}$ and highest $i_{L(AVG)}$ result in lowest RHP zero $z_{RHP(MIN)}$. Calculated $z_{RHP(MIN)}$ is 140 kHz. Worst-case t_R results in lowest hysteretic pole $p_{HYS(MIN)}$ & calculated $p_{HYS(MIN)}$ is 280 kHz. Placing the lower one of $z_{RHP(MIN)}$ and $p_{HYS(MIN)}$ above f_{0dB} stabilizes the loop with more than 45° phase margin:

$$f_{0dB} = \frac{\beta_{VFB} A_{E0} D_O}{2\pi C_O \beta_{IFB}} \le \min\left\{p_{HYS(MIN)}, z_{RHP(MIN)}\right\}. \quad (20)$$

Assuming an ideal $\beta_{VFB} \approx v_R/v_O = 24\%$, setting $A_{E0} = 50$ V/V as a design choice and choosing $\beta_{IFB} = 1$ Ω satisfies (20).

Offset Correction: Fine-tuning β_{VFB} centers v_O around its target: v_R/β_{VFB}. Targeting mid-way $i_O = 0.5 i_{O(MAX)}$, calculated v_{VOS} is 8.9 mV and calculated β_{VFB} is 23.8% as (21) shows.

$$\beta_{VFB} \equiv \frac{v_{FB}}{v_O} = \frac{v_R - v_{VOS}}{v_O}. \quad (21)$$

IV. Validation

A. Load Dump Response

Simulated i_L & v_O under ± 480-mA 1-ns load dumps are shown in Fig. 11. t_R^+ & t_R^- are 2.1 µs & 1.7 µs. v_O never droops below the 4.5-V $v_{O(MIN)}$, so this design meets the target Table I sets. However, v_O deviates statically by 76 mV across 480-mA load change Δi_O. This translates to 160 mV/A load regulation, which is to be reduced in the next sub-section.

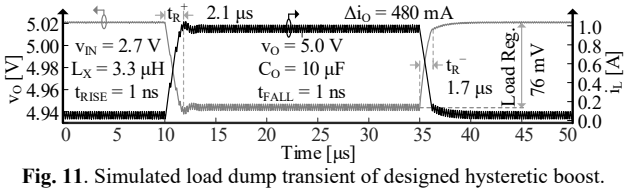

Fig. 11. Simulated load dump transient of designed hysteretic boost.

B. Load Regulation

Load compensator $R_{LD} = 4$ MΩ and $C_{LD} = 4$ pF places p_{LD} at 10 kHz, which is much lower than the calculated f_{0dB} (102 kHz) as (15) requires. To simulate load regulation, i_O rises very slowly from 50 to 500 mA across 9.5 ms as the dash line in Fig. 12 shows. Simulated v_O with & without compensation are shown as solid black and grey in Fig. 12. Without compensation, v_O drops from 5.02 V to 4.94 V, which agrees with Fig. 11. With compensation, v_O's average hardly drops.

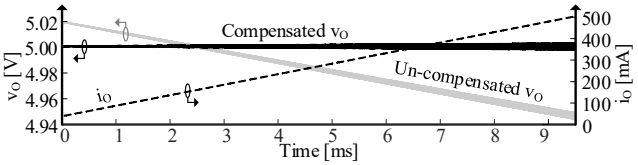

Fig. 12. Simulated load regulation with & without compensation.

v_O's ripple $\Delta v_{O(AC)}$ rises from 0.7 mV to 5.4 mV as i_O rises. With a Δi_O of 480 mA, v_O's error $\Delta v_{O(LD)}$ is about 80 mV. Table II lists performances of the designed hysteretic supply.

TABLE II: PERFORMANCE

Name	Value	Name	Value	Name	Value	Name	Value
v_{IN}	2.7 V	v_O	5.0 V	t_{SW}	4.7 MHz	Δi_O	480 mA
$\Delta v_{O(AC)}$	0.7–5.4 mV	$\Delta v_{O(LD)}$	80 mV	L_X	3.3 µH	C_O	10 µF
t_R^+	2.1 µs	t_R^-	1.7 µs	$i_{O(MAX)}$	500 mA	–	–

C. SoA Comparison

This analysis is applicable to a generic power stage given its frequency response (which can be found in [30]), unlike analyses in [20–21] that are only applied to SL bucks. This analysis is also applicable to different control schemes, like contracted and load-compensated loops.

This analysis includes IC design issues, such as t_P, v_{VOS}, v_{IOS}, and the resulting load regulation. Since analyses in [12–21] assume ideal control loops, so only the proposed analysis provides more complete insights & guidance on designing IC-level hysteretic SL power supplies.

Valuable analyses in [12–19] are based strictly on non-linear control theory, which make them very solid & thorough. In addition to the SoA, the proposed analysis hinges on insights and provides straight-forward expressions on L_X, C_O, A_{E0}, β_{VFB}, β_{IFB}, R_{LD}, and C_{LD} that set IC designers ready for practical chip-level implementations.

V. Conclusions

This paper presents an insightful IC-design oriented analysis on hysteretic current-mode switched-inductor (SL) power supplies. The fundamental attribute of this analysis is realizing that a hysteretic loop is fundamentally a relaxation oscillator and should be modeled using a transconductor with one pole. The proposed analysis applies to a generic SL power stage and incorporates practical IC design concerns that are mostly absent in prior analyses (i.e., propagation delay, current and voltage offset, contraction, and load compensation). With straight-forward expressions, this analysis guides the design on inductor and capacitor selection, error amplifier gain, voltage and current feedback factors, and load compensators, and prepares IC designers with a ready-to-use workflow.

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