Power-Conversion Efficiency: Loss Dominance, Optimization, & Design Insight

Guillaume Guérin, *Graduate Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Fellow, IEEE*

***Abstract*—Power-conversion efficiency is critical in power supplies. Switched inductors are popular in this space because they can deliver a large fraction of the power they draw. This fraction hinges on the power that switches, diodes, resistances, and capacitances need to conduct and transfer power to the output. So, understanding how these loss mechanisms set and dictate efficiency across power levels is important, especially when designing and targeting particular load levels. This article details how these losses scale, when they dominate, and how and when they balance. Gate drive and controller losses are the ones that become a smaller fraction of input power as output power increases, leading to the increase of the power efficiency at the low-end of discontinuous conduction scale, while only gate charge loss plays this role at the low-end of the continuous conduction scale. Ohmic loss is the one that reduces power efficiency at the high-end of discontinuous and continuous conduction scale as ohmic loss becomes a larger fraction of input power as output power increases. Power efficiency peaks in continuous conduction when ohmic loss and gate charge losses balance. Overlap and dead time losses, although still important, do not shape the power efficiency in continuous conduction mode. In discontinuous conduction mode, all losses play a role and efficiency peaks when they all trickily balance. With this insight, predicting and controlling when efficiency rises, peaks, and falls across loads are possible. The fractional loss analysis and the design insight that make this possible are new contributions to the state of the art.**

***Index Terms*—Switched inductor, power efficiency, interpretation, fractional losses, loss dominance, optimization, design insight, peak efficiency.**

I. Power Supplies

Power supplies are everywhere nowadays. The rise of connected devices and systems known as the Internet-of-Things requires power supplies to be always more efficient and more versatile. Switched-inductor power supplies are pervasive in electronic systems because they output a large fraction of the power they draw from their inputs. The main reason for this is that the voltage that switches drop are a very small fraction of the output voltage. So, the inductor current usually delivers more power by design into the output than switches consume. Still, the heat that burning power generates can compromise electronic performance and mechanical integrity [1]. Also, losing battery energy or ambient power to the power supply reduces the charge life or functionality of a system.

Power-conversion efficiency η_C is the fraction of input power P_{IN} that the input v_{IN} delivers to the output v_O in Fig. 1. The load can be composed of Analog-to-Digital Converter (ADC), Digital Signal Processing microcontrollers (DSP), Digital-to-Analog Converter (DAC), voltage amplifiers, Power Amplifier (PA), and Sensors for instance. Internet-of-Things is a very good example of the diversity of a load.

Power efficiency η_C has to be as high as possible for several reasons. DC-DC converters can be found after an AC-DC converter, and therefore have to maintain a high rating. Losses occurring within the power supply also create heat difficult to cool down, thus limiting the power that can be delivered to the load. On top of heat, embedded systems, such as Internet-of-Things, which are often powered by batteries which provide only a limited amount of energy, cannot afford to lose too much power in losses.

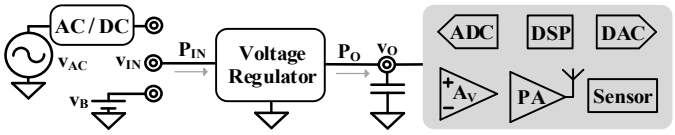

Fig. 1. Electronic system with power supply and load.

P_{IN} also supplies power losses P_{LOSS}. So, P_O outputs the difference P_{IN}– P_{LOSS}, fractional loss σ_{LOSS} is the fraction of P_{IN} lost in P_{LOSS}, and η_C is below 100% by the amount σ_{LOSS} sets. Thus, understanding the nature, makeup, and sensitivity of these losses is important.

Majority of state-of-the-art papers do not consider all kinds of losses: [2] ignores gate drive loss, while [3] and [4] do not consider dead time loss. [5]—[9] do not take into account IV overlap loss nor dead time loss. Some others don't even break down losses to analyze the losses significance and distribution across output power [10]—[27]. Moreover, none of state-of-the-art papers offer a fractional losses-oriented approach to break down and analyze power efficiency across output power. The contribution of this paper is an insightful losses and power efficiency analysis, allowing designers to predict when efficiency rises, peaks and falls across output power. This paper is organized as follows: Section II describes losses mechanisms, while Section III gives an insight about fractional losses and power efficiency. Section IV presents an example with a synchronous buck voltage regulator, Section V presents the significance of the analysis derived, and Section VI concludes the paper.

II. Loss Mechanisms

Many different kinds of losses contribute to reduce overall power efficiency. Fig. 2 shows a schematic of a buck-boost, with parasitic components. The most fundamental of these is conduction power. This is the power that components consume when they conduct inductor current. Series resistances (R_L and R_C in Fig. 2), transistors (M_{EI}, M_{DG}, M_{DO}

and M_{EG}, leading to ohmic losses P_R), and body diodes (D_{D1} and D_{D2}, leading to dead-time loss P_{DT}) are to blame for this.

Another loss is the power P_C that gate drivers need to transition switches between states. Stray capacitances C_{SW} at switching nodes leak power, included in P_{SW}. Switching mechanisms of hard-switched MOSFETs (M_{EI} and M_{EG} in Fig. 2) lead to overlap loss P_{IV}. Finally, controller burns power P_Q due to its quiescent current.

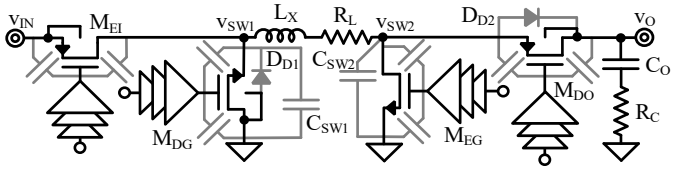

Fig. 2. CMOS switched-inductor power supply.

A. Discontinuous Conduction Mode

Loss expression actually depends on the regime of operation of the converter, if it is operating in continuous conduction mode (CCM), or discontinuous conduction mode (DCM). In DCM, energy packets are periodically delivered to the load. During energizing time, current rises in the inductance, and during draining time, inductor current drops, until it reaches zero at the end of the draining time. Energizing time and draining time define conduction time t_C, which is shorter than a switching period compared to CCM, as Fig. 3 illustrates. Regime of conduction changes loss expressions, but it also changes their dependency with output current, as Table I shows [26], [28]. C_{EQ} is the equivalent capacitance at the gate of a switch, and Δv_{EQ} is the equivalent voltage seen by this capacitance. t_I and t_V are the rising and falling times of the current and the voltage across the switch. When a switch closes or opens, it sees a voltage v_{SW} across it. During dead time t_{DT}, body diode drops a voltage v_{DG} while conducting. In DCM, inductor series resistance R_L and switches channel resistance R_{CH} burn ohmic power, while in CCM ohmic losses can be broken down into AC and DC losses through equivalent DC resistance R_{DC} and equivalent AC resistance R_{AC}. Controller consumes quiescent current $i_{Q(AVG)}$.

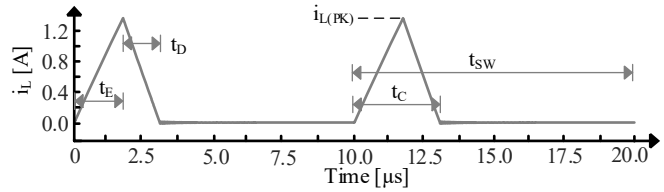

Fig. 3. Inductor current i_L in discontinuous conduction mode.

TABLE I. Losses expressions.

	DCM	CCM	
P_C	$v_{IN}C_{EQ}\Delta v_{EQ}f_{SW} \propto {i_O}^0$		
P_{IV}	$i_{L(PK)}v_{SW}t_{I/V}f_{SW} \propto {i_O}^{0.5}$	$\left(\frac{i_O}{d_{DO}}\right)v_{SW}t_{I/V}f_{SW} \propto {i_O}^1$	
P_{SW}	$C_{SW}f_{SW}\left(2{v_{DG}}^2 + 0.25{v_{IN}}^2 + v_{IN}v_{DG}\right) \propto {i_O}^0$		
P_{DT}	$i_{L(PK)}v_{DG}t_{DT}f_{SW} \propto {i_O}^{0.5}$	$2i_Ov_{DG}t_{DT}f_{SW} \propto {i_O}^1$	
P_R	$R_{L/CH}\left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2\left(\frac{t_C}{t_{SW}}\right) \propto {i_O}^{1.5}$	$P_{R(DC)}$	$R_{DC}\left(\frac{i_O}{d_{DO}}\right)^2 \propto {i_O}^2$
		$P_{R(AC)}$	$R_{AC}\left(\frac{0.5\Delta i_L}{\sqrt{3}}\right)^2 \propto {i_O}^0$
P_Q	$i_{Q(AVG)}v_{IN} \propto {i_O}^0$		

Fig. 4 below shows losses evolution across output power for a 1.8 V to 1 V buck voltage regulator operating in DCM, with their relative dependency with output current. In order to optimize losses depending on the regime of conduction, some techniques can be used, such as reducing MOSFETs' widths and switching frequency in DCM [9]. As the inductor current is lower in DCM, ohmic losses are lower, so MOSFETs' widths can be lowered to reduce gate charge loss P_C. P_C can be further reduced by reducing f_{SW}.

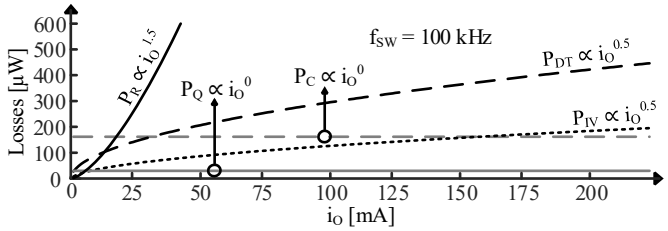

Fig. 4. Power losses across output current in DCM.

B. Continuous Conduction Mode

In CCM, there is always current flowing through the inductor, either energizing it, or draining it. The current in the inductor never reaches zero, as Fig. 5 illustrates.

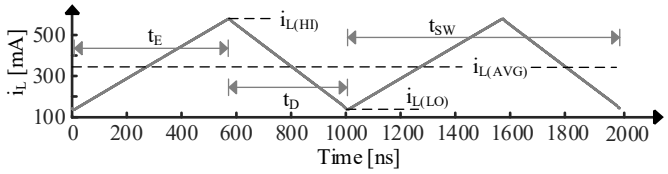

Fig. 5. Inductor current i_L in continuous conduction mode.

Losses distribution and their relative dependency with output current change when the converter operates in CCM. Fig. 6 shows this distribution. In Fig. 6, switches' width has been increased to reduce ohmic loss at high output power level.

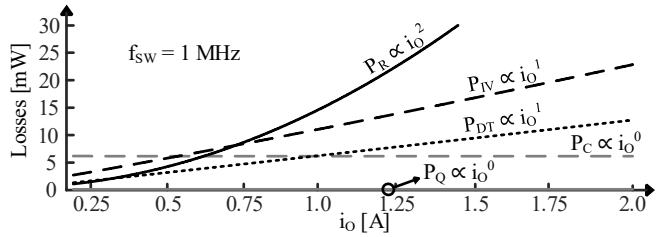

Fig. 6. Power losses across output current in CCM.

III. Power-Conversion Efficiency

Power-conversion efficiency refers to the fraction of P_{IN} that P_O outputs. η_C is ultimately a reflection of fractional losses. So, increasing η_C amounts to reducing σ_{LOSS}, as illustrates equation (1) below.

$$\eta_C = \frac{P_O}{P_{IN}} = \frac{P_{IN} - \sum P_L}{P_{IN}} = 1 - \sum \frac{P_L}{P_{IN}} = 1 - \sum \sigma_L. \qquad (1)$$

A. Fractional losses

Output power P_O (and thus input power P_{IN}) is proportional to output current i_O. What is ultimately important to understand what dictates the shape of power efficiency η_C is the dependence with output current of fractional losses. And this dependence also depends on the conduction mode.

DCM: In DCM, 3 components shape power efficiency η_C:

$$\sigma_{-1} = \frac{P_C + P_Q + P_{SW}}{P_{IN}} = \frac{K_{-1}}{i_O} \propto {i_O}^{-1}, \qquad (2)$$

$$\sigma_{-0.5} = \frac{P_{IV} + P_{DT}}{P_{IN}} = \frac{K_{-0.5}}{\sqrt{i_O}} \propto {i_O}^{-0.5}, \qquad (3)$$

and $$\sigma_{0.5} = \frac{P_R}{P_{IN}} = K_{0.5}\sqrt{i_O} \propto {i_O}^{0.5}. \quad (4)$$

σ_{-1} and $\sigma_{-0.5}$ will dominate at low i_O, then $\sigma_{0.5}$ will take over when i_O rises.

CCM: In CCM, 3 components also shape power efficiency η_C:

$$\sigma_{-1} = \frac{P_C+P_Q+P_{SW}+P_{R(AC)}}{P_{IN}} = \frac{K_{-1}}{i_O} \propto {i_O}^{-1}, \quad (5)$$

$$\sigma_0 = \frac{P_{IV}+P_{DT}}{P_{IN}} = K_0 \propto {i_O}^{0}, \quad (6)$$

and $$\sigma_1 = \frac{P_{R(DC)}}{P_{IN}} = K_1 i_O \propto {i_O}^{1}. \quad (7)$$

σ_{-1} will dominate at low i_O. At moderate i_O, σ_0 will be dominant, then σ_1 will take over when i_O further increase. In Fig. 7, a simulation of a 1.8 V to 1 V buck operating in DCM shows the fractional losses distribution.

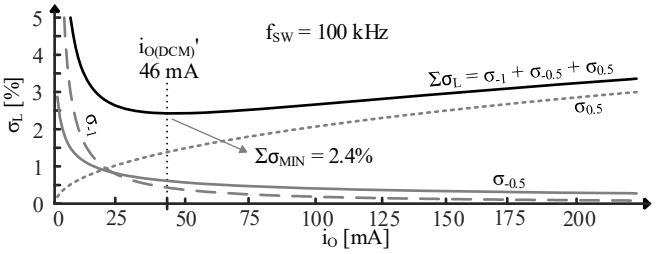

Fig. 7. Fractional losses in DCM.

Fig. 8 shows fractional losses for the same buck converter operating in CCM. When i_O reaches i_O", σ_0 will become dominant, and then σ_1 will take over when i_O reaches i_O'''. Optimal output current in CCM is reached when σ_{-1} and σ_1 are balanced. Relative dependence of fractional losses with output current ultimately dictates how η_C rises, peaks and falls.

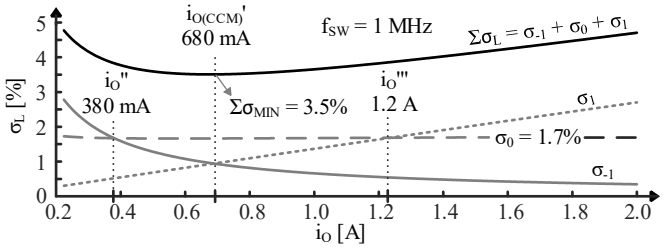

Fig. 8. Fractional losses in CCM.

B. Dominance

When lightly loaded, the i_O that sets P_O is so low that controller and gate-charge loss swamp all other losses. σ_{LOSS} in this region therefore rests on P_Q and P_C and the i_O that sets P_{IN}: σ_{-1} dominates in this region, as Fig. 9 illustrates. In this region, η_C climbs because P_Q and P_C dominate and do not scale with i_O, so σ_{LOSS} falls as i_O rises. η_C then falls after peaking when P_R equalizes and surpasses P_C and P_Q. $\sigma_{0.5}$ therefore dominates in the second section of the DCM region.

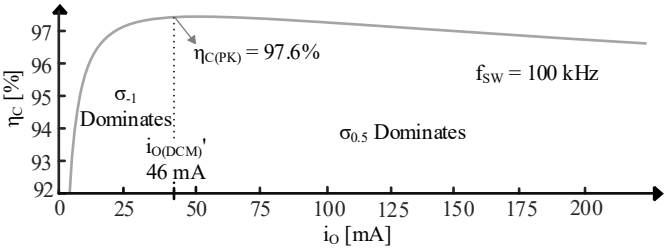

Fig. 9. Conversion efficiency in DCM.

Continuous conduction begins when $i_{L(AVG)}$ and the corresponding i_O surpass $0.5\Delta i_L$ and $0.5\Delta i_L$'s d_{DO} translation. In this region, P_C, $P_{R(AC)}$, P_Q and P_{SW}, which are independent of i_O, dominate. P_C influence this σ_{LOSS} when switches are large and f_{SW} is high, which is the case in Fig. 10. P_{SW} is usually negligible because it is normally much lower. But since $P_{R(AC)}$, P_C and P_{SW} do not scale with i_O and P_{IN} does, σ_{LOSS} falls and η_C climbs as i_O rises in region σ_{-1} in Fig. 10.

η_C peaks and flattens in region σ_0 when i_O-sensitive losses swamp $P_{R(AC)}$, P_C and P_{SW}. σ_{LOSS} is steady here because P_{DT}, P_{IV} and P_{IN} all scale with i_O. Static $i_{RMS}{}^2R_X$ losses dominate with higher i_O because $P_{R(DC)}$ increases faster with i_O than P_{DT} and P_{IV}. So, in region σ_1, σ_{LOSS} climbs and η_C falls because $P_{R(DC)}$'s quadratic rise outpaces P_{IN}'s linear climb.

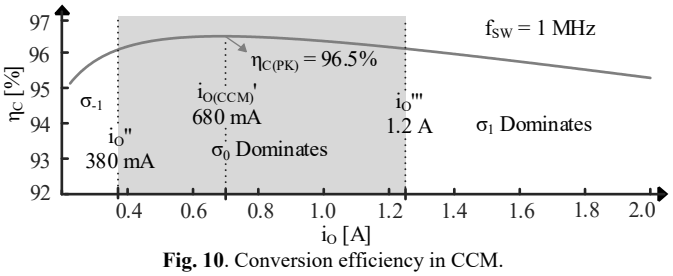

Fig. 10. Conversion efficiency in CCM.

C. Peak

DCM: $\sigma_{LOSS(DCM)}$ is the fraction of P_{IN} lost to $P_{R(AC)}$, P_{DT}, P_{IV}, P_C, and to a lesser extent, P_{SW}. So, P_Q, P_C, P_{SW} in region σ_{-1}, P_{IV} and P_{DT} in region $\sigma_{-0.5}$, and P_R in region $\sigma_{0.5}$ add in $\sigma_{LOSS(DCM)}$:

$$\sigma_{LOSS(DCM)} = \sigma_{-1} + \sigma_{-0.5} + \sigma_{0.5}. \quad (8)$$

$\sigma_{LOSS(DCM)}$ is minimal when the $\sigma_{LOSS(DCM)}$'s slope with respect to i_O is zero:

$$\left.\frac{\partial\sigma_{LOSS(DCM)}}{\partial i_O}\right|_{i_O'} = \left.\frac{\partial\sigma_{-1}}{\partial i_O}\right|_{i_O'} + \left.\frac{\partial\sigma_{-0.5}}{\partial i_O}\right|_{i_O'} + \left.\frac{\partial\sigma_{0.5}}{\partial i_O}\right|_{i_O'} = -\frac{K_{-1}}{{i_O'}^2} + \frac{K_{0.5}}{2\sqrt{i_O}} - \frac{K_{-0.5}}{2{i_O}^{3/2}} = 0. \quad (9)$$

This equation can be solved numerically in order to obtain i_O' in DCM.

CCM: A similar reasoning can be made in CCM. $\sigma_{LOSS(CCM)}$ in continuous conduction is ultimately the fraction of P_{IN} lost to $P_{R(DC)}$, $P_{R(AC)}$, P_{DT}, P_{IV}, P_C, and to a lesser extent, P_{SW}. So, $P_{R(AC)}$, P_C, P_{SW} in region σ_{-1}, P_{IV} and P_{DT} in region σ_0, and $P_{R(DC)}$ in region σ_1 add in σ_{LOSS}:

$$\sigma_{LOSS(CCM)} = \sigma_{-1} + \sigma_0 + \sigma_1. \quad (10)$$

σ_{LOSS} is minimal when the σ_{LOSS}'s slope with respect to i_O is zero, which happens at optimal output current i_O' when σ_{-1}'s fall cancel σ_1's rise, match, and $\sigma_{LOSS(MIN)}$ is the sum of σ_{CCM}'s at i_O':

$$\left.\frac{\partial\sigma_{LOSS(CCM)}}{\partial i_O}\right|_{i_O'} = \left.\frac{\partial\sigma_{-1}}{\partial i_O}\right|_{i_O'} + \left.\frac{\partial\sigma_0}{\partial i_O}\right|_{i_O'} + \left.\frac{\partial\sigma_1}{\partial i_O}\right|_{i_O'} = -\frac{K_{-1}}{{i_O'}^2} + K_1 = 0, \quad (11)$$

$$i_O' = \sqrt{\frac{K_{-1}}{K_1}}, \quad (12)$$

$$\sigma_{-1} = \sigma_1 = \sqrt{K_{-1}K_1}, \quad (13)$$

and

$$\sigma_{\mathrm{LOSS(CCM)(MIN)}} = \sigma_{-1}|_{i_O'} + \sigma_0|_{i_O'} + \sigma_1|_{i_O'} = \sigma_0 + 2\sqrt{K_{-1}K_1}. \quad (14)$$

IV. Validation

A. Synchronous Buck Example

In this section, a synchronous buck converter is studied to plot an experimental efficiency. During dead times, inductor current flows through M_G body diode. Fig. 11 shows the schematic of the simulated buck converter. Both power MOSFETs are driven by a one stage inverter in order to reduce overlap loss and make driver losses negligible. Quiescent power P_Q burned by the controller can be estimated about 30 µW [29].

In order to balance gate charge loss P_C with ohmic loss P_R of MOSFETs, MOSFETs' widths have been designed for P_C and P_R to be balanced for i_O = 30 mA in DCM, and for i_O = 1.2 A in CCM. Only M_{I1} and M_{G1} are used in DCM, and when the converter enters CCM, M_{I2} and M_{G2} are used in parallel of M_{I1} and M_{G1} to increase MOSFETs' width.

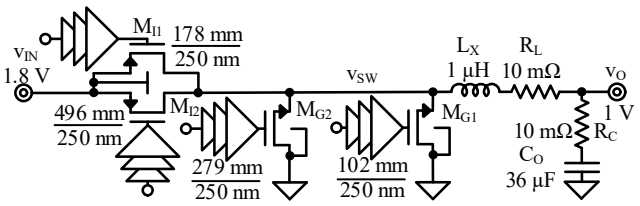

Fig. 11. Simulated synchronous buck.

B. Simulated Losses

Simulating with SPICE the circuit in Fig. 11 for different output current gives the following graph for simulated losses, as Fig. 12 illustrates in DCM and as Fig. 13 illustrates in CCM. The converter operates at 100 kHz in DCM, and at 1 MHz in CCM.

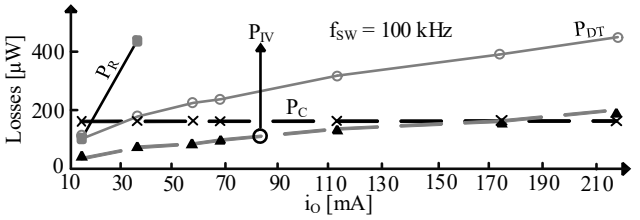

Fig. 12. Simulated losses in DCM.

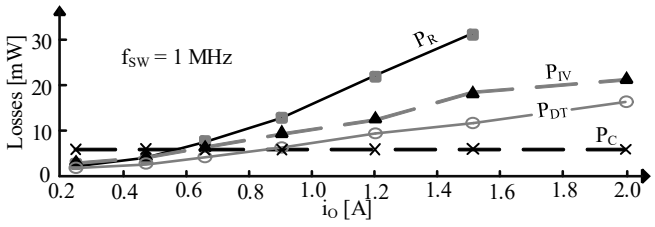

Fig. 13. Simulated losses in CCM.

C. Simulated Efficiency

Simulated efficiency can be extracted from simulations of the buck converter above. Fig. 14 and Fig. 15 show simulated efficiency for different output current levels. Interestingly, as both fractional losses in DCM and CCM include components which increase with output power and components which decrease with output power, power efficiency η_C shows 2 maxima, one in DCM, and one in CCM. Solving equation (12) and (14) as section III explains, optimal output current $i_O'_{(DCM)}$ and $i_O'_{(CCM)}$ are 46 mA and 680 mA.

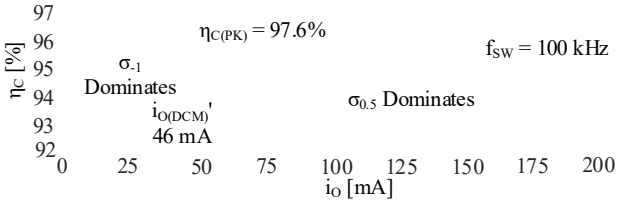

Fig. 14. Simulated efficiency in DCM.

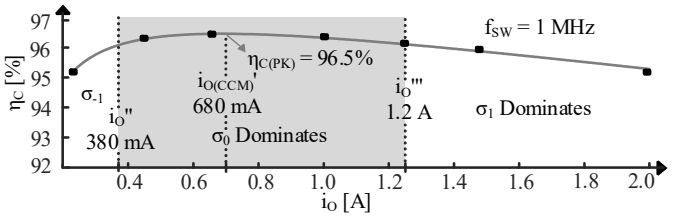

Fig. 15. Simulated efficiency in CCM.

V. Significance

This paper gives an understanding on how losses rise, decrease and balance each other. It describes with insight what is their relative dependencies with output current, and how it affects power efficiency. For many applications, the most probable output power level can be defined. Designers can therefore design power supplies for power efficiency to peak, in DCM and in CCM, at the output current level where the converter is the most likely to operate. For example, switches width can be chosen carefully for gate drive loss and MOSFET ohmic loss to balance each other at a specific current level.

The analysis derived in this paper allows for an insightful understanding of what makes the power efficiency peak. Depending on design and requirements (size constraints for instance), relative weight of all losses can be changed, but the analysis derived in this paper allows to predict the behavior of power efficiency with output power. Namely, L_X plays a pivotal role in determining i_O' and $\eta_{C(CCM)(PK)}$ when R_L is much greater than the on resistances of the switches. This can happen with small inductors because internal coils are thin. In these cases, engineers can influence, but not necessarily define the i_O' that peaks η_C.

VI. Conclusions

An insightful power efficiency interpretation has been presented in this article. This interpretation allows for understanding when power efficiency rises, peaks and falls, depending on the regime of conduction. Dependency of losses and fractional losses have been studied, allowing prediction of the behavior and dominance of losses across output power. An example of a buck converter has been studied to verify the theory presented.

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REFERENCES

[1] Z. Hong, X. Jian, Z. Liang, Y. Fei and C. Jiong, "Research on Adaptive Switching Power Supply Control Technology," *Proc. of 2018 International Conference of Safety Produce Informatization (IICSPI)*, Chongqing, China, 2018, pp. 742-745.

[2] P. Chhawchharia, D. K. W. Cheng and Y. S. Lee, "On the performance improvement for design optimization of buck convertors," *Proc. of Second International Conference on Power Electronics and Drive Systems*, Singapore, 1997, pp. 570-575.

[3] A. A. Fomani and W. T. Ng, "A segmented gate driver with adjustable driving capability for efficiency optimization," *Proc. of 2010 International Power Electronics Conference (ECCE ASIA)*, Sapporo, 2010, pp. 1646-1650.

[4] J. Lee, G. Hatcher, L. Vandenbergh and Chih-Kong Ken Yang, "Evaluation of fully-integrated switching regulators for CMOS process technologies," *Proc. of 2003 International Symposium on System-on-Chip* , Tampere, 2003, pp. 155-158.

[5] W. Wang, R. Wei and Y. Yin, "Efficiency-based power MOSFETs size optimization method for DC-DC buck converters," *Proc. of 2019 20th International Symposium on Power Electronics*, Novi Sad, Serbia, 2019, pp. 1-5.

[6] F. Haizoune, H. J. Bergveld, J. Popovic-Gerber and J. A. Ferreira, "Topology comparison and design optimisation of the buck converter and the single-inductor dual-output converter for system-in-package in 65nm CMOS," *Proc. of 2009 IEEE 6th International Power Electronics and Motion Control Conference*, Wuhan, 2009, pp. 295-301.

[7] Ke Wang, Li Geng and Qingrui Meng, "Efficiency improvement in buck-boost converter aimed at SOC utilization," *Proc. of 2008 IEEE International Conference on Industrial Technology*, Chengdu, 2008, pp. 1-5.

[8] K. B. Östman and J. K. Järvenhaara, "A Rapid Switch Bridge Selection Method for Fully Integrated DCDC Buck Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4048-4051, Aug. 2015.

[9] G. Sizikov, A. Kolodny, E. G. Fridman and M. Zelikson, "Efficiency optimization of integrated DC-DC buck converters," *Proc. of 2010 17th IEEE International Conference on Electronics, Circuits and Systems*, Athens, 2010, pp. 1208-1211.

[10] H. Huang, K. Chen and S. Kuo, "Dithering Skip Modulation, Width and Dead Time Controllers in Highly Efficient DC-DC Converters for System-On-Chip Applications," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2451-2465, Nov. 2007.

[11] V. Michal, "Peak-Efficiency Detection and Peak-Efficiency Tracking Algorithm for Switched-Mode DC–DC Power Converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6555-6568, Dec. 2014.

[12] Y. Yamauchi, Y. Yanagihara, H. Fuketa, T. Sakurai and M. Takamiya, "Optimal design to maximize efficiency of single-inductor multiple-output buck converters in discontinuous conduction mode for IoT applications," *Proc. of 2015 International Conference on IC Design & Technology (ICICDT)*, Leuven, 2015, pp. 1-4.

[13] G. Schrom, P. Hazucha, F. Paillet, D. S. Gardner, S. T. Moon and T. Karnik, "Optimal Design of Monolithic Integrated DC-DC Converters," *Proc. of 2006 IEEE International Conference on IC Design and Technology*, Padova, 2006, pp. 1-3.

[14] S. Bandyopadhyay, Y. K. Ramadass and A. P. Chandrakasan, "20μA to 100mA DC-DC converter with 2.8 to 4.2V battery supply for portable applications in 45nm CMOS," *Proc. of 2011 IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 386-388.

[15] V. Kursun, S. G. Narendra, V. K. De and E. G. Friedman, "Efficiency analysis of a high frequency buck converter for on-chip integration with a dual-V_{DD} microprocessor," *Proc. of the 28th European Solid-State Circuits Conference*, Florence, Italy, 2002, pp. 743-746.

[16] Y. Katayama, M. Edo, T. Denta, T. Kawashima and T. Ninomiya, "Optimum design method of CMOS IC for DC-DC converter that integrates power stage MOSFETs," *Proc. of 2004 IEEE 35th Annual Power Electronics Specialists Conference*, Aachen, Germany, 2004, pp. 4486-4491.

[17] B. Arbetter, R. Erickson and D. Maksimovic, "DC-DC converter design for battery-operated systems," *Proc. of Power Electronics Specialist Conference*, Atlanta, GA, USA, 1995, pp. 103-109.

[18] X. Li, F. Lin, X. Zhang, M. Huang and H. Wang, "Multi-objective Design of LC Filter for High-efficiency, High-power-density and High-performance Buck Converter," *Proc. of 2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 5132-5136.

[19] O. Djekic, M. Brkovic and A. Roy, "High frequency synchronous buck converter for low voltage applications," *Proc. of 29th Annual IEEE Power Electronics Specialists Conference*, Fukuoka, 1998, pp. 1248-1254.

[20] G. Villar, E. Alarcon, F. Guinjoan and A. Poveda, "Efficiency-oriented switching frequency tuning for a buck switching power converter," 2005 IEEE International Symposium on Circuits and Systems, Kobe, 2005, pp. 2473-2476 Vol. 3, doi: 10.1109/ISCAS.2005.1465127.

[21] X. Wang and A. Q. Huang, "Considerations on the optimal power stage segmentation algorithm for MHz integrated synchronous Buck DC-DC converters," *Proc. of 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, San Diego, CA, 2011, pp. 184-187.

[22] V. Kursun, S. G. Narendra, V. K. De and E. G. Friedman, "Low-voltage-swing monolithic dc-dc conversion," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 5, pp. 241-248, May 2004.

[23] Xunwei Zhou, T. G. Wang and F. C. Lee, "Optimizing design for low voltage DC-DC converters," *Proc. of Applied Power Electronics Conference (APEC)*, Atlanta, GA, USA, 1997, pp. 612-616 vol.2.

[24] Z. Zhang, W. Eberle, Z. Yang, Y. Liu and P. C. Sen, "Optimal Design of Current Source Gate Driver for a Buck Voltage Regulator Based on a New Analytical Loss Model," *Proc. of 2007 IEEE Power Electronics Specialists Conference*, Orlando, FL, 2007, pp. 1556-1562.

[25] J. Fu, Z. Zhang, Y. Liu and P. C. Sen, "MOSFET Switching Loss Model and Optimal Design of a Current Source Driver Considering the Current Diversion Problem," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 998-1012, Feb. 2012.

[26] Y. Naeimi and A. Huang, "Design and optimization of high conversion ratio quasi square wave buck converters," *Proc. of 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 148-152.

[27] R. Modak and M. S. Baghini, "A generic analytical model of switching characteristics for efficiency-oriented design and optimization of CMOS integrated buck converters," *Proc. of 2009 IEEE International Conference on Industrial Technology*, Gippsland, VIC, 2009, pp. 1-6.

[28] O. Lazaro and G. A. Rincon-Mora, "Minimizing MOSFET power losses in near-field electromagnetic energy-harnessing ICs," *Proc. of 2011 International SoC Design Conference*, Jeju, 2011, pp. 377-380.

[29] R. Damodaran Prabha and G. A. Rincón-Mora, "0.18-μm Light-Harvesting Battery-Assisted Charger–Supply CMOS System," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2950-2958, April 2016.