Power-Conversion Efficiency: Loss Dominance, Optimization, & Design Insight

Guillaume Guérin, Graduate Student Member, IEEE, and Gabriel A. Rincón-Mora, Fellow, IEEE

Abstract—Power-conversion efficiency is critical in power supplies. Switched inductors are popular in this space because they can deliver a large fraction of the power they draw. This fraction hinges on the power that switches, diodes, resistances, and capacitances need to conduct and transfer power to the output. So, understanding how these loss mechanisms set and dictate efficiency across power levels is important, especially when designing and targeting particular load levels. This article details how these losses scale, when they dominate, and how and when they balance. Gate drive and controller losses are the ones that become a smaller fraction of input power as output power increases, leading to the increase of the power efficiency at the low-end of discontinuous conduction scale, while only gate charge loss plays this role at the low-end of the continuous conduction scale. Ohmic loss is the one that reduces power efficiency at the high-end of discontinuous and continuous conduction scale as ohmic loss becomes a larger fraction of input power as output power increases. Power efficiency peaks in continuous conduction when ohmic loss and gate charge losses balance. Overlap and dead time losses, although still important, do not shape the power efficiency in continuous conduction mode. In discontinuous conduction mode, all losses play a role and efficiency peaks when they all trickily balance. With this insight, predicting and controlling when efficiency rises, peaks, and falls across loads are possible. The fractional loss analysis and the design insight that make this possible are new contributions to the state of the art.

Index Terms—Switched inductor, power efficiency, interpretation, fractional losses, loss dominance, optimization, design insight, peak efficiency.

I. POWER SUPPLIES

Power supplies are everywhere nowadays. The rise of connected devices and systems known as the Internet-of-Things requires power supplies to be always more efficient and more versatile. Switched-inductor power supplies are pervasive in electronic systems because they output a large fraction of the power they draw from their inputs. The main reason for this is that the voltage that switches drop are a very small fraction of the output voltage. So, the inductor current usually delivers more power by design into the output than switches consume. Still, the heat that burning power generates can compromise electronic performance and mechanical integrity [1]. Also, losing battery energy or ambient power to the power supply reduces the charge life or functionality of a system.

Power-conversion efficiency \( \eta_C \) is the fraction of input power \( P_{IN} \) that the input \( V_{IN} \) delivers to the output \( V_O \) in Fig. 1. The load can be composed of Analog-to-Digital Converter (ADC), Digital Signal Processing microcontrollers (DSP), Digital-to-Analog Converter (DAC), voltage amplifiers, Power Amplifier (PA), and Sensors for instance. Internet-of-Things is a very good example of the diversity of a load.

Power efficiency \( \eta_C \) has to be as high as possible for several reasons. DC-DC converters can be found after an AC-DC converter, and therefore have to maintain a high rating. Losses occurring within the power supply also create heat difficult to cool down, thus limiting the power that can be delivered to the load. On top of heat, embedded systems, such as Internet-of-Things, which are often powered by batteries which provide only a limited amount of energy, cannot afford to lose too much power in losses.

Fig. 1. Electronic system with power supply and load.

\( P_{IN} \) also supplies power losses \( P_{LOSS} \). So, \( P_O \) outputs the difference \( P_{IN} - P_{LOSS} \). Fractional loss \( \sigma_{LOSS} \) is the fraction of \( P_{IN} \) lost in \( P_{LOSS} \), and \( \sigma_C \) is below 100% by the amount \( \sigma_{LOSS} \) sets. Thus, understanding the nature, makeup, and sensitivity of these losses is important.

Majority of state-of-the-art papers do not consider all kinds of losses: [2] ignores gate drive loss, while [3] and [4] do not consider dead time loss. [5]—[9] do not take into account IV overlap loss nor dead time loss. Some others don’t even break down losses to analyze the losses significance and distribution across output power [10]—[27]. Moreover, none of state-of-the-art papers offer a fractional losses-oriented approach to break down and analyze power efficiency across output power. The contribution of this paper is an insightful losses and power efficiency analysis allowing designers to predict when efficiency rises, peaks and falls across output power. This paper is organized as follows: Section II describes losses mechanisms, while Section III gives an insight about fractional losses and power efficiency. Section IV presents an example with a synchronous buck voltage regulator, Section V presents the significance of the analysis derived, and Section VI concludes the paper.

II. LOSS MECHANISMS

Many different kinds of losses contribute to reduce overall power efficiency. Fig. 2 shows a schematic of a buck-boost, with parasitic components. The most fundamental of these is conduction power. This is the power that components consume when they conduct inductor current. Series resistances (\( R_L \) and \( R_C \) in Fig. 2), transistors (\( M_{EI} \), \( M_{DG} \), \( M_{DO} \)), and...
and $M_{EG}$, leading to ohmic losses $P_R$), and body diodes ($D_{D1}$ and $D_{D2}$, leading to dead-time loss $P_{DT}$) are to blame for this.

Another loss is the power $P_C$ that gate drivers need to transition switches between states. Stres capacitances $C_{SW}$ at switching nodes leak power, included in $P_{SW}$. Switching mechanisms of hard-switched MOSFETs ($M_{EI}$ and $M_{EG}$ in Fig. 2) lead to overlap loss $P_{IV}$. Finally, controller burns power $P_Q$.

In order to optimize losses depending on the regime of conduction, some techniques can be used, such as reducing MOSFETs’ widths and switching frequency in DCM [9]. As the inductor current is lower in DCM, ohmic losses are lower, so MOSFETs’ widths can be lowered to reduce gate charge loss $P_C$. $P_C$ can be further reduced by reducing $f_{SW}$.

### III. Power-Conversion Efficiency

Power-conversion efficiency refers to the fraction of $P_{IN}$ that $P_O$ outputs. $\eta_C$ is ultimately a reflection of fractional losses. So, increasing $\eta_C$ amounts to reducing $\sigma_{LOSS}$, as illustrates equation (1) below.

$$\eta_C = \frac{P_O}{P_{IN}} = \frac{P_{IN} - \Sigma P_L}{P_{IN}} = 1 - \Sigma \frac{P_L}{P_{IN}} = 1 - \Sigma \sigma_L. \quad (1)$$

### A. Fractional losses

Output power $P_O$ (and thus input power $P_{IN}$) is proportional to output current $i_O$. What is ultimately important to understand what dictates the shape of power efficiency $\eta_C$ is the dependence with output current of fractional losses. And this dependence also depends on the conduction mode.

**DCM:** In DCM, 3 components shape power efficiency $\eta_C$:

$$\sigma_{-1} = \frac{P_C + P_M + P_{SW}}{P_{IN}} = \frac{K_{-1}}{i_O^{-1}},$$

$$\sigma_{-0.5} = \frac{P_C + P_M + P_{DT}}{P_{IN}} = \frac{K_{-0.5}}{i_O^{-0.5}}.$$

---

**Fig. 2. CMOS switched-inductor power supply.**

**Fig. 3. Inductor current $i_L$ in discontinuous conduction mode.**

**Fig. 4. Power losses across output current in DCM.**

**Fig. 5. Inductor current $i_L$ in continuous conduction mode.**

**Fig. 6. Power losses across output current in CCM.**
and \[ \sigma_{0.5} = \frac{P_R}{P_{IN}} = K_{0.5}\sqrt{i_o} \propto i_o^{0.5}. \]  

\( \sigma_1 \) and \( \sigma_{0.5} \) will dominate at low \( i_o \), then \( \sigma_{0.5} \) will take over when \( i_o \) rises.

**CCM:** In CCM, 3 components also shape power efficiency \( \eta_C \):

\[ \sigma_1 = \frac{C_{\text{CM}}+P_{\text{SW}}+P_{\text{R(AC)}}}{P_{\text{IN}}} = K_1 \propto i_o^{-1}. \]

\( \sigma_0 = \frac{P_{\text{IV}}+P_{\text{DT}}}{P_{\text{IN}}} = K_0 \propto i_o^0, \]

and \( \sigma_1 = \frac{P_{\text{R(DC)}}}{P_{\text{IN}}} = K_1 i_o \propto i_o^1. \)

\( \sigma_1 \) will dominate at low \( i_o \). At moderate \( i_o \), \( \sigma_0 \) will be dominant, and then \( \sigma_1 \) will take over when \( i_o \) further increase. In Fig. 7, a simulation of a 1.8 V to 1 V buck operating in DCM shows the fractional losses distribution.

![Fig. 7. Fractional losses in DCM.](image)

**B. Dominance**

When lightly loaded, the \( i_o \) that sets \( P_0 \) is so low that controller and gate-charge loss swamp all other losses. \( \sigma_{\text{LOSS}} \) in this region therefore rests on \( P_0 \) and \( P_C \) and the \( i_o \) that sets \( P_{\text{IN}} \): \( \sigma_1 \) dominates in this region, as Fig. 9 illustrates. In this region, \( \eta_C \) climbs because \( P_0 \) and \( P_C \) dominate and do not scale with \( i_o \), so \( \sigma_{\text{LOSS}} \) falls as \( i_o \) rises. \( \eta_C \) then falls after peaking when \( P_R \) equalizes and surpasses \( P_C \) and \( P_Q \). \( \sigma_{0.5} \) therefore dominates in the second section of the DCM region.

![Fig. 9. Conversion efficiency in DCM.](image)

Continuous conduction begins when \( i_{L(AVG)} \) and the corresponding \( i_o \) surpass 0.5A\( L \) and 0.5A\( L \)’s \( f_{SW} \) translation. In this region, \( P_C \), \( P_{\text{R(AC)}} \), \( P_{\text{Q}} \) and \( P_{\text{SW}} \), which are independent of \( i_o \), dominate. \( P_C \) influence this \( \sigma_{\text{LOSS}} \) when switches are large and \( f_{SW} \) is high, which is the case in Fig. 10. \( P_{\text{SW}} \) is usually negligible because it is normally much lower. But since \( P_{\text{R(AC)}} \), \( P_C \) and \( P_{\text{SW}} \) do not scale with \( i_o \) and \( P_{\text{IN}} \) does, \( \sigma_{\text{LOSS}} \) falls and \( \eta_C \) peaks as \( \sigma_1 \) rises in region \( \sigma_1 \) in Fig. 10.

\( \eta_C \) peaks and flattens in region \( \sigma_0 \) when \( i_o \)-sensitive losses swamp \( P_{\text{R(AC)}} \), \( P_C \) and \( P_{\text{SW}} \). \( \sigma_{\text{LOSS}} \) is steady here because \( P_{\text{DT}} \), \( P_{\text{IV}} \) and \( P_{\text{IN}} \) all scale with \( i_o \). Static \( i_{\text{MS}}^2R_X \) losses dominate with higher \( i_o \) because \( P_{\text{R(DC)}} \) increases faster with \( i_o \) than \( P_{\text{DT}} \) and \( P_{\text{IV}} \). So, in region \( \sigma_1 \), \( \sigma_{\text{LOSS}} \) climbs and \( \eta_C \) falls because \( P_{\text{R(DC)}} \)’s quadratic rise outpaces \( P_{\text{IN}} \)’s linear climb.

**C. Peak**

**DCM:** \( \sigma_{\text{LOSS(DCM)}} \) is the fraction of \( P_{\text{IN}} \) lost to \( P_{\text{R(AC)}} \), \( P_{\text{DT}} \), \( P_{\text{IV}} \), \( P_C \), and to a lesser extent, \( P_{\text{SW}} \). So, \( P_0 \), \( P_C \), \( P_S \) in region \( \sigma_1 \), \( P_{\text{IV}} \) and \( P_{\text{DT}} \) in region \( \sigma_{0.5} \), and \( P_R \) in region \( \sigma_{0.5} \) add in \( \sigma_{\text{LOSS(DCM)}} \):

\[ \sigma_{\text{LOSS(DCM)}} = \sigma_{-1} + \sigma_{-0.5} + \sigma_1. \]

\( \sigma_{\text{LOSS(DCM)}} \) is minimal when the \( \sigma_{\text{LOSS(DCM)}} \)’s slope with respect to \( i_o \) is zero:

\[ \frac{\partial \sigma_{\text{LOSS(DCM)}}}{\partial i_o} \bigg|_{i_o'} = 0. \]

This equation can be solved numerically in order to obtain \( i_o' \) in DCM.

**CCM:** A similar reasoning can be made in CCM. \( \sigma_{\text{LOSS(CCM)}} \) in continuous conduction is ultimately the fraction of \( P_{\text{IN}} \) lost to \( P_{\text{R(DC)}} \), \( P_{\text{R(AC)}} \), \( P_{\text{DT}} \), \( P_{\text{IV}} \), \( P_C \), and to a lesser extent, \( P_{\text{SW}} \). So, \( P_{\text{R(DC)}} \), \( P_C \), \( P_{\text{SW}} \) in region \( \sigma_1 \), \( P_{\text{IV}} \) and \( P_{\text{DT}} \) in region \( \sigma_{0.5} \), and \( P_R \) in region \( \sigma_{0.5} \) add in \( \sigma_{\text{LOSS}} \):

\[ \sigma_{\text{LOSS(CCM)}} = \sigma_{-1} + \sigma_0 + \sigma_1. \]

\( \sigma_{\text{LOSS}} \) is minimal when the \( \sigma_{\text{LOSS}} \)’s slope with respect to \( i_o \) is zero, which happens at optimal output current \( i_o' \) when \( \sigma_1 \)’s fall cancel \( \sigma_1 \)’s rise, match, and \( \sigma_{\text{LOSS(MIN)}} \) is the sum of \( \sigma_{\text{CCM}} \)’s at \( i_o' \):

\[ \frac{\partial \sigma_{\text{LOSS(CCM)}}}{\partial i_o} \bigg|_{i_o'} = 0. \]

(11)

\[ i_o' = \frac{K_1}{\sqrt{K_1}}. \]

(12)

\( \sigma_{-1} = \sigma_1 = \sqrt{K_1K_1}. \)
and
\[
\sigma_{\text{LOSS} (\text{CCM}) (\text{MIN})} = \sigma_{-1} I_{O} + \sigma_{0} I_{O} + \sigma_{1} I_{O} \\
= \sigma_{0} + 2\sqrt{K_{-1} K_{1}}.
\] (14)

IV. VALIDATION

A. Synchronous Buck Example

In this section, a synchronous buck converter is studied to plot an experimental efficiency. During dead times, inductor current flows through \( M_{G1} \) body diode. Fig. 11 shows the schematic of the simulated buck converter. Both power MOSFETs are driven by a one stage inverter in order to reduce overlap loss and make driver losses negligible. Quiescent power \( P_{Q} \) burned by the controller can be estimated about 30 \( \mu \text{W} \) [29].

In order to balance gate charge loss \( P_{C} \) with ohmic loss \( P_{R} \) of MOSFETs, MOSFETs’ widths have been designed for \( P_{C} \) and \( P_{R} \) to be balanced for \( i_{O} = 30 \text{ mA} \) in DCM, and for \( i_{O} = 1.2 \text{ A} \) in CCM. Only \( M_{11} \) and \( M_{G1} \) are used in DCM, and when the converter enters CCM, \( M_{12} \) and \( M_{G2} \) are used in parallel of \( M_{11} \) and \( M_{G1} \) to increase MOSFETs’ width.

B. Simulated Losses

Simulating with SPICE the circuit in Fig. 11 for different output current gives the following graph for simulated losses, as Fig. 12 illustrates in DCM and as Fig. 13 illustrates in CCM. The converter operates at 100 kHz in DCM, and at 1 MHz in CCM.

- In DCM, the losses peak at around 30 \( \mu \text{W} \) for \( i_{O} = 30 \text{ mA} \), and decrease with output power.
- In CCM, the losses peak at around 30 \( \mu \text{W} \) for \( i_{O} = 1.2 \text{ A} \), and also decrease with output power.

C. Simulated Efficiency

Simulated efficiency can be extracted from simulations of the buck converter above. Fig. 14 and Fig. 15 show simulated efficiency for different output current levels. Interestingly, as both fractional losses in DCM and CCM include components which increase with output power and components which decrease with output power, power efficiency \( \eta_{C} \) shows 2 maxima, one in DCM, and one in CCM. Solving equation (12) and (14) as section III explains, optimal output current \( i_{O}^{(DCM)} \) and \( i_{O}^{(CCM)} \) are 46 mA and 680 mA.

V. SIGNIFICANCE

This paper gives an understanding on how losses rise, decrease and balance each other. It describes with insight what is their relative dependencies with output current, and how it affects power efficiency. For many applications, the most probable output power level can be defined. Designers can therefore design power supplies for power efficiency to peak, in DCM and in CCM, at the output current level where the converter is the most likely to operate. For example, switches width can be chosen carefully for gate drive loss and MOSFET ohmic loss to balance each other at a specific current level.

The analysis derived in this paper allows for an insightful understanding of what makes the power efficiency peak. Depending on design and requirements (size constraints for instance), relative weight of all losses can be changed, but the analysis derived in this paper allows to predict the behavior of power efficiency with output power. Namely, \( L_{X} \) plays a pivotal role in determining \( i_{O}^{*} \) and \( \eta_{C}^{(CCM)(PK)} \) when \( R_{L} \) is much greater than the on resistances of the switches. This can happen with small inductors because internal coils are thin. In these cases, engineers can influence, but not necessarily define the \( i_{O}^{*} \) that peaks \( \eta_{C} \).

VI. CONCLUSIONS

An insightful power efficiency interpretation has been presented in this article. This interpretation allows for understanding when power efficiency rises, peaks and falls, depending on the regime of conduction. Dependency of losses and fractional losses have been studied, allowing prediction of the behavior and dominance of losses across output power. An example of a buck converter has been studied to verify the theory presented.

ACKNOWLEDGMENT

The authors thank Texas Instruments (TI) for sponsoring this research and Dr. Orlando Lazaro, Dr. Andres Blanco, Dr. Nan Xing, and Dr. Jeff Morrow for their support and advice.
REFERENCES


