Ripple Suppression of On-Chip Switched-Inductor Power Supplies

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***Abstract*—Emerging applications demand compact, battery-powered, and highly functional microsystems that require on-chip integration, low average power, and high peak-to-average power ratios. Switched inductors are popular power supplies because they are power efficient. Switching a power inductor, however, generates a nonlinear current ripple that is often difficult to tolerate and manage. The problem is more severe with on-chip nH inductors and pF capacitors. This paper explores how switching power supplies can manage and reduce this ripple. Although multiphase and filter suppressors help, analog cancellation can be 38× to 77× more effective, but also less power efficient and 23× to 55× more sensitive to mismatch from drift.**

Keywords—Monolithic power supplies, on-chip integration, switched inductors, dc–dc converters, ripple suppressors.

I. On-Chip Power Supplies

Emerging wireless microsensors and other micro-scale applications demand more integration and functionality than ever before. This is because fewer board components, fewer pins, and lower board complexity reduce volume, cost, and risk [1]–[3]. But devices are so small and functionality is so high that onboard batteries drain and deplete quickly.

With so little energy, on-chip power supplies cannot afford to lose much power. Linear regulators are compact and free of switching noise, but not very efficient. Switched capacitors (SC) are more efficient [4], but not as much as switched inductors (SL) because, with fewer switches, SL's have less gate capacitance to charge [5]. The current ripples that SL's produce, however, burn power and generate noise [6]–[8].

In the basic buck converter shown in Fig. 1, for example, switch S_I energizes and S_G drains inductor L_X from input v_{IN} to output v_O in alternating phases of the switching period t_{SW}. L_X's current i_O therefore rises in Fig. 2 across the energizing period t_E that S_I establishes and falls across the drain time t_D that S_G sets. Since the load i_{LD} normally draws i_O's average $i_{O(AVG)}$, the output capacitor C_O sinks i_O's ripple Δi_O. This means, C_O's equivalent series resistance R_{CO} burns $\Delta i_{O(RMS)}{}^2R_{CO}$ power, and together with C_O, produce the voltage ripple Δv_O shown in v_O.

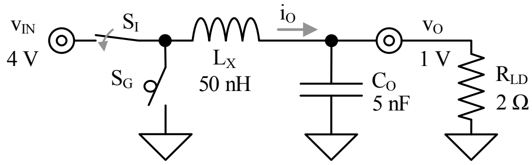

Fig. 1. Basic buck dc–dc converter.

When integrated on chip, L_X and C_O can be 50 nH and 500 pF [9]–[18]. So when t_{SW}, v_{IN}, v_O, and R_{LD} are 100 ns, 4 V, 1 V, and 2 Ω and R_{CO} is negligibly low, Δi_O is so high that L_X conducts discontinuously and Δv_O is excessively noisy. Increasing the switching frequency f_{SW} to 100 MHz reduces Δi_O and Δv_O to 150 mA and 220 mV. Switching S_I and S_G at 100 MHz, however, requires more gate-drive power [5]. Plus, 220 mV's ±11% ripple about 1 V is too noisy for modern applications. Increasing C_O to 5 nF, which is possible on chip, but typically impractical, reduces Δv_O further to the 38-mV (±1.5%) ripple shown in Fig. 2, which is more acceptable.

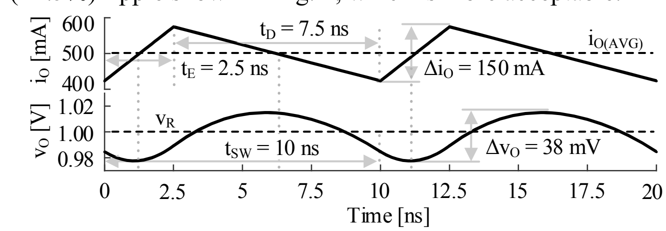

Fig. 2. Current and voltage waveforms of the basic buck at 100 MHz.

This paper explores how to suppress these ripples in switched-inductor supplies so that both L_X and C_O can be on chip and switch at practicable frequencies. To this end, Sections II–V describe and compare ripple suppressors. Section VI then draws and summarizes relevant conclusions.

II. Multiphase Cancellation

A. Operation

Since multiphase converters feed out-of-phase inductor currents into one output, current ripples tend to cancel [19]. Cancellation is nearly perfect when feeding two 50% duty-cycled phases, which only happens when v_O is half of v_{IN} in bucks [20]. Cancellation deteriorates as duty cycle d_E deviates.

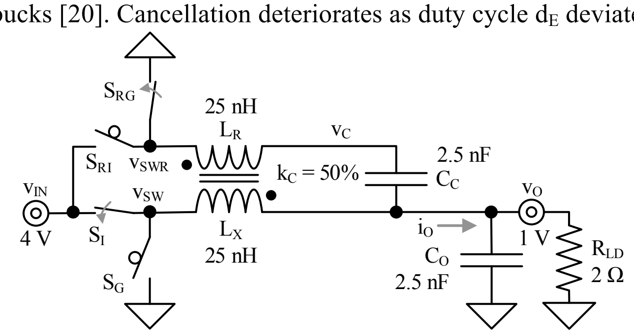

Fig. 3. Magnetically-coupled multiphase buck.

A replica, but complementary-phased inductor L_R, however, can produce an equal, but opposite-phased ripple current that, when coupled into v_O like C_C in Fig. 3 shows, can cancel the ripple of a switched power inductor L_X [2], [21]–[22]. For perfect cancellation, L_R must drain with the same voltage that L_X energizes, and *vice versa*. Plus, C_C must not alter the ripple that L_X produces and injects into v_O.

This works because L_R and L_X are dc shorts, v_{SWX}'s average $v_{SWX(AVG)}$ and v_O are duty-cycled fractions of v_{IN}: $v_{IN}d_E$, and v_{SWR}'s average $v_{SWR(AVG)}$ and v_C are complementary fractions: $v_{IN}(1 - d_E)$. So as L_X energizes with $v_{IN} - v_{IN}d_E$, L_R drains with $-(1 - d_E)v_{IN}$ or $-v_{IN} + d_Ev_{IN}$. And L_X drains with $-v_{IN}d_E$ as L_R energizes with $v_{IN} - (1 - d_E)v_{IN}$ or d_Ev_{IN}. This way, when C_C keeps v_C steady at $v_{SWR(AVG)}$, the current ripples cancel.

In the case of on-chip inductors, L_X and L_R are very low, so their current ripples are very high. Although this does not affect their cancellation, L_X's and L_R's series resistances R_{LX} and R_{LR} can burn substantial power. The purpose of the magnetic coupling between L_X and L_R is to *couple* voltages that oppose. That way, with lower effective voltages across the *intrinsic* inductors, their currents ripple less, and as a result, burn less RMS power [21]–[23]. Even if the coupling factor k_C is low at 10%, the effect is to reduce the ripple. Since L_X and L_R are both on the same chip, coupling them is possible [21].

B. Sensitivity

As long as inductor voltages and inductances match, cancellation is perfect. But for that, v_C must be as steady as its complementary counterpart v_O, which without ripple current into C_O, hardly ripples. So cancellation is perfect only when C_C is nearly infinite. This is why the current ripple Δi_O in Fig. 4 is never zero and falls with higher C_C's.

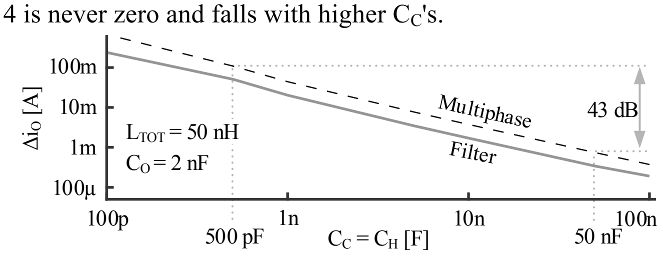

Fig. 4. Multiphase and filter sensitivity to coupling and holding capacitance.

Perfect cancellation also presupposes L_X and L_R match perfectly, which is not true in practice. ±5% mismatch when C_C is 100 µF, for example, produces a 22-mA ripple Δi_O, as Fig. 5 shows. Interestingly, this mismatch can oppose the effect of a lower C_C. So a 20% higher L_R can reduce the 110-mA ripple that an on-chip 500-pF C_C produces in Fig. 4 to 23 mA.

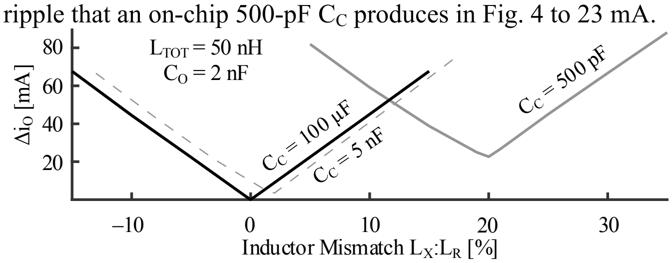

Fig. 5. Multiphase sensitivity to inductor mismatch.

III. Shunt-Filtered Removal

A. Operation

When tuned, filters can suppress ripples with less inductance and capacitance than the buck in Fig. 1 can. The series LC resonator in [24], for example, phase-shifts and cycles back some of the ripple energy that C_O would otherwise receive. Unfortunately, the resonator slows the response of the power supply [25]–[26]. Plus, the resonator's sinusoidal current cannot completely cancel L_X's triangular ripple.

The shunt filter in Fig. 6, however, can cancel the ripple [27]. For this, L_S drops a voltage-divided fraction of the switching voltage v_{SW} that matches the coupled voltage that L_{XO} drops. So the opposing magnetic action between L_X and L_{XO} couples a voltage into L_{XO} that cancels the voltage that L_S imposes. This way, L_{XO} outputs a non-rippling current i_O.

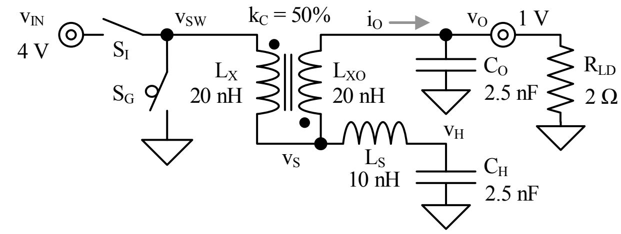

Fig. 6. Magnetically-coupled shunt-filtered buck.

L_S essentially shunts L_X's ripple current and L_{XO} steers L_X's average dc component into v_O. For L_S to conduct as much ripple as L_X, L_S should match L_X's coupled reflection k_CL_X in L_{XO} [28]. This way, L_S drops a full k_C fraction of L_X's voltage to sink as much current ripple as L_X. [29] applies similar concepts, but requires another capacitor.

B. Sensitivity

Ripple removal is perfect when the voltage v_H across the holding capacitor C_H is perfectly steady. But since on-chip capacitance is so low, v_H fluctuates and produces a variation in the current that L_S shunts, and as a result, the current that L_{XO} outputs. This is why L_{XO}'s current ripple Δi_O in Fig. 4 rises from 190 µA to 240 mA when C_C falls from 100 nF to 100 pF.

Inductor mismatch also produces an imbalance that keeps L_{XO}'s voltages from cancelling. ±5% mismatch when C_C is 100 µF, for example, produces a 4-mA ripple, like Fig. 7 shows. This imbalance, however, can offset the effect of a lower C_H. So a 49% higher L_S can reduce the 51-mA ripple that an on-chip 500-pF C_C produces in Fig. 4 to 9.9 mA.

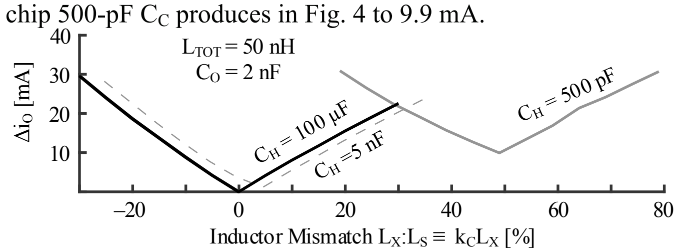

Fig. 7. Filter sensitivity to inductor mismatch.

IV. Analog Cancellation

A. Operation

Another way to cancel current ripple is to construct a complementary, inductor-like ripple with analog circuits [8]. A feedback loop, for example, can sense C_O's voltage ripple and output a current that opposes that ripple [30]. This reduces the ripple, but not below the offset that the loop's delay allows.

Feed-forwarding an inductor-like ripple is better because a tunable delay block can eliminate the phase difference between the two paths. For this to work, the circuit must predict (rather than sense) the current ripple. But since the voltages that establish the ripple (v_{IN} and v_O) are available, and inductance is largely static, predicting the ripple is possible.

In Fig. 8, for example, the digital signal v_{SW}' fed to G_I produces a duty-cycled current into C_I that generates a triangular voltage ripple v_I that G_O then converts into a current i_{GO} [31]. Since i_{GO}'s duty cycle matches that of L_X's current i_{LX} and G_O inverts the ripple, i_{GO} can cancel i_{LX}'s ripple Δi_{LX}. The cancellation is perfect when i_{GO}'s amplitude and phase match Δi_{LX}'s, which happens when G_I and G_O's gain and delay match L_X's. [6]–[7] and [25]–[26] similarly feed-forward signals that cancel i_{LX}'s ripple, but with large transformers.

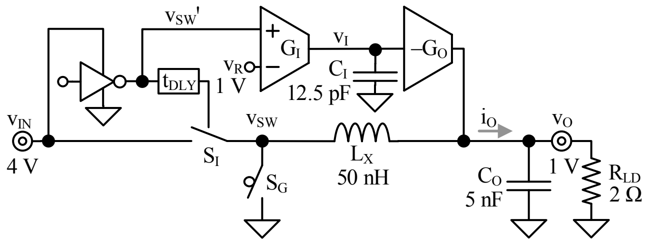

Fig. 8. Analog feed-forward cancellation of the basic buck.

v_{SW}' swings between v_{IN} and ground like v_{SW}. Since G_I's inverting input-reference v_R matches v_O's target, G_I's positive and negative input voltages $v_{IN} - v_R$ and $-v_R$ match L_X's energizing and drain voltages $v_{IN} - v_O$ and $-v_O$. This way, G_I processes the same voltage v_L that S_I and S_G impress across L_X. So when G_IG_O/C_I matches $1/L_X$, i_{GO} is equal, but opposite Δi_{LX}:

$$i_{GO} = -\frac{v_L G_I G_O}{sC_I} \equiv -\Delta i_{LX} = -\frac{v_L}{sL_X}. \quad (1)$$

Since G_I and G_O delay i_{GO}'s feed-forward action, the purpose of the delay block t_{DLY} is to delay L_X's v_{SW} by the same time.

B. Sensitivity

Cancellation is perfect when G_I and G_O's gain and delay match L_X's. Of these, cancellation is more sensitive to delay mismatch. For example, ±5% delay mismatch (from Fig. 9) produces a 15× greater ripple Δi_O than gain error. Cancellation is so sensitive to delay that mismatches over ±10% output more ripple than the basic buck. In other words, the benefits of suppression disappear beyond ±10%. This is why tuning t_{DLY} is necessary. Although tracking L_X's drift over time and temperature also helps, the effect of this gain error is lower.

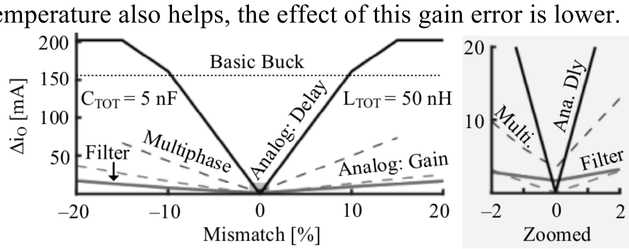

Fig. 9. Sensitivity to mismatch.

IV. Comparison

A. Load

Although the principle aim of a power supply is to feed and satisfy a load, the operational objective of the control loop is to regulate the output voltage v_O. So what ultimately matters most is voltage ripple Δv_O. Output current ripple Δi_O is critical in this respect because Δi_O into output capacitance C_O produces Δv_O. The load is also important because it can alter how much current C_O receives and how much v_O ripples.

Since v_O ripples in practice, loading the output with a resistive load R_{LD} introduces a load ripple Δi_{LD} or $\Delta v_O/R_{LD}$. Fortunately, this current ripple draws more current when v_O rises and less current otherwise. So the net effect is to oppose v_O's unloaded ripple. This is why Δv_O in Fig. 10 is lower with heavier resistive loads (i.e., lower R_{LD}'s). The benefit of R_{LD}, however, disappears when R_{LD} surpasses 1 Ω. In other words, Δi_O is so much greater than Δi_{LD} at and past this point that Δi_{LD} produces negligible variations in C_O's current and Δv_O.

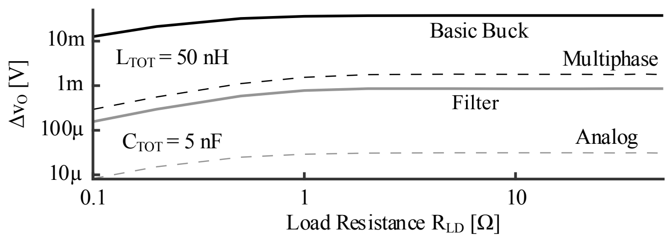

Fig. 10. Sensitivity to load resistance.

B. Integration

With 50 nH of total inductance L_{TOT} and 5 nF of total capacitance C_{TOT}, analog cancellation can suppress the current ripple of a basic buck the most by 65 dB, whereas multiphase and filtered schemes reduce the ripple by, at most, 28–34 dB. This is, in part, because multiphase and filtered circuits share L_{TOT}, so their power inductor L_X is only a fraction of L_{TOT}. As inductance climbs, however, like Fig. 11 illustrates, multiphase and filtered suppression improve more than analog cancellation does. So much so that suppression is nearly the same for all three with 1 μH. In other words, analog cancellation is more effective than the others when total inductance is lower, as in the case of on-chip inductors.

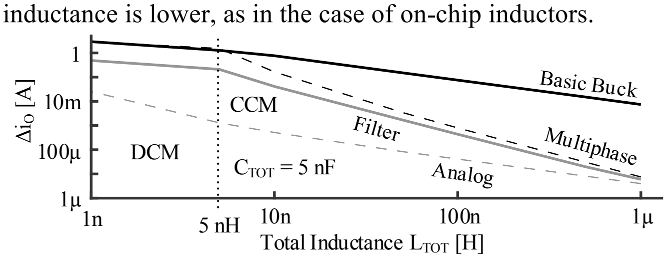

Fig. 11. Sensitivity to total inductance.

When L_{TOT} falls below 5 nH, L_X's current i_{LX} fluctuates so much that i_{LX} is no longer triangular like in Fig. 2. Below 5 nH, L_X conducts current discontinuously (in discontinous conduction mode: DCM). With so much nonlinearity, the cancelling effects of the multiphase circuit vanish. The analog circuit also suffers, but gradually. So even with 1 nH, the ripple is 41 dB below the basic buck's. Although the filter does not suffer, the ripple is 21 dB higher than the analog's 1-nH level. Analog cancellation still works well in DCM because the circuit reconstructs the cancellation current from the same operating conditions that produce L_X's DCM ripple.

Since ripple suppressors distribute total capacitance C_{TOT} differently, on-chip integration of capacitance does not limit the schemes in the same way. Multiphase and filter strategies, for example, rely on coupling and holding capacitors C_C and C_H to suppress Δi_O. Ripple suppression is highest when C_O and C_C or C_H share C_{TOT} equally. This way, raising C_C and C_H by 40 dB from 250 pF to 25 nF suppresses Δi_O by nearly the same amount: 37–40 dB, and raising C_O by 40 dB from 250 pF to 25 nF reduces Δi_O's impact on Δv_O by another 40 dB or so. So combined, Δv_O in Fig. 12 is 73–78 dB lower.

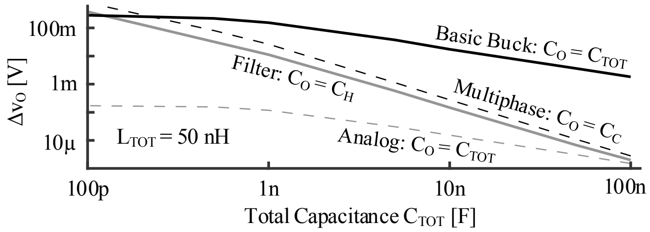

Fig. 12. Sensitivity to total capacitance.

C_O is the only power capacitor in the analog scheme, and as a result, the sole beneficiary of additional C_{TOT}. Since C_O does not alter the cancellation current, increasing C_O has little effect on Δi_O. Doing so, however, still reduces Δi_O's impact on Δv_O, so raising C_O by 40 dB from 500 pF to 50 nF suppresses Δv_O in Fig. 12 by 34 dB. The improvement is so much lower than the multiphase and filter schemes that suppression is the same for all three at 100 nF. In other words, analog cancellation is more effective when capacitance is lower: with on-chip capacitors.

With 50 nF of off-chip capacitance, the multiphase and filter strategies suppress the basic buck's Δi_O by 48–53 dB and Δv_O by 51–55 dB. But when constrained to 500 pF, the suppression falls to 6.8–8.7 dB, like Table I shows. Since Δi_O reduction in the analog scheme is much more effective and at the same time also indepedent of C_O, Δi_O and Δv_O are 65 and 62–63 dB lower than the basic buck's, irrespective of C_O. In other words, on-chip integration reduces the effectiveness of the multiphase and filter circuits, but not that of the analog's.

TABLE I: PERFORMANCE SUMMARY

	Buck		Multiphase		Filter		Analog	
	Δi_O [mA]	Δv_O [mV]	Δi_O [mA]	Δv_O [mV]	Δi_O [mA]	Δv_O [mV]	Δi_O [mA]	Δv_O [mV]
Nominal	151	37.4	6.15	1.13	3.05	0.57	0.08	0.03
+5% Mismatch	–	–	26.9	14.0	5.47	2.01	7.14*	1.78*
–5% Mismatch			21.0	15.6	4.54	3.28	7.95*	1.97*
+20% L_{TOT}	125	31.0	4.26	1.12	2.04	0.51	25.0	6.23
–20% L_{TOT}	189	46.7	8.20	5.16	3.71	2.25	37.5	9.39
L_{TOT} = 50 nH	151	37.4	3.46	1.66	1.7	0.86	0.08	0.03
L_{TOT} = 5 µH	0.50	0.37	0.001	0.0007	0.001	0.005	0.0008	0.0003
C_{TOT} = 500 pF	153	219	58.3	80.6	25.7	32.1	0.09	0.16
C_{TOT} = 50 nF	149	3.63	0.60	0.01	0.35	0.01	0.08	0.003
R_{LD} = 100 mΩ	150	12.7	3.51	0.29	1.71	0.16	0.08	0.008
R_{LD} = 50 Ω	151	37.7	3.37	1.78	1.69	0.86	0.08	0.03
Additional Components	–		S_{IR}, S_{GR}, L_R, and C_C		L_{XO}, L_S, and C_H		G_I, C_I, and G_O	

*Tuned delay with ±5% drift in inductance or ±5% mismatch in gain.

Analog cancellation is so effective that 2-MHz operation is possible with practical on-chip components. i_O in Fig. 13, for example, ripples across 9.6 mA with 50 nH and v_O ripples across 19 mV with 500 pF. Current ripple is so high in the multiphase and filtered circuits that the power inductor cannot conduct continuously (in continuous conduction mode: CCM).

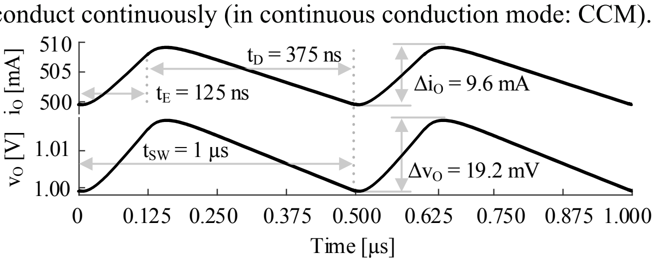

Fig. 13. Current and voltage waveforms with analog cancellation at 2 MHz.

C. Sensitivity

All schemes ultimately rely on matching components to cancel the current ripple. Unfortunately, components do not match perfectly. In the analog circuit, ±5% gain mismatch or ±5% drift in inductance magnifies Δi_O by 99× and Δv_O by 66× (in Fig. 9). ±5% inductance mismatch in the multiphase scheme has less impact: Δi_O climbs up to 4.4× and Δv_O up to 14×. The effect is even lower in the shunt filter with ±5% mismatch in inductance: Δi_O rises up to 1.8× and Δv_O up to 5.8×.

±1% mismatch in delay in the analog scheme amplifies Δi_O by 200× and Δv_O by 190×. With this mismatch, current and voltage ripples Δi_O and Δv_O are up to 12× greater than in the filter. The benefits of analog cancellation over the filter therefore disappear with ±1% delay mismatch, like Fig. 9 shows. This is why tuning delay (by for example, adjusting capacitance or the number of inverters in a chain of inverters) is a requirement for the analog scheme.

D. Power Consumption

Switches require gate-drive power and equivalent series resistances in power inductors and capacitors burn ohmic power. Relative to the basic buck, the shunt filter uses three additional passive components: L_{XO}, L_S, and C_H, but no additional switches. Although the multiphase circuit uses one less: L_R and C_C, two more switches are necessary: S_{IR} and S_{GR}. So of these, multiphase cancellation consumes more power.

Analog cancellation does not require additional power switches or passive components (because C_I does not conduct much current and is therefore small). Output transconductor G_O, however, conducts as much ripple current as the power inductor L_X, so G_O consumes analog power. This power is significant because G_O supplies current across v_{IN} and v_O and sinks current across v_O and ground. So the transistors that carry this current drop $v_{IN} - v_O$ and v_O, which are substantially higher voltages than power switches would. Analog cancellation can therefore require more power than the other two schemes.

V. CONCLUSIONS

Analog cancellation is 38× more effective in suppressing current ripple Δi_O than the shunt filter and 77× more effective than multiphase cancellation. Unfortunately, the analog circuit is also 55× and 23× more sensitive to ±5% gain mismatch and drift. So without tracking inductance, the shunt filter is the most effective. However, when constrained to 50 nH and 500 pF, Δi_O is so great in the shunt filter that operation at low frequencies is not possible. The analog scheme is the only one that can keep voltage ripple within ±20 mV at 2 MHz with on-chip components (50 nH and 500 pF), albeit at the expense of analog power. Irrespective of the means and values used (for capacitance, inductance, and frequency), as long as the design is optimal for those values, ripple noise and power efficiency ultimately deteriorate with integration. While analog cancellation favors noise reduction the most, shunt-filtering the current ripple balances noise and power better.

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