# How to Design Battery-Assisted Photovoltaic Switched-Inductor CMOS Charger–Supplies

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Abstract—Wireless microsensors can sense and share data that can save lives, energy, and money. Recharging or replacing thousands of tiny, easily exhaustible batteries, however, is too costly. Fortunately, photovoltaic (PV) cells can generate 100× more power from sunlight than other transducers can from motion, heat, or radiation. But since PV cells cannot supply the milliwatts that microsystems can at times require, this paper shows how to design battery-assisted PV-sourced CMOS charger–supplies that supply PV power to the system, excess PV power to the battery, and battery power to the system when PV power is insufficient. The design process proposed accounts for power losses and silicon area. This way, simulations show that 10% of losses are from switches when inductor resistance R<sub>ESR</sub> is 2.2  $\Omega$  and silicon area can be 80% smaller when R<sub>ESR</sub> is 5.5  $\Omega$ .

# Index Terms—Charger, harvester, light energy, photovoltaic (PV), power supply, switched inductor, microsensor, microsystem.

#### I. BATTERY-ASSISTED MICROSYSTEMS

Microsensors can add life-, energy-, and cost-saving intelligence to homes, hospitals, factories, and cities [1]–[6]. But since tiny batteries deplete easily, life times can be short and recharge cycles frequent. And the cost of recharging or replacing thousands of nodes is excessive. Fortunately, ambient energy is often abundant, and as a result, able to repeatedly replenish the energy that the batteries lose.

Photovoltaic (PV) cells, for example, can output  $100 \times$  more power from sunlight than competing transducers can from motion, heat, or radiation [3]–[6]. But since light is not always available, and modern microsensors can at times require milliwatts to operate [1], the system in Fig. 1 draws assistance from a battery v<sub>BAT</sub>. Here, the charger–supply draws PV power P<sub>PV</sub>, draws and replenishes battery power P<sub>BAT</sub>, and supplies system power P<sub>SYS</sub> to the sensor, digital-signal processor (DSP), transmitter, and other subsystems.



Fig. 1. Battery-assisted photovoltaic-sourced wireless microsensor

Although linear supplies can transfer and condition power, linear circuits usually lose more power than switched topologies [2]. And unlike switching circuits, linear circuits cannot supply higher voltages. Of switching options, switched capacitors normally require many more switches than switched inductors, so switched inductors typically lose less ohmic and gate-drive power [6]–[7]. This is why the charger–supplies discussed here are switched inductors.

The aim of this presentation is to show how to design switched-inductor charger–supplies, which is absent in literature. For this, Section II first explains how to configure the switching network. Then, with Section III's foundation on CMOS switches, Sections IV and V show and simulate how NFETs and PFETs can realize low-loss and area-efficient charger–supplies. Section VI closes with conclusions.

#### **II. SWITCHING NETWORKS**

The role of the switching network in a charger–supply is to energize and drain an inductor  $L_X$  from a source into an output. With a battery-assisted photovoltaic (PV) source  $v_{PV}$ , the network should be able to draw and supply power from  $v_{PV}$  and  $v_{BAT}$  to the load at  $v_O$  and  $v_{BAT}$ . Here, drawn battery power  $P_{B(AID)}$  supplements  $v_{PV}$ 's  $P_{PV}$  to supply a heavy load and excess PV power  $P_{B(CHG)}$  from a light load charges  $v_{BAT}$ .

#### A. Non-Reversing Switched-Inductor Charger–Supply

The non-reversing inductor  $L_X$  in Fig. 2 [8]–[12] steers power in one direction only. To derive and supply power from  $v_{PV}$ and  $v_{BAT}$  to  $v_O$  and  $v_{BAT}$ , switches  $S_{PV}$  and  $S_{B(AID)}$  connect the receiving terminal of  $L_X$  at  $v_{SW1}$  to  $v_{PV}$  and  $v_{BAT}$  and  $S_O$  and  $S_{B(CHG)}$  connect the supply terminal at  $v_{SW2}$  to  $v_O$  and  $v_{BAT}$ . This way, and with ground switches  $S_{G1}$  and  $S_{G2}$ ,  $S_{PV}$ – $S_{G2}$ energize  $L_X$  from  $v_{PV}$  and  $S_{G1}$ – $S_O$  drain  $L_X$  into  $v_O$  and  $S_{G1}$ –  $S_{B(CHG)}$  into  $v_{BAT}$ . Similarly,  $S_{B(AID)}$ – $S_{G2}$  energize  $L_X$  from  $v_{BAT}$  and  $S_{G1}$ – $S_O$  drain  $L_X$  into  $v_O$ .



Fig. 2. Non-reversing switched-inductor charger-supply.

#### B. Reversing Switched-Inductor Charger-Supply

The reversing inductor  $L_{\rm X}$  in Fig. 3 [13]–[14] conducts in both directions.  $L_{\rm X}$  steers PV power  $P_{\rm PV}$  to the right to  $v_{\rm O}$  and  $v_{\rm BAT}$  and battery-assistance power  $P_{B(AID)}$  to the left to  $v_{\rm O}$ . So  $S_{\rm PV},\,S_{O(SUP)}$ , and  $S_{\rm B}$  connect  $L_{\rm X}$  from  $v_{\rm PV}$  to  $v_{\rm O}$  and  $v_{\rm B}$  and  $S_{O(AID)}$  from  $v_{\rm BAT}$  to  $v_{\rm O}$ . This way, and with ground switches  $S_{G1}$  and  $S_{G2},\,S_{\rm PV}{-}S_{G2}$  energize  $L_{\rm X}$  from  $v_{\rm PV}$  and  $S_{G1}{-}S_{O(SUP)}$  drain  $L_{\rm X}$  into  $v_{\rm O}$  and  $S_{G1}{-}S_{\rm B}$  into  $v_{\rm BAT}$ . Similarly,  $S_{B}{-}S_{G1}$  energize  $L_{\rm X}$  from  $v_{\rm BAT}$  and  $S_{G2}{-}S_{O(AID)}$  drain  $L_{\rm X}$  into  $v_{\rm O}$ .



Fig. 3. Reversing switched-inductor charger-supply.

# **III. CMOS SWITCHES**

Ideal switches occupy no space, drop no voltage, leak no current, and respond instantly. In practice, however, switches occupy space and incorporate resistance, capacitance, and leakage paths. So in addition to requiring space, they also drop voltages, leak currents, and require time to respond.

### A. Synchronous Switches

<u>MOSFETs</u>: NFETs and PFETs in Fig. 4a–b are *synchronous* devices because they transition between on–off states when prompted by synchronizing gate signals. They can drop 10–200 mV in the on state and respond in nanoseconds. Since current can flow in both directions, either terminal can serve as the *source*. In the off state, their body diodes can always conduct current: substrate NFETs from the grounded substrate and welled PFETs into the well.



<u>Blocking MOSFETs</u>: Isolating the bulk of welled FETs and blocking the bulk path with opposing diodes keep body diodes from leaking current. The body diodes of the in-line pair  $M_{P1}-M_{P2}$  in Fig. 4c, for example, block one another, so they cannot conduct. This way, when  $M_{P1}-M_{P2}$  close, switch terminals bias the bulk  $v_B$  within mV's of their terminal potentials. And when  $M_{P1}-M_{P2}$  open, bulk capacitance holds  $v_B$ , or if either switch terminal rises, the diode attached to that terminal raises and biases  $v_B$  to the higher potential.

With the body always biased close to the higher potential, the welled FETs do not suffer bulk effect when conducting. However, two switches offer twice  $2\times$  the resistance or twice  $2 \times$  the capacitance of one switch. This is a drawback because higher resistance burns more ohmic power and higher capacitance requires more gate-drive power [15].

Biasing the bulk with off-line FETs eliminates the second in-line FET. Off-line cross-coupled pair  $M_{X1}-M_{X2}$  in Fig. 4d, for example, biases  $M_P$ 's bulk  $v_B$  to the highest potential:  $M_{X1}$  to  $v_{S/D}$  when  $v_{S/D}$  exceeds  $v_{D/S}$  and  $M_{X2}$  to  $v_{D/S}$  otherwise. The drawback is that  $M_{X1}-M_{X2}$  are off when terminal voltages are within a threshold of one another, so body diodes bias  $v_B$  to the higher potential. This means,  $v_B$  may not rise as quickly as the higher potential. Fortunately, this is only momentary.

#### B. Asynchronous Switches

Diodes and diode-connected FETs in Fig. 5a–b are *asynchronous* because they close and open automatically when current flows and reverses. In other words, they do not require a synchronizing signal. They can drop 0.5-0.7 V in the on state and respond in nanoseconds.



Threshold-shifted [15] and comparator-synchronized [15] FETs in Fig. 5c–d can drop much lower voltages. But since matching and tracking a threshold voltage  $v_T$  across process and temperature is less accurate than sensing a voltage difference, comparator-synchronized FETs drop lower voltages. The drawback is that the comparator requires  $\mu$ W's to respond within 1  $\mu$ s [11]. Still, the mW's saved with a lower voltage drop outweigh the  $\mu$ W's lost in the comparator.

#### C. Low-Loss MOSFETs

Transistors consume ohmic power  $P_R$  when they conduct and require gate-drive power  $P_G$  to switch between states [15]. Interestingly, resistance falls and capacitance climbs with wider channels. So channel widths should be just high enough for the rise in  $P_G$  to cancel the fall in  $P_R$  [16]. And channel lengths should be as short as possible because both resistance and capacitance climb with channel length.

In practice, gate signals across the circuit crisscross during transitions. As a result, adjacent switches momentarily short the inputs and outputs to which they connect. This is a problem because, when optimized like just described, resistances are so low that they can burn excessive power when they short. This is why designers insert dead-time periods between the gate signals of adjacent switches [15].

#### IV. CMOS CHARGER-SUPPLIES

The most important difference between switched inductors in Section II is voltage swing because capacitances require more gate-drive power to charge across higher voltages. Although  $v_{SW2}$  in both networks swings to  $v_0$  and  $v_{BAT}$ ,  $v_{SW1}$  in the non-reversing inductor of Fig. 2 swings to  $v_{PV}$  and  $v_{BAT}$  and in the reversing case of Fig. 3 to  $v_{PV}$  and  $v_0$ . So when  $v_{PV}$  is less

than  $v_O$  and  $v_{BAT}$ , which is often the case [5], and  $v_O$  is greater than  $v_{BAT}$ , the non-reversing scheme swings and consumes less than the reversing counterpart, and *vice versa*. This means, the non-reversing topology is more efficient when  $L_X$ boosts  $v_{PV}$  and  $v_{BAT}$  to  $v_O$  and the reversing inductor is more efficient when  $L_X$  boosts  $v_{PV}$  and bucks  $v_{BAT}$  to  $v_O$ . This is why simulated losses in Fig. 6 are increasingly higher for the non-reversing case when  $v_{BAT}$  climbs above  $v_O$ 's 1 V to 1.8 V.



Fig. 6. Simulated switch losses for reversing and non-reversing inductors.

#### A. Boost–Boost Charger–Supply

<u>Headroom</u>: Since stacked PV cells lose space and mismatch power between cells [5],  $v_{PV}$  is usually one PV cell at 0.4–0.5 V.  $v_0$  is usually so high in boost–boost applications that  $v_0$ gated NFETs at  $v_{PV}$  in Fig. 2 offer much less resistance and capacitance than ground-gated PFETs. This is why  $S_{PV}$  is an NFET  $M_{PV}$  in the boost–boost charger–supply of Fig. 7.





When  $v_0$  is the highest voltage,  $v_0$ -gate NFETs at  $v_0$  are ineffectual, so  $S_0$  in Fig. 2 is a PFET  $M_0$  in Fig. 7 with its bulk at  $v_0$ . Similarly, ground switches are NFETs  $M_{G1}$  and  $M_{G2}$  because ground-gate PFETs cannot close. Since  $v_{BAT}$  can be between  $v_{PV}$  and  $v_0$  in boost-boost cases,  $v_{BAT}$  switches  $S_{B(AID)}$  and  $S_{B(CHG)}$  can include both NFETs and PFETs.

<u>Dead-Time Paths</u>: The circuit should conduct  $L_X$ 's current  $i_L$  across dead-time periods  $t_{DT}$  to the highest and lowest potentials available. Fortunately, NFETs at  $v_{SW1}$  incorporate grounded body diodes that can feed  $L_X$  across  $t_{DT}$ . Since  $v_O$  is the highest potential in boost–boost applications,  $v_O$ 's  $M_O$  incorporates a body diode that can similarly steer  $i_L$  to  $v_O$ .  $M_{BP(CHG)}$ 's body diode to  $v_{BAT}$ , however, should not conduct. This is why cross-coupled FETs block  $M_{BP(CHG)}$ 's diodes.

<u>Protection</u>: Although  $i_L$  should always flow to the right, the controller might inadvertently allow  $i_L$  to reverse. Connecting  $M_{BP(AID)}$ 's bulk to  $v_{BAT}$  both eliminates its bulk effect and introduces a body diode that can steer reverse  $i_L$  to  $v_{BAT}$ . NFETs at  $v_{SW2}$  incorporate grounded diodes that can similarly feed  $L_X$  when  $i_L$  reverses.

#### B. Boost–Buck Charger–Supply

<u>Headroom</u>: Since  $v_{BAT}$  is higher than  $v_O$  in boost–buck applications,  $L_X$  in Fig. 3 can energize directly into  $v_O$ . That means,  $S_B$  and  $S_{O(AID)}$  can energize  $L_X$ , instead of  $S_B$  and  $S_{G1}$ .  $S_{G1}$  is therefore unnecessary in Fig. 8. And  $v_{PV}$  is so low [5] and  $v_{BAT}$  so high that  $v_{BAT}$ -gated NFETs at  $v_{SW1}$  offer much less resistance and capacitance than ground-gated PFETs, so  $S_{PV}$  is an NFET  $M_{PV}$ . With no voltage higher than  $v_{BAT}$ ,  $v_{BAT}$ gate NFETs at  $v_{BAT}$  are ineffectual, so  $S_B$  is a PFET  $M_B$  with its bulk at  $v_{BAT}$ . Ground switch  $S_{G2}$  is an NFET  $M_{G2}$  because ground-gate PFETs cannot close.  $v_O$  switches  $S_{O(AID)}$  and  $S_{O(SUP)}$ , however, can incorporate NFETs and PFETs because  $v_O$  can be anywhere between  $v_{PV}$  and  $v_{BAT}$ .



Fig. 8. Boost-buck switched-inductor CMOS charger-supply.

<u>Dead-Time Paths</u>: The circuit should conduct  $i_L$  across dead-time periods  $t_{DT}$  to the highest and lowest potentials available. NFETs at  $v_{SW1}$  incorporate grounded body diodes that can feed  $i_L$  and PFET  $M_{OP(AID)}$ 's diode can sink  $i_L$  into  $v_O$ , the highest potential at  $v_{SW1}$ . NFET diodes at  $v_{SW2}$  can similarly feed  $i_L$  and PFET  $M_B$ 's diode sink  $i_L$  into  $v_{BAT}$ , the highest potential at  $v_{SW2}$ .  $M_{OP(SUP)}$ 's diode to  $v_O$  at  $v_{SW2}$  should not conduct, so cross-coupled FETs block  $M_{OP(SUP)}$ 's diodes.

#### V. DESIGN VARIATIONS

#### A. Asynchronous Simplifications

Non-reversing switches that conduct dead-time currents in the same direction can be diodes. Ground and  $v_O$  FETs  $M_{G1}$  and  $M_O$  in the boost–boost of Fig. 7 and  $v_O$  FETs in the boost–buck of Fig. 8  $M_{OP(AID)}$  and  $M_{ON(AID)}$ , for example, conduct  $i_L$  in and out of dead time in one direction. So diode or diode equivalents can replace them like Figs. 9 and 10 show.



Fig. 9. Simplified boost-boost switched-inductor CMOS charger-supply.

#### B. Gate-Drive Simplifications

If  $v_{BAT}$  is low and well below  $v_O$  in the boost–boost of Fig. 7,  $v_{BAT}$ 's ground-gate PFETs  $M_{BP(AID)}$  and  $M_{BP(CHG)}$  can be much more resistive than  $v_O$ -gate NFETs. So removing these

PFETs like Fig. 9 shows can be as efficient with less area. Without  $v_{SW1}$ 's  $M_{BP(AID)}$ , however, reverse  $i_L$  has no path, so adding a protection diode  $D_X$  to  $v_{BAT}$  in Fig. 9 is prudent.



Fig. 10. Simplified boost-buck switched-inductor CMOS charger-supply.

 $v_{\rm O}{\rm s}~v_{BAT}{\rm -}$ gate NFETs in the boost–buck of Fig. 8 can similarly lose more power than ground-gate PFETs when  $v_{BAT}$  falls towards  $v_O$ , like Fig. 11 shows. So if  $v_O$  is high and close to  $v_{BAT}$ , removing  $v_O$  NFETs  $M_{ON(AID)}$  and  $M_{ON(SUP)}$  like Fig. 10 shows can be as efficient with less area. And if close enough to  $v_{BAT}$ , bulk effect in  $v_O$  PFET  $M_{O(SUP)}$  from connecting its bulk to  $v_{BAT}$  might not be significant.



Fig. 11. Simulated NFET and PFET losses in  $S_{\mathrm{O}(\mathrm{AID})}$  from the boost–buck.

# C. Inductor ESR Considerations

High-inductance  $L_X$ , low-resistance  $R_{ESR}$  inductors transfer lots of power with little losses. More turns and thicker coils, however, require more space. So tiny inductors burn more power with higher  $L_X$ . And as  $R_{ESR}$  losses in  $P_{ESR}$  climb, switch losses  $P_{SW}$  are less significant. As a result, the loss savings of a low-loss network diminish with higher  $R_{ESR}$ . So although the reversing scheme in Fig. 3 is up to 5% more efficient with low  $R_{ESR}$  in Fig. 12, the non-reversing case in Fig. 2 [12] is nearly as efficient above 2.2  $\Omega$ .



Fig. 12. Simulated savings of the reversing over non-reversing schemes.

Since switch losses lose significance with high  $R_{ESR}$ , silicon area becomes more important. So instead of using low-loss channel widths, which balance ohmic and gate-drive losses [16], switches can be narrower, and therefore, smaller. By keeping fractional switch losses at 10%, for example, switches in the reversing circuit of Fig. 3 occupy up to 20000

 $\mu$ m<sup>2</sup> or 80% less silicon area when R<sub>ESR</sub> is greater than 5.5  $\Omega$ , as Fig. 12 demonstrates.

## VI. CONCLUSIONS

This paper shows how to design low-loss battery-assisted photovoltaic-sourced CMOS charger–supplies. And that nonreversing switched inductors are less lossy than the reversing counterparts when the output voltage is greater than the battery voltage, and *vice versa* otherwise. Headroom, deadtime currents, and reverse-current protection dictate which and how FETs should switch the network. Unidirectional switches that conduct dead-time currents in the same direction can be diodes or diode-emulating FETs. But as inductor resistance and losses climb, the benefits of low-loss CMOS choices diminish. In these cases, switches can be lossier, and as such, occupy up to 80% less silicon area.

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