Efficiency of Switched-inductor DC–DC Converter ICs across Process Technologies

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***Abstract*—Battery-powered electronics rely on integration and power efficiency for size and operational life. Switched-inductor converters play a critical role in this because most portable systems depend on dc–dc converters to supply power efficiently. Understanding the collective impact of shrinking dimensions on total power losses in a switching converter is therefore important when selecting a process technology for the power-supply chip, because the optimal choice results in longer battery life. This paper analyzes and validates the effects of finer CMOS technologies (which feature shorter minimum channel lengths L_{MIN}, higher oxide capacitance, and lower breakdown voltages) on the efficiency performance of switched-inductor dc–dc converters in continuous- and discontinuous-conduction modes (CCM and DCM). Simulation results show that conduction and gate-drive losses in switches rise with $L_{MIN}^{1.5}$ and bias and bandwidth-critical quiescent losses with L_{MIN} and L_{MIN}^{3}, respectively. In other words, because parasitic components and gate-drive voltages rise with L_{MIN}, efficiency drops with coarser technologies: E.g., the efficiencies of optimized 0.18-, 0.35-, and 0.5-µm buck converters peaked at 93%, 89%, and 79%.**

I. Integrated Supplies

As the appeal for and utility of portable electronics like smart phones and digital assistants rise, their functionality continues to expand [1]. Unfortunately, performing more tasks demands more power, and more power translates to shorter battery life. Reducing power losses in portable devices is therefore imperative, which is why many supply systems employ switched-inductor dc–dc converters to deliver power [2]–[3].

Integrating these switching converters on chip saves real estate in the printed-circuit board (PCB) and improves output regulation (i.e., accuracy) [4]–[5]. In selecting the process technology with which to build the supply chip, designers often base their decision on cost, breakdown voltage, and efficiency. However, while many applications and markets can afford to sacrifice efficiency for cost and breakdown voltage, many emerging mobile systems cannot.

By adopting transistor-stacking and partial gate-drive techniques [6]–[7] that protect low-voltage transistors from battery-level voltages, designers can now favor efficiency over other factors when choosing a technology. For this purpose, and because published literature excludes a more thorough treatment, this paper (in Section III) analyzes and validates how power losses in a switching dc–dc converter (when optimally designed) change across technology nodes. For context, Sections II and IV introduce the basic operating principles and conduction modes of switched-inductor circuits and the implications of using low-voltage transistors in higher voltage applications. Section V ends by drawing conclusions.

II. Switched-inductor Converters

A. Operation

DC–DC converters use an inductor to transfer energy from an input source to a load. For that purpose, switches (S_I and S_{EN} in Fig. 1a) energize and (S_O and S_{DE} in Fig. 1b) de-energize an inductor L_X from an input V_{IN} to an output v_O in alternating cycles. Operationally, the circuit impresses a positive voltage across L_X (e.g., V_{IN}) to raise inductor current i_L and a negative voltage (e.g., $-v_O$) to lower i_L and steer energy to v_O. In buck converters, when v_O is always below V_{IN}, L_X can energize directly to v_O, which is why S_{EN} and S_O are normally absent in buck supplies. Similarly, when v_O is higher than V_{IN}, L_X can de-energize directly from V_{IN}, so S_I and S_{DE} are often absent in boost implementations. The general case presented in Fig. 1 corresponds to a non-inverting buck–boost topology.

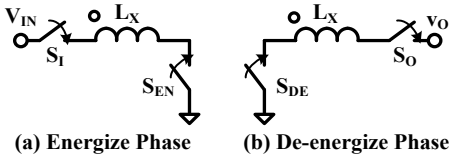

Fig. 1. Alternating (a) energize and (b) de-energize cycles.

B. Continuous- and Discontinuous-conduction Modes

In continuous-conduction mode (CCM), i_L never ceases to conduct current. In other words, as Fig. 2a illustrates, i_L rises and falls continuously as L_X continually energizes and de-energizes across switching period T_{SW}. When the output load current is low, however, L_X need not carry as much average current $i_{L(AVG)}$. Under these conditions, the converter can dissipate less power if L_X stops conducting. For that reason, many converters enter discontinuous-conduction mode (DCM) when the load falls below a threshold. As such, i_L rises from and falls back to zero within one T_{SW}, as Fig. 2b shows, and remains at zero until the onset of the next period.

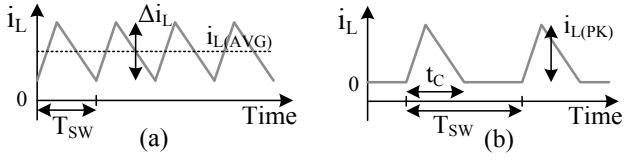

Fig. 2. Inductor-current waveforms in CCM and DCM.

C. Loss Mechanisms

Irrespective of the specific embodiment, all switched-inductor dc–dc converters incorporate the same loss mechanisms: conduction, capacitor-drive, and quiescent power [2], [8]. In a buck, for example, the switches that energize and de-energize the inductor (L_O in Fig. 3) from V_{IN} to v_O and v_O to ground (i.e., M_P and M_N) and other stray resistances in the power-conduction path (e.g., L_O's $R_{L.ESR}$ and C_O's $R_{C.ESR}$) consume energy when they conduct. Parasitic capacitances (e.g., M_P and M_N's $C_{G.P}$ and $C_{G.N}$) also require supply energy to charge and the feedback controller similarly demands current to operate. Because these losses are common to all converter implementations, how losses change across process nodes in a buck circuit is representative of the others, and vice versa.

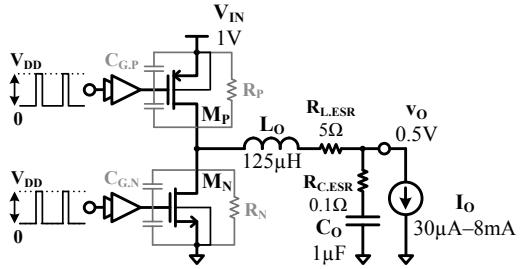

Fig. 3. Switching buck dc–dc converter.

III. Power Losses Across Process Technologies

A. Process Parameters

The driving motivation behind scaling semiconductor technologies is increasing the number of transistors that can fit in one silicon chip. Minimum channel length L_{MIN} is therefore an important measure of integration. Reducing L_{MIN}, however, requires other modifications in the process. Oxide thickness T_{OX}, for example, decreases [9], which means oxide capacitance per unit area C_{OX}" and transconductance parameter K' increase. Electric fields also intensify as a result of reductions in T_{OX}, so gate- and drain-source breakdown voltages $|V_{GS(MAX)}|$ and $|V_{DS(MAX)}|$ drop, and therefore, so does supply voltage V_{DD} [10]. The 0.18-, 0.35-, and 0.5-µm CMOS nodes in Table 1 show these trends.

Table 1. Process parameters across process nodes.

L_{MIN}	0.18 µm	0.35 µm	0.5 µm
	N/P-MOS	N/P-MOS	N/P-MOS
$\|V_{GS(MAX)}\|$ and $\|V_{DS(MAX)}\|$	1.8 V	3.3 V	4.5 V
$\|V_{TH}\|$	0.65/0.58 V	0.5/0.6 V	0.86/0.8 V
C_{OX}"	7.7 fF/µm^2	4.5 fF/µm^2	2.3 fF/µm^2
T_{OX}	45 Å	74 Å	151 Å
K'	135/35 µA/V^2	89/33 µA/V^2	47/12.5 µA/V^2

Process engineers typically offset reductions in gate drive, which result from lower $|V_{GS(MAX)}|$ values, with lower threshold voltages ($|V_{TH}|$). An implant step in the fabrication process adjusts V_{TH} for this purpose [11]. The objective is to keep gate-drive voltages (i.e., $V_{GS} - V_{TH}$) as high as possible. Unfortunately, reducing V_{TH} increases leakage currents and decreases noise margins in digital gates [12]. As a result, V_{TH} does not fall linearly with L_{MIN}.

B. Switch Power

Conduction: As already mentioned, resistors in the power-conduction path dissipate Ohmic power when they conduct L_O's i_L. The equivalent resistances of the power switches in a switching converter therefore consume conduction power P_C when engaged. As such, the power that their combined equivalent resistance R_{EQ} dissipates increases quadratically with i_L's root-mean-squared value $i_{L(RMS)}$:

$$P_C = R_{EQ}\, i_{L(RMS)}{}^2 \propto \frac{L_{MIN}}{W_{EQ}}. \qquad (1)$$

Since conducting switches only drop millivolts, MOSFETs operate in triode. As such, their resistances increase linearly with minimum channel length L_{MIN} and decrease linearly with maximum gate-drive $|V_{GS(MAX)}| - |V_{TH}|$:

$$R_{EQ} \approx \frac{L_{MIN}}{\mu_M C_{OX}"\, W_{EQ}\left(\left|V_{GS(MAX)}\right| - \left|V_{TH}\right|\right)} = \frac{L_{MIN}}{\mu_M C_{OX}"\, W_{EQ}\left(V_{DD} - \left|V_{TH}\right|\right)} \propto \frac{L_{MIN}}{W_{EQ}}, \qquad (2)$$

where μ_M is charge-carrier mobility and W_{EQ} the equivalent channel width of the MOSFET. In a buck converter, for example, M_P and M_N's equivalent resistances R_P and R_N (from Fig. 3) combine in R_{EQ} to conduct L_O's $i_{L(RMS).CCM}$ in CCM and $i_{L(RMS).DCM}$ in DCM [13], where

$$i_{L(RMS).CCM}{}^2 = i_{L(AVG)}{}^2 + \left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2, \qquad (3)$$

$$i_{L(RMS).DCM}{}^2 = \left(\frac{t_C}{T_{SW}}\right)\left(\frac{i_{L(PK)}}{\sqrt{3}}\right)^2, \qquad (4)$$

and Δi_L is i_L's peak-to-peak ripple, t_C over T_{SW} is L_O's conduction fraction across T_{SW}, and $i_{L(PK)}$ is i_L's peak in DCM (from Fig. 2). Therefore, because the fall in C_{OX}" offsets V_{DD}'s rise when L_{MIN} increases, R_{EQ} and P_C rise with L_{MIN}.

Drive: Although capacitors do not dissipate power, the switches that charge and discharge them do. In fact, V_{DD} loses all the charge it supplies to drive gates to V_{DD}, as set by $|V_{GS(MAX)}|$. In other words, when combining gate capacitors into an equivalent capacitance C_{EQ}, V_{DD} supplies $C_{EQ}V_{DD}$ across each switching period T_{SW} to lose drive power P_D:

$$P_D = \left(\frac{C_{EQ}V_{DD}}{T_{SW}}\right)V_{DD} = \left(C_{OX}"\, W_{EQ}L_{MIN}\right)V_{DD}{}^2 f_{SW} \propto W_{EQ}L_{MIN}{}^2. \qquad (5)$$

Because C_{OX}" drops with L_{MIN} and V_{DD} rises, C_{OX}" offsets L_{MIN} but not $V_{DD}{}^2$, so P_D increases quadratically with L_{MIN}.

C. Quiescent Power

The circuit blocks in the controller require current to operate, so they too dissipate power. When heavily loaded, a converter typically operates in CCM and switches at a moderately high f_{SW}. So, in CCM, most, if not all, circuit blocks function and consume power continuously across T_{SW}. Under light loads, however, the supply can save power by operating in DCM and switching at a lower f_{SW}. Still more, T_{SW} in microwatt applications can be long enough to allow system components to momentarily disengage, so as to save additional power.

Irrespective of the mode and f_{SW} of the converter and the duty cycle of its components, circuits in the feedback loop require sufficient quiescent current $I_{Q(BW)}$ to process information within one T_{SW}. Generally, the quiescent power $P_{Q(BW)}$ that bandwidth-critical circuits consume reduces to

$$P_{Q(BW)} = K_{DC} I_{Q(BW)} V_{DD} \propto L_{MIN}^{3}, \quad (6)$$

where K_{DC} is a correction fraction that accounts for duty-cycled elements in the feedback loop. Because the unity-gain frequency of the loop f_{0dB} is ultimately proportional to transistor transconductances g_m over parasitic capacitors C_{PAR}:

$$f_{0dB} \propto \frac{g_m}{C_{PAR}} \propto \frac{\sqrt{I_{Q(BW)}}}{C_{PAR}}, \quad (7)$$

$I_{Q(BW)}$ should be proportional to C_{PAR}^{2} (and as a result, to L_{MIN}^{2}), to maintain the same f_{0dB}. That means $P_{Q(BW)}$ increases with L_{MIN}^{3}.

Converters also include another class of circuits that need not process information within one T_{SW}, like the bias-current generator, protection circuitry, and monitoring blocks. These subsystems require sufficient bias current $I_{Q(B)}$ to remain operational in the presence of substrate and supply noise. For these circuits, their quiescent power $P_{Q(B)}$ is

$$P_{Q(B)} = K_{DC} I_{Q(B)} V_{DD} \propto L_{MIN}, \quad (8)$$

which roughly increases with V_{DD}, and therefore, with L_{MIN}.

D. Other Losses

Like the power switches, L_O's and C_O's parasitic resistances $R_{L.ESR}$ and $R_{C.ESR}$ also conduct part or all of $i_{L(RMS).CCM}$ and $i_{L(RMS).DCM}$. These resistances and currents, however, do not change with L_{MIN}. As a result, their corresponding conduction losses are independent of L_{MIN}.

Because power switches can conduct substantial current, converters normally introduce a dead time T_{DT} between the conduction times of adjacent power transistors. i_L cannot drop to zero instantaneously, however, so diodes in the circuit engage during T_{DT} to conduct i_L. As a result, these diodes dissipate dead-time power P_{DT} across T_{DT} of every T_{SW}:

$$P_{DT} = V_D i_{L(DT)} \left(\frac{T_{DT}}{T_{SW}} \right) = V_D i_{L(DT)} T_{DT} f_{SW}, \quad (9)$$

where V_D is the diode voltage and $i_{L(DT)}$ L_O's current during T_{DT}, which is practically a constant across T_{DT} because T_{DT} is a small fraction of T_{SW} – $i_{L(DT)}$ is roughly $2i_{L(AVG)}$ in CCM and $i_{L(PK)}$ in DCM [13]. Note none of these terms relate to L_{MIN}.

The switch that engages after T_{DT} conducts slightly more than i_L to lower the voltage across its terminals from V_{DD} + V_D to millivolts. During this transition, the transistor's current i_D and drain-source voltage v_{DS} overlap (T_{IV}) and therefore dissipate power P_{IV}:

$$P_{IV} = (V_{DD} + V_D) i_{IV} \left(\frac{T_{IV}}{T_{SW}} \right) = (V_{DD} + V_D) i_{IV} T_{IV} f_{SW} \propto L_{MIN}, \quad (10)$$

where i_{IV} is practically constant across T_{IV} because T_{IV} is a small fraction of T_{SW} and equal to $i_{L(AVG)}$ in CCM and $0.5i_{L(PK)}$ in DCM [13]. Since V_{DD} increases with L_{MIN}, P_{IV} also rises with L_{MIN}.

E. Minimizing Losses

Comparing efficiency across process nodes is only valid after optimizing the design for minimum losses. Off-chip losses, however, such as in L_O's $R_{L.ESR}$ and C_O's $R_{C.ESR}$, do not vary with process. Although diodes can be on chip, diode voltages change little with process. As such, dead-time losses P_{DT} are similarly independent to process. Because overlap time T_{IV} depends on how fast transistors drive parasitic capacitances, overlap power P_{IV} changes with W_{EQ} (design). Still, when compared to other switch losses, P_{IV} and P_{DT} are usually insignificant. So, only switch and quiescent losses remain.

Switch: Because both conduction and drive power P_C and P_D generally rise with channel length, L_{MIN} is the optimum channel length for all switches in the power stage. However, while P_C falls with channel width W_{EQ}, P_D increases. As such, combined losses are lowest when P_C equals P_D [13]–[14], which results at an optimum width W_{OPT}. Equating the sum of P_C and P_D's respective derivatives with respect to W_{EQ} to zero in CCM and DCM and solving for W_{EQ} reveals that

$$W_{OPT.CCM} = \frac{i_{L(RMS).CCM}}{V_{DD}\sqrt{\mu_M C_{OX}" ^2 f_{SW} (V_{DD} - |V_{TH}|)}} \propto \frac{1}{\sqrt{L_{MIN}}} \quad (11)$$

and $$W_{OPT.DCM} = \frac{i_{L(RMS).DCM}}{V_{DD}\sqrt{\mu_M C_{OX}" ^2 (V_{DD} - |V_{TH}|)}} \propto \frac{1}{\sqrt{L_{MIN}}}, \quad (12)$$

which the analytical results in Fig. 4 of the buck converter in Fig. 3 corroborate. Note that, since V_{DD} rises with L_{MIN} and C_{OX}" falls, W_{OPT} drops with the square root of L_{MIN}.

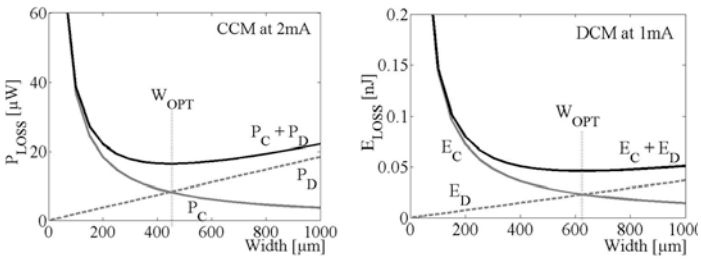

Fig. 4. Switch losses across channel widths.

Combined Losses: Because W_{OPT} drops with $L_{MIN}^{0.5}$, both P_C and P_D (from Eqs. 1 and 5) rise with $L_{MIN}^{1.5}$, so their sum also rises with $L_{MIN}^{1.5}$ in both CCM and DCM, as the analytical results in Fig. 5 of the buck converter in Fig. 3 show. Therefore, since bias and bandwidth-critical quiescent losses (from Eqs. 6 and 8) increase with L_{MIN} and L_{MIN}^{3}, all losses in an optimized design rise with coarser process nodes. In other words, finer pitched technologies yield higher efficiencies, as the simulated results in Fig. 6 of the converter in Fig. 3 with optimized 0.18-, 0.35-, and 0.5-µm CMOS switches show. The driving reason for this trend is V_{DD}'s quadratic and linear effects on drive and quiescent losses P_D and P_Q, respectively. Notice that derived theory follows simulations closely.

Simulation Notes: V_{IN} is 1 V to keep the terminal voltages of 0.18 µm transistors within their breakdown limits – stacking techniques would circumvent this limitation [6]–[7]. For maximum gate drive, V_{DD} is 1.5, 3, and 4 V for 0.18-, 0.35-, and 0.5-µm switches, respectively. With 125 µH and 1 µF for L_O and C_O, the converter transitions from DCM to CCM when

load current I_O is 2 mA. For ease of implementation, a comparator ensures $i_{L(PK)}$ is 4 mA and a clock changes f_{SW} to ensure the converter can sustain I_O. W_{EQ} is optimum at W_{OPT} (by design) for 0 – 2mA loads in DCM, and for 2mA load in CCM.

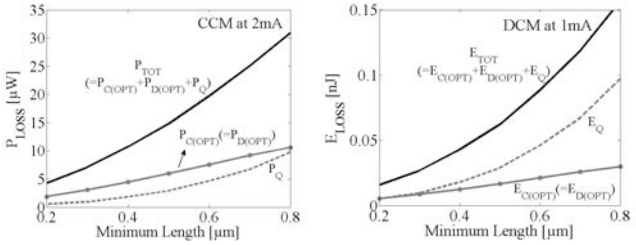

Fig. 5. Losses of optimized design across L_{MIN}.

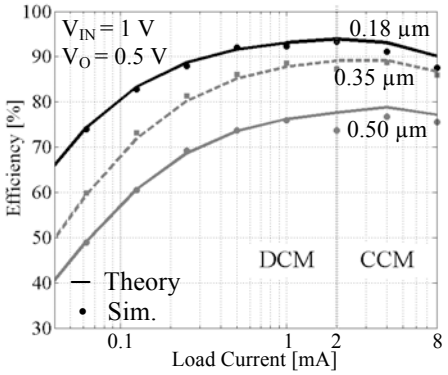

Fig. 6. Efficiency of optimized design across process nodes.

IV. Maximum Gate Drive vs Input Supply

Designers conventionally select the process so that its breakdown voltages match the application's input supply V_{IN}. With this approach, choosing the lowest L_{MIN} that can sustain V_{IN} yields the highest efficiency (e.g., 0.5-µm switches for a Li Ion's 2.7 – 4.2 V). Higher efficiency is possible, however, if L_{MIN} were lower (as Section III shows). For this, stacking transistors in series (with M_P and M_N in Fig. 3) can limit the voltage each switch receives to a fraction of V_{IN} [6]–[7].

Although series components add resistance, the quadratic fall in drive power P_D (from Eq. 5) that results from a lower gate-drive voltage V_{DD} more than offsets the linear rise in conduction power P_C (from Eq. 1). The challenge here is designing dedicated gate-drive circuits whose losses do not negate P_D's quadratic savings. Assuming this is not an issue, differentiating P_D and P_C with respect to V_{DD} and equating their sum to zero reveals that switch losses are lowest when V_{DD} is $2|V_{TH}|$, as the analytic results in Fig. 7 corroborate.

V. Conclusions

Theory and simulations presented for optimized 0.18-, 0.35-, and 0.5-µm CMOS switching buck dc–dc converters in CCM and DCM show that lower minimum channel lengths (L_{MIN}) yield higher efficiencies with peaks at 93%, 89%, and 79%, respectively. The fundamental reason for this trend is gate drive V_{DD} increases with L_{MIN}, which causes a quadratic rise in drive losses P_D and a linear rise in quiescent power P_Q that more than offset the resulting linear drop in conduction power P_C. Even when input supply V_{IN} exceeds maximum gate-drive $|V_{GS(MAX)}|$, limiting gate drive can save sufficient power to negate additional losses in the dedicated drive circuits to net a gain in efficiency. What is more, switch losses are lowest when $|V_{GS(MAX)}|$ is $2|V_{TH}|$. Therefore, irrespective of application, converter topology, and mode of operation, finer pitched technologies yield higher efficiency, as long as leakage current, which has a tendency to rise with reductions in L_{MIN}, do not become a considerable fraction of the load.

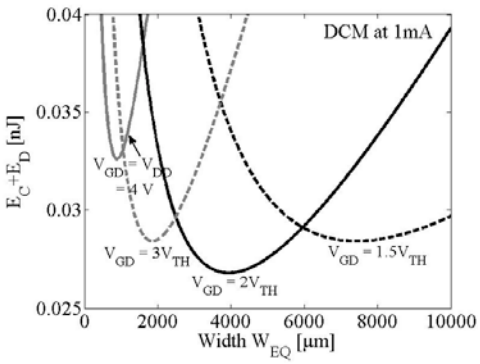

Fig. 7. Losses across width and gate-drive voltages in DCM.

References

[1] T. Simunic, *et al*, "Energy Efficient Design of Portable Wireless Devices," *Int. Symp. on Low Power Electronics and Design*, pp. 49–54, Aug. 2000.

[2] A. Stratakos, *et al*. "A low voltage cmos dc-dc converter for a portable battery-operated system," *IEEE IEEE Power Electronics Specialists Conference*, pp. 619–626, June 1994.

[3] G.A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators*, New York: McGraw-Hill, 2009.

[4] V. Kursun, *et al*, "Monolithic DC-DC Converter Analysis and MOSFET Gate Voltage Optimization," *IEEE/ACM Int. Symp. on Quality Electronic Design*, pp. 279-284, Mar. 2003.

[5] V. Kursun, *et al*, "Analysis of Buck Converters for On-Chip Integration with a Dual Supply Voltage Microprocessor," *IEEE Trans. on Very Large Scale Integration Systems*, vol. 11, no. 3, pp. 514-522, June 2003.

[6] S.K. Reynolds, "A DC-DC converter for short-channel CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 1, pp. 111-113, Jan. 1997.

[7] S. Bandyopadhyay, *et al*, "20µA to 100mA DC-DC converter with 2.8 to 4.2V battery supply for portable applications in 45nm cmos," *IEEE Int. Solid-State Circuits Conference*, pp. 386–387, 2011.

[8] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd Ed., New York: Springer Science & Business Media, LLC, 2001.

[9] Q. Huang, *et al*, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 1023-1036, Jul. 1998.

[10] V. Kursun, *et al*, "High input voltage step-down dc–dc converters for integration in a low-voltage CMOS process," *IEEE/ACM Int. Symp. on Quality Electronic Design*, pp. 517–521, Mar. 2004.

[11] M.R.M. Pherson, "The adjustment of MOS transistor threshold voltage by ion implantation," *Applied Physics Letters*, vol. 18, no. 11, pp. 502-504, June 1971.

[12] A.P. Chandrakasan, S. Sheng, and R.W. Brodersen, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473-484, Apr. 1992.

[13] S. Kim and G.A. Rincon-Mora, "Achieving High Efficiency under Micro-Watt Loads with Switching Buck DC-DC Converters," *Journal of Low Power Electronics*, vol. 5, no. 2, Aug. 2009.

[14] S. Musunuri and P.L. Chapman, "Optimization of CMOS transistors for low power DC-DC converters," *IEEE Power Electronics Specialists Conference*, pp. 2151-2157, 2005.