High-Damping Energy-Harvesting Electrostatic CMOS Charger

Karl Peterson and Gabriel A. Rincón-Mora
School of Electrical and Computer Engineering, Georgia Institute of Technology
Atlanta, Georgia U.S.A.
{petersok, Rincon-Mora}@gatech.edu

***Abstract*—Because small batteries store little energy, micro-scale systems often trade functionality or lifetime, or both, for integration. Harnessing ambient energy can abate the sacrifice, but only to the extent transducer and circuit efficiencies allow. Optimally adjusting the electrical damping force in the transducer is therefore as important as lowering power losses in the circuit. In kinetic electrostatic harvesters, raising the voltage across the moving parallel plates increases this force, which is what the energy-harvesting 0.35-µm CMOS charger proposed achieves with a 10-nF capacitor C_{CLAMP}. The system presented harnesses fifteen times (15×) more energy at 16 V (with 15 nJ/Cycle) than at 4 V (with 1 nJ/Cycle) from 50 – 250-pF, 60-Hz variations to generate (after discounting loses in the system) a net gain of 8.8 nJ/Cycle at 16 V.**

I. Powering Wireless Microsensors

Wireless microsensors add transforming intelligence to inaccessible, difficult-to-replace, and expensive-to-upgrade infrastructures like hospitals, factories, and the human body [1]. Their small batteries, however, can only power them for short periods, and recharging or replacing the batteries of thousands of networked nodes is, if not impossible, prohibitively expensive. Luckily, harvesting ambient energy can offset these drawbacks, even if power is low and sporadic.

Of possible sources, light supplies the most power *only* under direct sunlight. Radiation and heat seem ubiquitous, but radiated energy decreases drastically with distance and temperatures across miniaturized platforms are often impractically low [2]. Vibrations, on the other hand, are fairly abundant, and the kinetic energy that transducers harness from them can also be sufficient to power many microsystems [2]. Electromagnetic transducers, however, draw little energy and piezoelectric devices, although moderately powerful, do not scale as well as electrostatic transducers can with micro-electromechanical systems (MEMS) technologies [3].

Still, tiny transducers generate little power, so optimally damping them is as important as reducing energy losses across the system. This paper therefore proposes a CMOS charger that increases damping in an electrostatic transducer to harness kinetic energy in vibrations. To this end, Section II reviews how to harvest kinetic energy electrostatically and Sections III and IV present and discuss the system. Section V then evaluates the technology and Section VI draws conclusions.

II. Harvesting Kinetic Energy Electrostatically

An electrostatic transducer is basically a parallel-plate capacitor (C_{VAR}) with one plate fixed and the other suspended so that motion can change the distance between the plates [3]. An initial charge across C_{VAR} establishes the electrostatic damping force against which vibrations work to separate the plates. This way, as C_{VAR} decreases, if disconnected (i.e., charge constrained), C_{VAR}'s voltage v_{VAR} rises and v_{VAR}'s squared rise in C_{VAR}'s energy $0.5C_{VAR}v_{VAR}^2$ offsets C_{VAR}'s linear fall to produce a net gain in energy. Alternatively, when constrained to a voltage V_{PC}, C_{VAR}'s charge $C_{VAR}V_{PC}$ drops with C_{VAR}, which means C_{VAR} sources current (i.e., power). In other words, C_{VAR} converts kinetic energy from vibrations into the electrical domain when its plates separate.

Therefore, a harvester must invest energy E_{PC} to precharge C_{VAR} at C_{MAX}, as Fig. 1 shows. C_{VAR} then harnesses ambient energy E_{HARV} when C_{VAR} falls to C_{MIN}. After delivering and storing E_{HARV} elsewhere in the system, the circuit can recover what remains of E_{PC} in C_{VAR} as E_{REC}, before C_{VAR} uses E_{REC} to pull its plates together and rise to C_{MAX}.

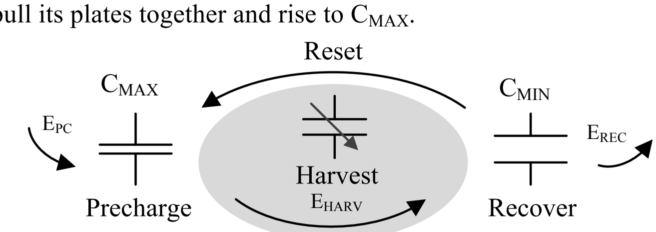

Fig. 1. Electrostatic harvesting process.

The damping force present in C_{VAR} when it falls to C_{MIN} determines how much energy C_{VAR} extracts from motion. As such, raising v_{VAR} –which establishes this force– as high as possible produces the most gain [4]. In other words, output energy per cycle E_O is highest when keeping v_{VAR} at the highest possible level throughout the *entire* harvesting period. When constraining C_{VAR} to V_{MAX} this way, E_{HARV} together with what remains in C_{VAR} at C_{MIN} (as E_{REC}) surpasses the investment needed to charge C_{VAR} to V_{MAX} (with E_{PC}) to produce a net gain in E_O:

$$E_{PC} = 0.5C_{MAX}V_{MAX}^2, \tag{1}$$

$$E_{HARV} = \left(C_{MAX} - C_{MIN}\right)V_{MAX}^2, \tag{2}$$

and

$$E_{REC} = 0.5C_{MIN}V_{MAX}^2, \tag{3}$$

so

$$E_O = E_{HARV} + E_{REC} - E_{PC} = 0.5V_{MAX}^2\left(C_{MAX} - C_{MIN}\right), \tag{4}$$

neglecting (for now) parasitic power losses in the circuit.

III. Proposed Voltage-constrained Harvester

A. Circuit Operation

While constraining C_{VAR} to a battery V_{BAT} (e.g., 2.7 – 4.2-V lithium-ion cell) is convenient and effective [5], it is not optimal because V_{BAT} is seldom near the maximum voltage that the transducer can sustain. At the cost of printed-circuit-board (PCB) real estate, a large off-chip capacitor C_{CLAMP} can, instead, clamp C_{VAR} at a higher voltage to produce more power. Permanently connecting C_{CLAMP} to C_{VAR} [3], however, forces the system to completely discharge and again precharge C_{CLAMP} together with C_{VAR}, the transfer losses of which are significant at an elevated voltage.

A diode D_{CLAMP} between C_{CLAMP} and C_{VAR} avoids having to discharge and precharge C_{CLAMP} every cycle by connecting C_{CLAMP} to C_{VAR} asynchronously only when v_{VAR} is close to v_{CLAMP}. In [6], for example, the system precharges C_{VAR} to V_{BAT} and kinetic energy in motion raises (in charge-constrained fashion) v_{VAR} until D_{CLAMP} and C_{CLAMP} clamp C_{VAR}. The drawbacks here are that D_{CLAMP} consumes power and C_{VAR} does not harvest at an elevated voltage for the *entire* harvesting period. Alternatively, the harvester proposed in Fig. 2 precharges C_{VAR} all the way to v_{CLAMP} and connects C_{VAR} to C_{CLAMP} with synchronous switch S_3 to ensure C_{VAR} harvests both close to v_{CLAMP} and through the entire harvesting period. (Note the system precharges C_{CLAMP} only once, during startup, to a voltage that is slightly below the IC's breakdown level.)

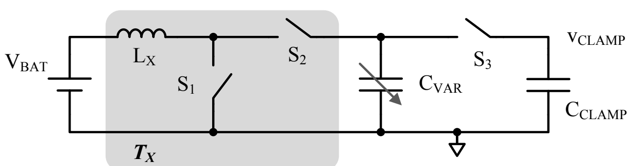

Fig. 2. Precharging C_{VAR} from V_{BAT} before clamping C_{VAR} with C_{CLAMP}.

More specifically, transfer block T_X energizes inductor L_X from V_{BAT} with S_1 and subsequently de-energizes L_X into C_{VAR} with S_2 to precharge C_{VAR} at C_{MAX} to v_{CLAMP}. Once done, S_3 connects C_{VAR} to C_{CLAMP} and C_{VAR} falls to C_{MIN} to harvest energy at v_{CLAMP}. Because C_{CLAMP} is substantially larger than C_{VAR}, v_{CLAMP} is nearly constant through the harvesting period. When C_{VAR} reaches C_{MIN}, S_2 and S_3 energize L_X from C_{CLAMP} and C_{VAR} until C_{CLAMP} discharges to its precharged state, at which point S_3 opens to allow S_2 to discharge C_{VAR} further. S_2 then opens and S_1 closes to drain L_X into V_{BAT}. After this, vibrations (and what little energy remains in C_{VAR}) push C_{VAR}'s plates closer together to raise C_{VAR} to C_{MAX}, where the cycle repeats. Notice that, while C_{VAR} cycles once across several milliseconds, energy transfers require only microseconds, so transfers are practically instantaneous.

B. Energy-transfer Sequence

Since transferring less energy incurs less conduction losses, reducing the energy that L_X transfers is important. In the case of Fig. 2, while V_{BAT} invests E_{PC}, recovers E_{REC}, and receives E_{HARV}, C_{CLAMP} both receives and sources E_{HARV}, as Fig. 3a shows. Alternatively, investing E_{PC} from what C_{CLAMP} gains in E_{HARV}, like Fig. 3b shows, reduces the energy that L_X transfers from C_{CLAMP} to V_{BAT} to E_{NET}, while keeping all other transfers at equivalent levels.

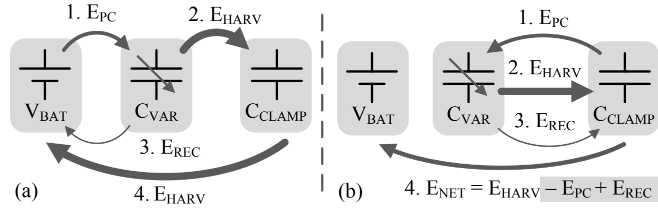

Fig. 3. (a) Battery- and (b) C_{CLAMP}-derived precharge investment strategies.

C. Circuit Implementation

Fig. 4 illustrates the switching network that realizes the modified sequence in Fig. 3b. Here, with S_{VAR} closed, S_{HS} energizes L_X from C_{CLAMP} and S_{LS} de-energizes L_X into C_{VAR} to precharge C_{VAR} to v_{CLAMP}, as Fig. 5 shows. Then, with S_{VAR}, S_H, and S_L opened, S_{HARV} closes to steer C_{VAR}'s E_{HARV} into C_{CLAMP} until C_{VAR} falls to C_{MIN}. At C_{MIN}, S_{VAR} closes to drain C_{VAR}'s E_{REC} into C_{CLAMP} by energizing L_X with S_{LS} and de-energizing L_X with S_{HS}. The sequence continues by disengaging all switches so that vibrations can raise C_{VAR} back to C_{MAX} through the reset phase. Finally, just before the next precharge phase, S_{BAT} closes and S_{LS} and S_{HS} switch to transfer the net energy gained E_{NET} in C_{CLAMP} to V_{BAT}.

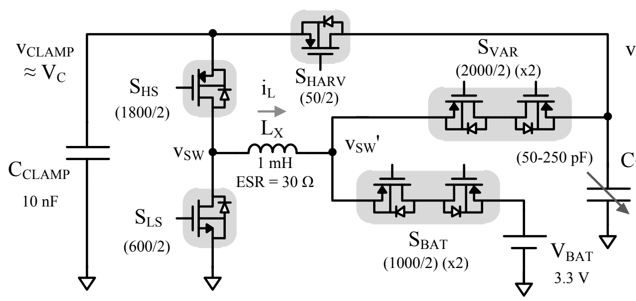

Fig. 4. Proposed harvester (with MOSFET dimensions in μm).

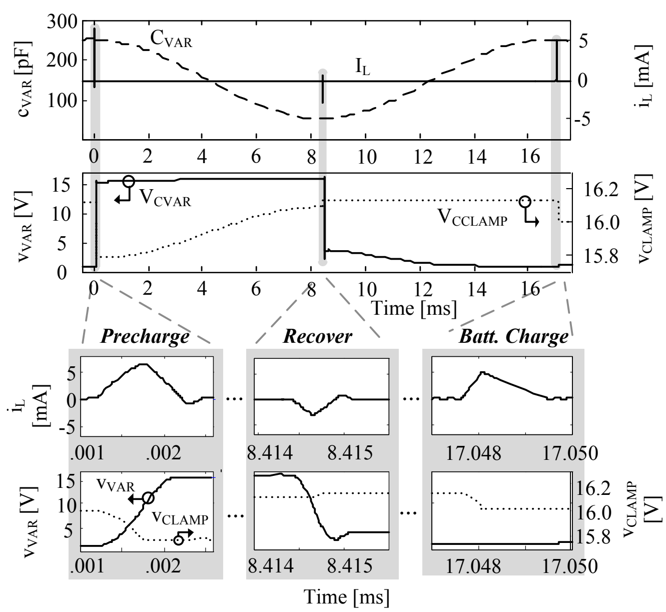

Fig. 5. Operational waveforms of the proposed energy-harvesting charger.

D. Integration

Although building a reliable MEMS C_{VAR} is still the subject of research, 50 – 250 pF seems feasible at 1 cm^2 [3]–[4], [7]–[9]. Therefore, to keep v_{CLAMP} nearly unchanged through the harvesting period, C_{CLAMP} is high at 10 nF. L_X is also high at 1 mH because higher inductances lower current-conduction losses in the system. Unfortunately, the silicon-area costs and series-resistance losses that 10 nF and 1 mH require and introduce are unacceptably high, so C_{CLAMP} and L_X are both off-chip. Still, at maybe $2 \times 2 \times 1.5$ mm^3, co-packaging them with or attaching them to an integrated circuit (IC) is possible.

Since the system relies on a high v_{VAR} to generate more power and the 0.35-μm CMOS technology considered includes 18-V devices, v_{CLAMP} is roughly 16 V and the switches in Fig. 4 are all 18-V transistors. Back-to-back FETs implement S_{BAT} and S_{VAR} to ensure their body diodes are off across all values of v_{SW}', across 0 – 16 V. Finally, because p- and n-type MOSFETs have more gate-drive when connected to high and low voltages, respectively, S_{HS} and S_{HARV}, which connect to v_{CLAMP}, are p-type devices and S_{LS}, which connects to ground, is an n-type transistor.

IV. Power Losses and Output Power

A. Conduction Losses

A fundamental loss in switching converters is the power that inductor current i_L dissipates across series resistances in its path. In Fig. 4, L_X's i_L loses energy to parasitic switch and series resistances R_{EQ} in its path. Because L_X transfers packets of energy by energizing and de-energizing across voltages that barely change, i_L is triangular, as Fig. 5 corroborates. As such, i_L's RMS current $I_{L(RMS)}$ depends on i_L's peak $I_{L(PEAK)}$:

$$I_{L(RMS)} = \frac{I_{L(PEAK)}}{\sqrt{3}}, \tag{5}$$

which means R_{EQ} dissipates $R_{EQ}I_{L(RMS)}{}^2$ across conduction time T_L to consume conduction energy E_C:

$$E_C = R_{EQ} I_{L(RMS)}{}^2 T_L \,. \tag{6}$$

Because V_{BAT} (e.g., 3.3 V) and v_{CLAMP} (e.g., 16 V) surpass R_{EQ}'s combined voltage by at least an order of magnitude, R_{EQ}'s effects in $I_{L(PEAK)}$ and T_L are not as significant. In other words, C_{VAR}, C_{CLAMP}, L_X, V_{BAT}, and how much energy L_X transfers roughly set $I_{L(PEAK)}$ and T_L. Table I summarizes theoretical $I_{L(PEAK)}$ and T_L values that the system requires to (*i*) precharge C_{VAR} with $0.5C_{MAX}v_{CLAMP}{}^2$, (*ii*) recover $0.5C_{MIN}v_{CLAMP}{}^2$, and (*iii*) charge V_{BAT} with net gain E_{NET}', which is $0.5(C_{MAX} - C_{MIN})v_{CLAMP}{}^2$ minus other conduction losses. Since recovery yields transcendental equations, Table I shows only numerical solutions for the recovery phase.

B. Drive Losses

Another basic loss in dc–dc converters is the energy (E_D) drawn to charge stray capacitances (C_{PAR}) in the circuit, especially when driving them across wide voltages:

$$E_D = 0.5C_{PAR}\left(V_{C(FIN)}{}^2 - V_{C(INI)}{}^2\right), \tag{7}$$

where $V_{C(FIN)}$ and $V_{C(INI)}$ refer to C_{PAR}'s final and initial voltages, respectively. The gates of the power devices and, from Fig. 4, parasitic capacitances at v_{SW} and v_{SW}' cause these losses. Because traversing across v_{CLAMP} (e.g., 0 – 16 V) dissipates substantial power, reducing gate drive to lower voltages is important.

TABLE I. CONDUCTION LOSSES

	$I_{L(PEAK)}$	T_L	Predicted Losses	Simulated Losses
Precharge	$\frac{v_{CLAMP}}{2}\sqrt{\frac{3C_{MAX}}{L_X}}$	$\frac{2\pi}{3}\sqrt{L_X C_{MAX}}$	1.8 nJ	2.3 nJ
Recover	–	–	0.12 nJ	0.16 nJ
Battery Charge	$\sqrt{\frac{2E_{NET}'}{L_X V_{BAT}}\left(\frac{V_{BAT}v_{CLAMP}}{V_{BAT}+v_{CLAMP}}\right)}$	$\frac{2E_{NET}'}{V_{BAT}I_{L(PEAK)}}$	2.2 nJ	2.4 nJ

C. Quiescent Losses

The controller that decides when to engage each switch also dissipates quiescent energy E_Q. Here, seven comparators achieved the gate signals desired to switch the network. Each comparator requires quiescent current I_Q (i.e., power P_{CMP}) from supply V_{DD} only while engaged, through on time T_{ON}:

$$E_Q = \sum\left(P_{CMP}T_{ON}\right) = \sum\left(I_Q V_{DD} T_{ON}\right). \tag{8}$$

To account for these losses in the simulations, macro-models emulating the losses that low-power comparators reported in [5], [10]–[12] suffered implemented the comparators used to drive the 0.35-μm 18-V MOSFETs in Fig. 4.

D. Simulations

Because v_{CLAMP} is so high, drivers should lower gate drive to V_{BAT} levels (e.g., 3.3 V) with, for example, floating switched capacitors. Reducing S_{BAT}'s gate swing, however, is not possible because S_{BAT}'s gates must fall well below V_{BAT} to engage and charge V_{BAT} (with E_{NET}') and rise well above V_{BAT} to v_{CLAMP} after that to keep S_{BAT} off during C_{VAR}'s precharge phase, when v_{SW}' reaches v_{CLAMP}. S_{BAT}, as a result, loses more drive power in the battery-charge phase than S_{VAR} in precharge, even when S_{BAT} is smaller than S_{VAR}.

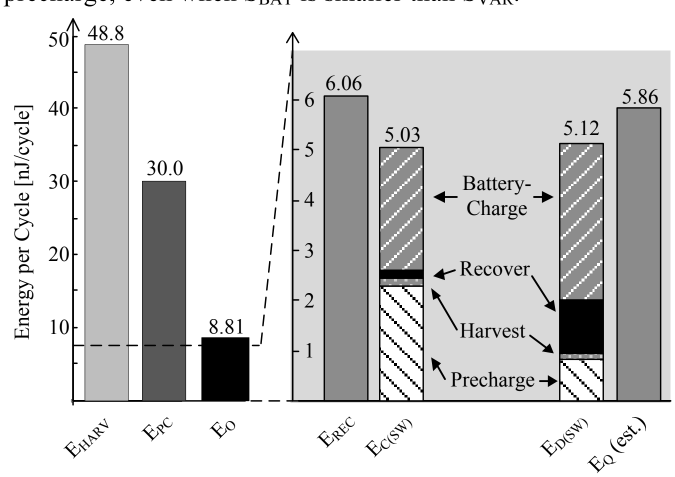

Fig. 6. Simulated energy transfers and losses across one C_{VAR} cycle.

Ultimately, minimizing the power lost in the switches amounts to balancing their conduction and gate-drive losses

$E_{C(SW)}$ and $E_{D(SW)}$, which, as Fig. 6 demonstrates, the 18-V transistors in Fig. 4 achieve. When subjected to 50 – 250-pF variations at 60 Hz and clamped to 16 V, simulated conduction losses in the battery-charge phase exceed theory by roughly 10% because resistances in the circuit, which theoretical values in Table I neglect, reduce L_X's voltage and, as a result, extend T_L. Simulated recovery and precharge losses are about 25% higher because i_L is more often near its peak than the approximated triangle predicts, which means $I_{L(RMS)}$ is higher than theorized. In the end, after subtracting conduction, drive, and quiescent losses E_C, E_D, and E_Q, the system generates 8.8 nJ/Cycle, which is equivalent to 530 nW.

One of the key features of the proposed system is its ability to harvest kinetic energy at elevated C_{VAR} voltages. Consider that, before discounting control losses, while clamping C_{VAR} near 16 V harvests close to 15 nJ/Cycle, keeping v_{VAR} at 4 V generates only 1.0 nJ/Cycle, as Fig. 7 illustrates. In fact, recovery losses at 4 V surpass C_{VAR}'s energy at C_{MIN} (E_{REC}), which is why [5] skips altogether the recovery phase. In other words, after including control losses and a recovery phase, the conditions that produce a gain at 16 V suffer a loss at 4 V.

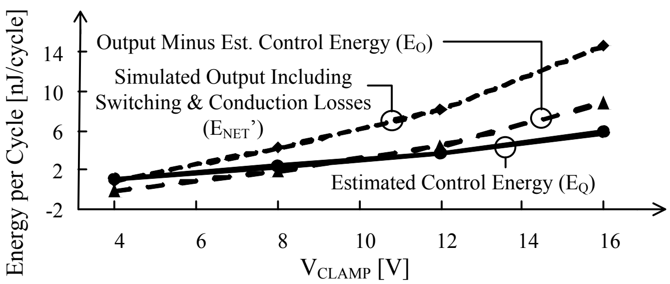

Fig. 7. Output energy per cycle E_O across clamping voltage V_{CLAMP}.

V. Role of Electrical Damping

An initial charge on C_{VAR}, as mentioned earlier, presents an electrical damping force across C_{VAR} that opposes the ambient mechanical forces that separate C_{VAR}'s plates. In other words, electrical damping reduces the extent to which ambient kinetic energy moves C_{VAR}'s plates, thereby reducing C_{VAR}'s range [9]. In the case of small MEMS transducers, however, which exhibit low coupling factors (k_C) and therefore convert only a small fraction of ambient energy into the electrical domain, electrical damping has minimal effects on C_{MAX} and C_{MIN}. Still, arbitrarily increasing the electrical damping force in C_{VAR} will, at some point, affect C_{MAX} and C_{MIN}, and in the extreme case, keep C_{VAR}'s suspended plate motionless.

The simulation results in Fig. 7 illustrate how the system proposed performs when mechanical forces overwhelm damping forces to such an extent that increasing v_{CLAMP} has a negligible impact on C_{VAR}'s range. This is a reasonable assumption for miniaturized systems because C_{VAR}'s mechanical properties and semiconductor breakdown voltages in the integrated circuit (IC) limit k_C and V_{CLAMP}, respectively. Better (and perhaps larger) transducers and circuit technologies with higher breakdown voltages, however, can negate this assumption and alter C_{MAX} and C_{MIN}. When electrical damping becomes this significant, maximum output power results when the interface circuit establishes a damping force whose equivalent mechanical impedance matches that of the transducer's [13]. With the system proposed, tracking the maximum power point is possible by adjusting v_{CLAMP}.

VI. Conclusions

With 0.35-µm 18-V CMOS transistors, a 10-nF clamping capacitor C_{CLAMP}, and a 50 – 250-pF electrostatic transducer C_{VAR} oscillating at 60 Hz, the proposed harvester draws from C_{VAR} fifteen times (15×) more energy per cycle at 16 V (with 16 nJ/Cycle) than at 4 V (with 1 nJ/Cycle), generating (after discounting other losses in the system) a net gain of 8.8 nJ/Cycle at 16 V and a net loss of 4.8 nJ/Cycle at 4 V. To achieve this performance, the system (*i*) reduces conduction losses by minimizing the energy transferred per operation, (*ii*) reduces overall losses by balancing conduction and gate-drive losses in the switches, and (*iii*) raises C_{VAR}'s harvesting voltage well above the battery's. The drawback of using a large capacitor rather than a battery to set C_{VAR}'s voltage is off-chip area (e.g., $2 \times 2 \times 1.5$ mm^3). Generating higher output power, however, can easily outweigh the cost of one additional off-chip component when considering the functional (i.e., power) and lifetime (i.e., energy) requirements of emerging microsystems.

References

[1] D. Puccinelli and M. Haenggi, “Wireless sensor networks: applications and challenges of ubiquitous sensing,” *IEEE Circuits and Syst. Magazine,* vol. 5, no. 3, pp. 19–31, Sept, 2005.

[2] S. Roundy *et al.*, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications,* vol. 26, no. 11, pp. 1131–1144, July 2003.

[3] S. Meninger*, et al.*, "Vibration-to-electric energy conversion," *IEEE Trans. Very Large Scale Integr. (VLSI) Sys.,* vol. 9, no. 1, pp. 64–76, Feb. 2001.

[4] P. Basset *et al*., "A batch-fabricated and electret-free silicon electrostatic vibration energy harvester," *J. Micromechanics and Microengineering,* vol. 19, no. 11 , p. 115025, Nov. 2009.

[5] E.O. Torres and G.A. Rincon-Mora, "A 0.7µm BiCMOS Electrostatic Energy-Harvesting System IC," *IEEE J. Solid-State Circuits,* vol. 45, no. 2, pp. 483–496, Feb. 2010.

[6] B.C. Yen and J.H. Lang, "A variable-capacitance vibration-to-electric energy harvester," *IEEE Trans. Circuits and Systems I, Reg. Papers,* vol. 53, no. 2, pp. 288–295, Feb. 2006.

[7] Y. Chiu and V.F.G. Tseng, "A capacitive vibration-to-electricity energy converter with integrated mechanical switches," *J. Micromechanics and Microengineering,* vol. 18, no. 10, p. 104004, Oct. 2008.

[8] G. Despesse*, et al.*, "Design and Fabrication of a New System For Vibration Energy Harvesting," *IEEE 2005 PhD Research in Microelectron. and Electon.*, vol. 1, pp. 225–228.

[9] S. Roundy*, et al.*, *Energy Scavenging for Wireless Sensor Networks*, Springer, 2003.

[10] Y.K. Ramadass and A.P. Chandrakasan, "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," *IEEE. J. Solid-State Circuits,* vol. 45, no. 1, pp. 189–204, Jan. 2010.

[11] T.T. Le*, et al.*, "Piezoelectric micro-power generation interface circuits," *IEEE J. Solid-State Circuits,* vol. 41, no. 6, pp. 1411–1420, June 2006.

[12] H. Lhermet*, et al.*, "Efficient Power Management Circuit: From Thermal Energy Harvesting to Above-IC Microbattery Energy Storage," *IEEE J. Solid-State Circuits,* vol. 43, no. 1, pp. 246–255, Jan. 2008.

[13] D. Galayko and P. Basset, "A General Analytical Tool for the Design of Vibration Energy Harvesters (VEHs) Based on the Mechanical Impedance Concept," *IEEE Trans. Circuits and Systems I, Reg. Papers,* vol. 58, no. 2 pp. 299–311, Feb. 2011.