A Rectifier-Free Piezoelectric Energy Harvester Circuit

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***Abstract*—Although the benefits of incorporating non-invasive intelligence to state-of-the-art (e.g. wireless micro-sensors) and difficult-to-replace technologies are undeniable, micro-scale integration constrains energy and power to the point lifetime and functionality fall below practical expectations, forcing technologists to seek energy and power from the surrounding environment. To this end, a piezoelectric energy harvester circuit is proposed. The 2µm CMOS design circumvents the need for (and losses and low-voltage restrictions associated with) a rectifier by extracting and transferring energy directly from the piezoelectric transducer to the battery via a switched inductor. Simulation results show that the proposed system can harvest 45nJ and 10nJ per period at 71% and 69% efficiency from 3V and 1.5V peak piezoelectric voltages, respectively.**

I. Harvesting Piezoelectric Energy

Wireless micro-sensors, biomedical implants, and other miniaturized devices suffer from limited lifetime performance because the energy and power available in micro-scale sources such as thin-film Li Ions and micro-fuel cells [1] are insufficient. Harvesting energy from the surrounding environment in the form of heat, vibration, and/or light is therefore one of the most promising means of overcoming this shortage. Of these, vibration energy from piezoelectric materials is appealing because they, like solar energy, produce moderate power densities, which is not the case for energy derived from heat, internal lighting, and vibration via electromagnetic and electrostatic means [1-3].

Generally, a harvester system extracts and transfers energy from a source to a power cache such as a large capacitor or Li Ion so that a load may later draw whatever power it needs on demand. A piezoelectric material, for example, when affixed to a stationary base (Fig. 1), generates ac charge (and energy E_{IN}) in response to oscillating mechanical displacements (i.e., energy E_{ME} in vibrations) [4]. The harvester circuit conditions and steers this charge into a battery, trickle-charging it to power and extend the life of electronic devices such as wireless micro-sensors [5].

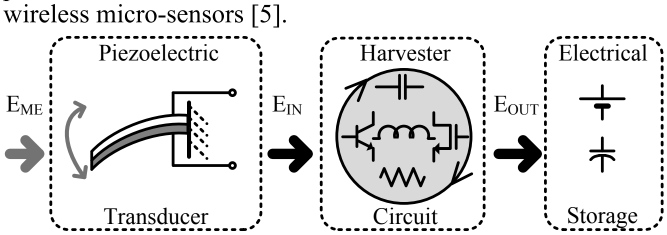

Fig. 1. Piezoelectric harvester system.

The aim of the harvester is to generate a net energy gain E_{OUT} from a small-footprint solution so E_{IN}, energy losses, and printed-circuit-board (PCB) real estate must be as high, low, and small, respectively, as possible. In light of these, Sections II-III review the state of the art in harvesting microelectronics and discuss how the proposed piezoelectric harvester circuit optimally induces more E_{IN} from the piezoelectric device; employs a tuned, rectifier-free power-efficient switching converter; and uses only one inductor as the low-loss energy-transfer medium. Section IV then presents and discusses the circuit designed to achieve these objectives along with its simulation results, drawing conclusions in Section V.

II. Harvesting Circuits

A. Rectifier

Harvesting electrical energy from an ac source like the piezoelectric transducer into a dc energy-storage device like the Li Ion requires ac-dc conversion, for which diode and diode-configured transistor rectifiers are popular. Although diode and diode-connected transistors (Fig. 2(a)) [6] are simple and robust, they require 0.7-1V to conduct current. The main problem with this approach is micro-scale piezoelectric harvesters produce low voltages (v_{IN}) when constrained to micro-scale dimensions so the resulting rectifier (Fig. 2(d)) can only process a fraction of E_{IN}. Additionally, the forward voltage drops (v_D) across each diode and diode-connected devices incur considerable conduction power losses.

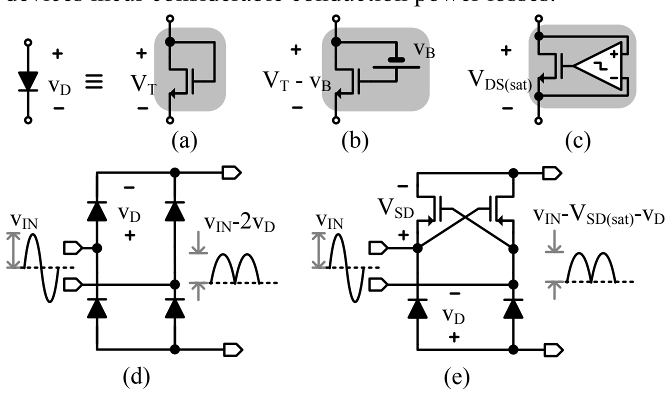

Fig. 2. (a) Diode-connected, (b) V_T-cancelled, and (c) feedback-enhanced transistors used in full-wave (d) diode-based and (e) cross-coupled rectifiers.

One way of reducing v_D is to superimpose a bias voltage v_B onto the gate of the MOSFET that effectively cancels the drop associated with threshold voltage V_T (Fig. 2(b)) [7]. Doing so, however, requires processing energy and induces higher off-state leakage current, given the device is on the verge of conduction in its off state. Sensing and feeding an amplified version of the voltage across the transistor back to the gate (Fig. 2(c)) also reduces v_D [8], except the comparator used requires energy. Nevertheless, if the comparator consumes less energy than the conduction energy otherwise lost through a more conventional diode, a full-wave rectifier (Fig. 2(d)) reaps some benefits from replacing its diodes with feedback-enhanced transistors. Still, satisfying the comparator's input common-mode range, bandwidth, and drive requirements with little energy is challenging.

On the other hand, given the ac characteristic of the input voltage, cross-coupling v_{IN}'s complementary inputs can drive

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and enhance the gates of the rectifying transistors (Fig. 2(e)) [6, 9]. Diodes in the positive and negative conduction paths remain because they must block reverse current, for which feedback-enhanced transistors (Fig. 2(c)) may be used. The technique ultimately reduces the number of comparators needed and the losses they incur. Still, the efficiency benefits associated with higher output voltage swings do not relax the circuit's input voltage requirements, as v_{IN} must exceed V_T to engage the MOSFETs.

B. Power Conditioner

A rectifier alone cannot charge a battery or generally supply a load because its output voltage is neither flexible nor regulated. As in [10] (Fig. 3(a)), conditioning the rectified output amounts to inserting a dc-dc converter and regulating its charging current by modulating the duty cycle of the switching network. The conditioner and its control circuitry, however, require energy to operate, not to mention considerable excess (i.e., unharvested) energy generated from vibrations remains in the piezoelectric material's equivalent capacitance [13], as the circuit is not able to fully extract it.

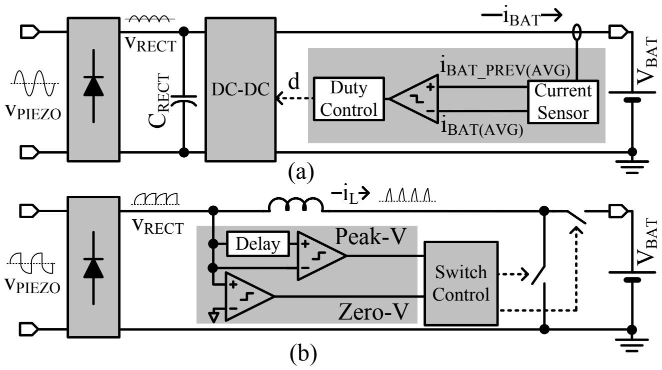

Fig. 3. (a) Feedback and (b) feed-forward power conditioners.

A way to fully deplete the piezoelectric material of its energy (and harvest more energy [12]) is to sense its state and drive whatever current is possible to the battery, as in [11] (Fig. 3(b)). The idea is to monitor the rectified voltage, whose level is an indicator of how much energy is available, and control a switching converter to transfer all energy present in the source capacitor (i.e., piezoelectric material) into an inductor so that it may later drive energy into a battery or load. Though the system is now optimized, the rectifier consumes energy and superimposes input-voltage constraints on the piezoelectric device, which limit energy and integration.

III. Proposed Harvester

A. System Operation

The objectives of the proposed harvester are to (1) reduce the input voltage requirements of the rectifier, (2) extract as much energy as possible from the piezoelectric material, and (3) reduce the energy lost in the system. One way to reduce the voltage constraints and energy overhead associated with the rectifier is to eliminate the block altogether and connect a smarter conditioner directly to the piezoelectric material, as proposed in Fig. 4. The conditioner is a magnetic based switching converter because neither a capacitor-based nor the linear counterpart can fully deplete the source. What is more, to conform to micro-scale dimensions, the circuit employs only one off-chip inductor.

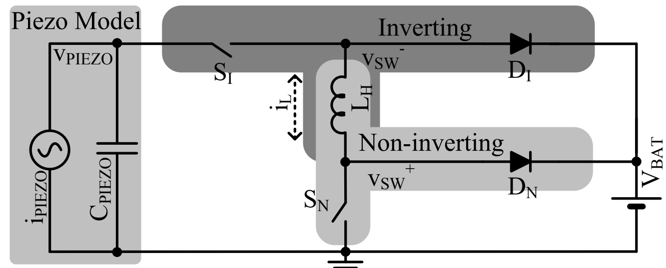

Fig. 4. Proposed rectifier-free piezoelectric harvester.

The converter offers two energy-flow paths to the output (i.e., battery voltage V_{BAT}): one for positive piezoelectric voltages (v_{PIEZO}^+) and another for the negative counterparts (v_{PIEZO}^-). In Fig. 4, non-inverting boost converter $L_HS_ND_N$ processes v_{PIEZO}^+, transferring piezoelectric energy to V_{BAT}. Similarly, inverting boost converter $L_HS_ID_I$ processes v_{PIEZO}^-, likewise driving energy to V_{BAT}. A boost converter is used in both cases because $|v_{PIEZO}|$ is below its average Li Ion target of 3.6V, allowing the harvester to process the low piezoelectric voltages a rectifier would otherwise be unable to handle.

Each converter operates in alternating cycles, transferring energy from piezoelectric capacitor C_{PIEZO} to V_{BAT} by energizing and de-energizing the harvesting inductor L_H in alternating phases. Each cycle (positive and negative) extracts and transfers all the generated charge in C_{PIEZO}. The converter controls the cycles and their respective phases by synchronizing them to v_{PIEZO}'s positive and negative peaks. To reduce conduction losses, feedback-enhanced switching transistors (Fig. 2(c)) implement D_N and D_I.

B. Energy Flow and Timing Diagram

The energy-flow paths highlighted on the schematic of Fig. 5 and the ensuing timing diagram that results (Fig. 6) illustrate the cycle-by-cycle and phase-by-phase operation of the proposed harvester. First, at the onset of a positive cycle, S_I is off and vibrations charge C_{PIEZO} (i.e., v_{PIEZO} increases) with transduced energy E_C^+ for a duration of τ_C^+. When v_{PIEZO} reaches its positive peak, S_I and S_N engage, drawing energy E_L^+ from C_{PIEZO} to energize L_H for duration τ_L^+, during which time v_{PIEZO} decreases and inductor current i_L increases. When i_L reaches its peak, S_N disengages, allowing freewheeling D_N to steer output energy E_B^+ into V_{BAT} for time τ_B^+. Note that in de-energizing L_H via S_I, L_H also energizes C_{PIEZO}, but with negative charge (i.e., v_{PIEZO} decreases below ground), which means C_{PIEZO} diverts part of E_L^+ away from V_{BAT}. The purpose of this investment in C_{PIEZO} is to induce more electrical damping on the piezoelectric material so that more energy can be harvested in the negative cycle [12, 14].

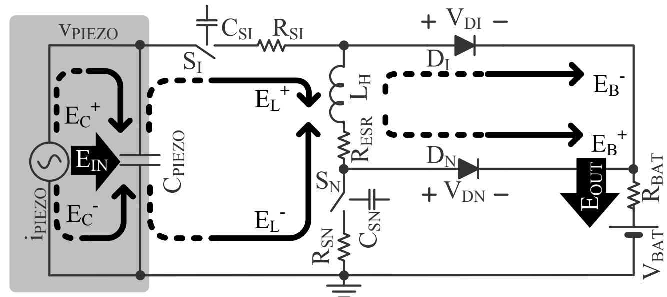

Fig. 5. Energy-flow paths and parasitic devices present in the harvester.

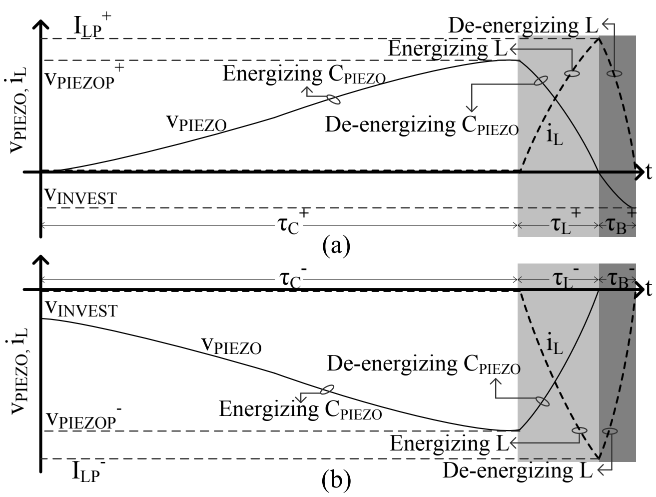

Fig. 6. (a) Positive- and (b) negative-cycle timing diagrams.

When i_L reaches zero, D_N shuts off, disconnecting C_{PIEZO} from all low-impedance points and consequently allowing vibrations to energize C_{PIEZO} with negative charge so that v_{PIEZO} decreases further below ground. When v_{PIEZO} reaches its negative peak, S_I and S_N again engage, energizing L_H with energy stored in C_{PIEZO}. When C_{PIEZO} is completely discharged, S_I shuts off, allowing freewheeling D_I to channel energy to V_{BAT}. D_I disengages when i_L reaches zero, at which point the system is ready for another positive cycle.

The system must only sense and synchronize the circuit to v_{PIEZO}'s positive and negative peaks. Additionally, because L_HC_{PIEZO} tank requires one fourth its resonant period to energize L_H with C_{PIEZO}'s energy (in τ_L^+ and τ_L^-), the corresponding switches need only derive its control from a delay block, not a current sensor. Simplifying the control of these switches in this way decreases the total energy lost.

C. Energy Losses and Efficiency

Energy losses through the system fall in one of three categories: conduction, switching, and quiescent. Parasitic resistances and diode drops through the conduction path, for example, dissipate Ohmic power when i_L is non-zero: during positive and negative inductor energizing and de-energizing phases τ_L^+, τ_B^+, τ_L^-, and τ_B^-. Since i_L ramps linearly during L_H's de-energizing phases, given the voltage across L_H is constant at V_{BAT}, i_L's RMS values during positive and negative cycles are $I_{LP}^+/\sqrt{3}$ and $I_{LP}^-/\sqrt{3}$, respectively, where I_{LP} refers to peak currents. As a result, parasitic resistors dissipate RMS losses and D_N and D_I, because they drop constant voltages V_{DN} and V_{DI}, dissipate power with average currents $0.5I_{LP}^+$ and $0.5I_{LP}^-$, the sum of which yields de-energizing positive- and negative-cycle conduction losses E_{CD}^+ and E_{CD}^-:

$$E_{CD}^+ \approx \left(R_{SI} + R_{ESR} + R_{BAT}\right)\left(\frac{I_{LP}^+}{\sqrt{3}}\right)^2 \tau_B^+ + V_{DI}\left(\frac{I_{LP}^+}{2}\right)\tau_B^+ \quad (1)$$

and

$$E_{CD}^- \approx \left(R_{SN} + R_{ESR} + R_{BAT}\right)\left(\frac{I_{LP}^-}{\sqrt{3}}\right)^2 \tau_B^- + V_{DN}\left(\frac{I_{LP}^-}{2}\right)\tau_B^-. \quad (2)$$

L_H's de-energizing phases τ_B^+ and τ_B^- depend on I_{LP}^+ and I_{LP}^-, which in turn depend on L_HC_{PIEZO}'s resonance period during the previous cycle and peak voltages v_{PIEZOP}^+ and v_{PIEZOP}^-:

$$\tau_B^+ \approx L_H\left(\frac{I_{LP}^+}{V_{BAT}}\right) = \sqrt{L_H C_{PIEZO}}\left(\frac{v_{PIEZOP}^+}{V_{BAT}}\right) = \frac{2}{\pi}\left(\frac{v_{PIEZOP}^+}{V_{BAT}}\right)\tau_L^+ \quad (3)$$

and

$$\tau_B^- \approx L_H\left(\frac{I_{LP}^-}{V_{BAT}}\right) = \sqrt{L_H C_{PIEZO}}\left(\frac{v_{PIEZOP}^-}{V_{BAT}}\right) = \frac{2}{\pi}\left(\frac{v_{PIEZOP}^-}{V_{BAT}}\right)\tau_L^-. \quad (4)$$

Although i_L is sinusoidal through L_H's energizing phases, given L_HC_{PIEZO}'s resonance, a linear approximation produces sufficiently accurate results so i_L's RMS values remain unchanged and the resistors dissipate similar positive and negative energizing conduction losses E_{CE}^+ and E_{CE}^-:

$$E_{CE}^+ \approx \left(R_{SI} + R_{ESR} + R_{SN}\right)\left(\frac{I_{LP}^+}{\sqrt{3}}\right)^2 \tau_L^+ \quad (5)$$

and

$$E_{CE}^- \approx \left(R_{SI} + R_{ESR} + R_{SN}\right)\left(\frac{I_{LP}^-}{\sqrt{3}}\right)^2 \tau_L^-, \quad (6)$$

where L_H's energizing phases τ_L^+ and τ_L^-, as stated earlier, are one fourth L_HC_{PIEZO}'s resonance.

Parasitic capacitances in the switches also require energy to charge and discharge. In the proposed harvester, transistors engage and disengage only once per vibration period so total switching gate-drive loss E_{SGD} is the linear sum of the constituent one-time CV^2 losses. Because S_I, D_I, and D_N's gate capacitances C_{SI}, C_{DI}, and C_{DN} transition supply voltage V_{BAT} and S_N's gate capacitance C_{SN} transitions $2V_{BAT}$, E_{SGD} reduces to

$$E_{SGD} = C_{SI}V_{DD}^2 + C_{SN}\left(2V_{BAT}\right)^2 + C_{DI}V_{BAT}^2 + C_{DN}V_{BAT}^2, \quad (7)$$

where gate capacitances depend on transistor dimensions.

Ultimately, system efficiency is the ratio of harvested energy E_{OUT} to input piezoelectric energy E_{IN}, the former of which is E_{IN} minus all the aforementioned losses, including the quiescent energy (E_Q) required to control the circuit:

$$\eta = \frac{E_{OUT}}{E_{IN}} = \frac{E_{IN} - E_C - E_{SIV} - E_{SGD} - E_Q}{E_{IN}}, \quad (8)$$

where E_C includes all conduction losses E_{CD}^+, E_{CD}^-, E_{CE}^+, and E_{CE}^-. E_{IN} is the mechanically transduced energy in piezoelectric capacitance C_{PIEZO}, which can be described in terms of v_{PIEZOP}^+ and v_{PIEZOP}^-:

$$E_{IN} = \frac{1}{2}C_{PIEZO}\left(v_{PIEZOP}^+\right)^2 + \frac{1}{2}C_{PIEZO}\left(v_{PIEZOP}^-\right)^2, \quad (9)$$

where the absolute value of v_{PIEZOP}^- equals the sum of the absolute value of v_{PIEZOP}^+ and the absolute value of v_{INVEST}, the latter of which can be derived by dividing the diverted charge during τ_B^+ by C_{PIEZO}:

$$v_{PIEZOP}^- \approx -v_{PIEZOP}^+ - \frac{I_{LP}^+\tau_B^+}{2C_{PIEZO}} = -v_{PIEZOP}^+\left(1 + \frac{v_{PIEZOP}^+}{2V_{BAT}}\right). \quad (10)$$

IV. Circuit and Simulation Results

Fig. 7 illustrates the CMOS circuit embodiment of the system proposed in Figs. 4-5. The 100µH inductor with 3.4Ω series resistance emulates a $3\text{x}3\text{x}1.5\text{mm}^3$ off-chip inductor. Back-to-back transistors implement S_I and S_N because their otherwise unblocked body diodes would conduct current away from their intended destinations (i.e., lose energy). To reduce E_Q, D_I and D_N's sensing comparators remain off (i.e., lossless) until current reaches their respective negative input terminals, during which time the rising voltage enables the comparators, keeping them engaged only through τ_B^+ and τ_B^-.

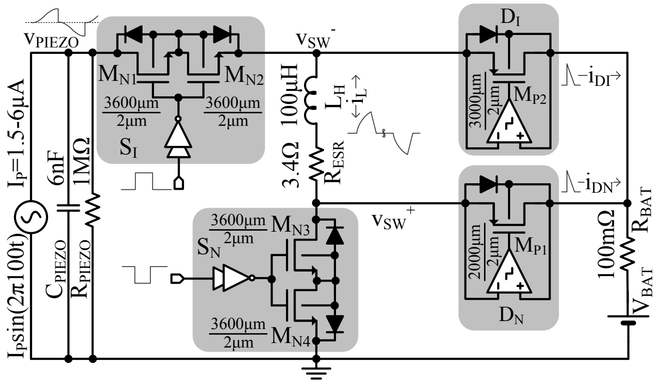

Fig. 7. Circuit embodiment of the proposed harvester system.

Fig. 8 illustrates simulation results showing the harvested energy (E_{OUT}) over multiple 10ms vibration periods (T_{VIB}). E_{OUT} increases twice with every period in stepwise fashion because charge is momentarily driven into V_{BAT} only during L_H's two de-energizing phases (τ_B^+ and τ_B^-). As a result, E_{OUT} increases at rates of 45, 10, 4, and 1.5 nJ per period under piezoelectric peak voltages of 3, 1.5, 1, and 0.75 V, respectively. It is important to note that the quiescent energy loss of the peak detection block is not included in these simulation results. In fact, results show that the peak detection block should consume no more than 1.5nJ per period to produce a net energy gain from slow (e.g., 100Hz), low-amplitude (e.g., v_{PIEZOP}^+ is 0.75V) low-energy vibrations.

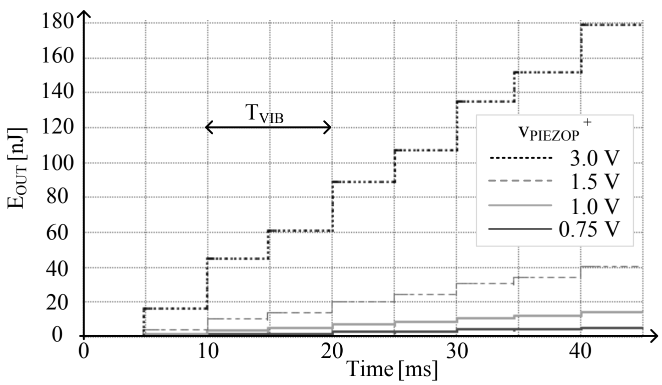

Fig. 8. Simulation results showing energy harvested.

TABLE I. THEORETICAL AND SIMULATED ENERGY LOSSES PER PERIOD.

Energy [nJ]	v_{PIEZOP}^+=0.75V		v_{PIEZOP}^+=1.5V		v_{PIEZOP}^+=3V	
	The.	Sim.	The.	Sim.	The.	Sim.
E_{IN}	3.72	3.86	16.3	16.0	72.7	67.2
S_I & S_N's E_C	0.70	0.68	2.42	2.41	10.25	11.5
R_{ESR} & R_{BAT}'s E_C	0.10	0.17	0.5	0.72	2.89	3.29
D_I & D_N's E_C	0.05	0.20	0.49	0.60	4.43	3.21
S_I & S_N's E_{SGD}	1.20	0.83	1.34	0.77	1.64	0.66
D_I& D_N's E_{SGD}	0.16	0.23	0.16	0.20	0.16	0.19
D_I & D_N's cp's E_Q	0.20	0.19	0.4	0.3	0.5	0.57
E_{OUT}	1.31	1.56	11.0	11.0	52.8	47.8
η [%]	35.2	40.4	67.4	68.8	72.6	71.1

Table I tabulates the theoretical (as derived from the previous section) and simulated losses and resulting efficiencies through the system. Efficiency increases with E_{IN} (and E_{OUT}) from 35% to 71% because conduction losses scale with E_{IN} (and E_{OUT}) and switching gate-drive losses do not. In other words, efficiency performance increases with rising E_{IN} (and E_{OUT}) values and peak piezoelectric voltages v_{PIEZOP}.

V. CONCLUSIONS

The proposed piezoelectric CMOS harvester circuit produced 45, 10, 4, and 1.5 nJ from peak piezoelectric voltages 3, 1.5, 1 and 0.75V at efficiencies of 71, 69, 58, and 41% The key features of the design are simplicity and scalability, as it bypasses the input-voltage requirements and saves the energy and silicon real estate associated with an ac-dc rectifier, in addition to only using one off-chip inductor. The system also invests (and recovers) some of its energy to increase the electrical damping during negative piezoelectric voltages, ultimately increasing the overall energy extracted during that phase and scavenging all the energy available in the piezoelectric material. The significance of harvesting all available energy with low piezoelectric voltages is micro-scale integration because the market space wireless micro-sensors enjoy in biomedical, commercial, industrial, military, and space applications may be as vast as the cellular phone's, if not larger.

REFERENCES

[1] S. Roundy *et al*, "A study of low level vibrations as a power source for wireless sensor nodes," *Computer Communications*, v. 26, n. 11, pp. 1131-44, Jul. 2003.

[2] H. Sodano *et al*, "A review of power harvesting from vibration using piezoelectric materials," *Shock and Vibration Digest*, v. 36, n. 3, pp. 197-205, May 2004.

[3] N. duToit *et al*, "Design considerations for MEMS-scale piezoelectric mechanical vibration energy harvesters," *Integrated Ferroelectrics*, v. 71, pp. 121-60, 2005.

[4] S. Sentruria, *Microsystem Design*. Boston: Kluwer Academic Publishers, 2001.

[5] E. Torres, and G. Rincón-Mora, "SiP integration of intelligent, adaptive, self-sustaining power management solutions for portable applications," *IEEE Int'l Symp. on Ckts. & Sys*., pp. 5311-4, 2006.

[6] Y. Lam *et al*, "Integrated low-loss CMOS active rectifier for wirelessly powered devices," *IEEE Trans. Ckts. & Sys. II, Express Briefs*, v. 53, n. 12, pp. 1378-82, Dec. 2006.

[7] T. Umeda *et al*., "A 950MHz rectifier circuit for sensor networks with 10m-distance," *IEEE Int'l. Solid-State Circuits Conf*., pp. 256-7, 597, Feb. 2005.

[8] T. Le *et al*., "Piezoelectric micro-power generation interface circuits," *IEEE J. Solid-State Circuits*, v. 41, n. 6, pp. 1411-20, Jun. 2006.

[9] M. Ghovanloo and K. Najafi, "Fully integrated wideband high-current rectifiers for inductively powered devices," *IEEE J. Solid-State Circuits*, v. 39, n. 11, pp. 1976-84, Nov. 2004.

[10] G. Ottman *et al*, "Adaptive piezoelectric energy harvesting circuit for wireless remote power supply," *IEEE Trans. Power Electron.*, v. 17, n. 5, pp. 669-76, Sept. 2002.

[11] S. Xu *et al.*, "Low frequency pulsed resonant converter for energy harvesting," *IEEE Trans. of Power Electron*., v. 22, n. 1, pp. 63-8, Jan. 2007.

[12] A. Badel *et al* "Piezoelectric energy harvesting using a synchronized switch technique," *J. Intelligent Material Systems and Structures*, v. 17, n. 8-9, pp. 831-9, Aug.-Sept. 2006.

[13] M. Goldfarb and L. Jones, "On the efficiency of electric power generation with piezoelectric ceramic," *ASME J. of Dynamic Systems, Measurement, and Control*, v. 121, pp. 566-71, Sept. 1999.

[14] G. Lesieutre *et al*, "Damping as a result of piezoelectric energy harvesting," *J. Sound and Vibration*, v. 269, n. 3-5, pp. 991-1001, Jan. 2004.