Designing an Accurate and Robust LC-Compliant Asynchronous ΣΔ Boost DC–DC Converter

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***Abstract*—Portable electronic devices not only require switching DC-DC converters to be compact and integrated but also compliant to wide off-chip LC filter variations, which are subject to manufacturing tolerances, temporal and thermal parameter drifts, and more often than not, application-driven constraints. While optimal LC compliance has been demonstrated in ΣΔ buck converters, little has been done in boosting applications. This paper presents an asynchronous ΣΔ boost converter and describes how LC variations affect stability, steady-state error, and switching frequency, and how a frequency-dependent gain mitigates these effects. Simulations show the circuit is stable for 1-30µH inductances and 15-350µF output capacitances, its steady-state error is less than 1%, and its switching frequency varies 15% less (over load and line variations) than in conventional ΣΔ converters.**

I. Introduction

The exploding mobile and battery-operated market continues to demand more integration, higher power efficiency, and lower cost, and the switching supplies that drive them demand no less. This is especially challenging when considering DC-DC controller integrated circuits (ICs) are exposed to off-chip LC filter components that vary considerably across process, temperature, time, and loading profiles, which are application driven [1]. Switching supplies with on-chip frequency compensation are therefore confined to specific applications or subject to degraded stability, transient, and regulation performance.

Asynchronous ΣΔ buck converters [2-3] do not suffer from LC compliance issues because they, in controlling output voltage v_{OUT}, also regulate inductor current i_L. In most portable applications, the output ripple voltage of a buck converter is mostly the voltage across the equivalent series resistor (ESR) of the output capacitor, which is a mere reflection of the inductor ripple current ($V_{ESR} = I_{L\text{-}Ripple}R_{ESR}$). Regulating V_{ESR} amounts to regulating i_L, as in current-mode control, and therefore making the inductor appear like a current source in the voltage feedback loop and turning the LC complex-conjugate pole pair into a single RC pole, the result of which is inherent stability, irrespective of LC. Any changes in LC are consequently compensated with corresponding changes in switching frequency.

The inductor ripple current in boost converters, on the other hand, does not fully flow to the output capacitor and cannot, as a result, be sensed by monitoring the output ripple voltage, which is why ΣΔ control in boost converters must sense i_L separately [4]. Even then, however, boost converters have one further complication when compared against their bucking counterparts and that is the presence of a right-hand plane (RHP) zero. Although ΣΔ control in boost switching supplies is reported to improve transient response to large load and line variations, the RHP zero still constrains its operating LC filter range [5-7]. A more detailed analysis of the effects of LC variations on ΣΔ boost converters and its design implications is therefore warranted.

This paper presents an asynchronous ΣΔ boost converter and discusses, analyzes, and validates via simulations its stability, steady-state error, and switching frequency performance. To start the discussion, ΣΔ boost converters are reviewed and the foregoing design presented in Section II. Section III describes the effects of LC variations on circuit performance and their design implications. Section IV then describes and validates the ΣΔ boost converter design. At the end, in Section V, relevant conclusions are drawn.

II. ΣΔ Boost DC-DC Switching Converters

A. Power Stage

The power stage of a boost converter is comprised of an inductor-switch L-MN combination (Fig. 1(a)) that draws and stores input energy, and a *catch* diode-output capacitor D-C combination (clamping peak sample and hold detector) whose purpose is to ultimately transfer the energy stored in L to the output. Since the steady-state voltage across L is zero, the average voltage across MN is V_{IN}; and because v_{PH} is zero when MN is on, the peak voltage across MN is higher than V_{IN} when MN is off. This peak voltage is captured by the peak-detecting D-C circuit, superimposing an output voltage v_{OUT} across C that is greater than V_{IN}. Since the inductor current i_L flows through D out to v_{OUT} only when switch MN is off, (Fig. 1(b)), v_{OUT} is a poor indicator of the inductor ripple current, and to realize ΣΔ control, i_L must be sensed separately.

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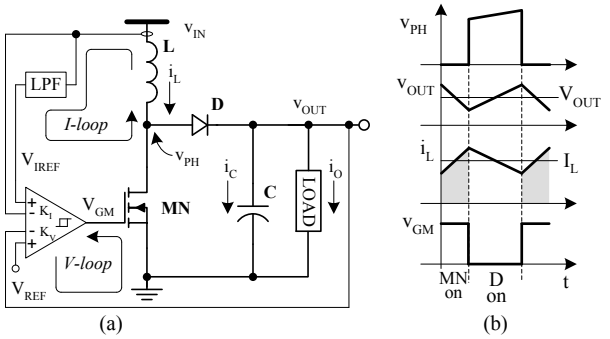

Fig. 1. ΣΔ boost converter (a) schematic and (b) corresponding waveforms.

B. ΣΔ Control

ΣΔ control in boost converters combines the scaled values of i_L and v_{OUT} ripples into a single summing (sliding) parameter S (Figs. 1(a)-2) that is then regulated to zero by a ΣΔ control loop. The ripples are extracted by subtracting the sensed voltage and current signals from their reference values. While independent DC reference V_{REF} is used for v_{OUT}, i_L, which varies with load, is referenced to the current necessary to sustain the load, which is i_L's average value: a low pass filtered version of i_L.

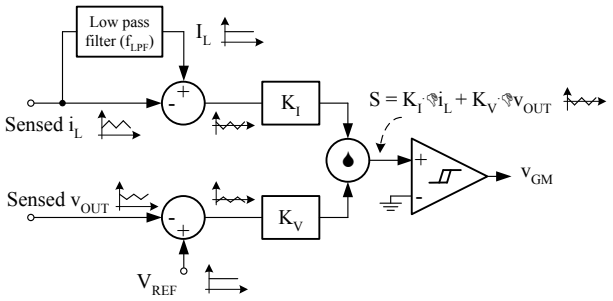

Fig. 2. Block-model representation of a boost ΣΔ controller.

The overriding objective of the converter, by definition, is to regulate v_{OUT}'s steady-state value to a predetermined DC value (V_{REF}). To do this, the DC gain of the voltage path in ΣΔ control variable S,

$$S = K_I(I_L - i_L) + K_V(V_{REF} - v_{OUT}), \quad (1)$$

must be considerably higher than that of the current path such that, when S is regulated to zero in steady state, the DC effects of i_L on the ΣΔ loop are negligible and DC V_{OUT} must consequently equal V_{REF} to satisfy the control equation.

III. Effects of LC Variations on Performance

A. ΣΔ Stability Requirements

ΣΔ control in boost converters consists of two control loops in parallel (one is the feed-forward path of the other): i_L and v_{OUT} control loops (I- and V loops) in Figs. 1(a)-2. Their respective loop gains are

$$G_I = -\left[1 - \left(\frac{1}{1 + s/p_{LPF}}\right)\right] K_I M \left(\frac{i_l}{d}\right)$$

and

$$= -\left(\frac{s/p_{LPF}}{1 + s/p_{LPF}}\right) K_I M \left(\frac{2I_L}{D'}\right)\left(\frac{\text{zero}_{LHP}}{\text{double LC pole}}\right), \quad (2)$$

$$G_V = -K_V M\left(\frac{v_{out}}{d}\right) = -K_V M\left(\frac{V_{OUT}}{D'}\right)\left(\frac{\text{zero}_{RHP}}{\text{double LC pole}}\right) \quad (3)$$

where M is the gain of the summing comparator (modulator), $\hat{d}$ and D are the small-signal and DC duty cycles of switch MN, D' is 1-D, and the two zeros are [8]

$$\text{zero}_{RHP} = \left(\frac{D'^2}{L}\right)\left(\frac{V_{OUT}}{I_O}\right) \quad (4)$$

and

$$\text{zero}_{LHP} = \frac{2I_O}{CV_{OUT}}. \quad (5)$$

The DC gain of voltage-loop gain G_V is designed to be higher than current DC loop gain G_I (Fig. 3) to ultimately regulate the steady-state output voltage to V_{REF}. However, at higher frequencies, to mask the effects of the RHP zero, G_I has higher gain and bandwidth, the end result of which is that the effects of G_V on summing variable S at high frequencies are overwhelmed by G_I (i.e., G_I's unity-gain frequency UGF_I is higher than G_V's unity-gain frequency UGF_V). In other words, stability (at the unity-gain frequency of S) is determined by G_I (not G_V), whose design constraint (using Eqs. (2)-(5) and superimposing the condition that UGF_I be greater than UGF_V) translates to:

$$\frac{K_I}{K_V} > \left(\frac{I_O}{V_{OUT}}\right)\left(\frac{L}{D'C}\right). \quad (6)$$

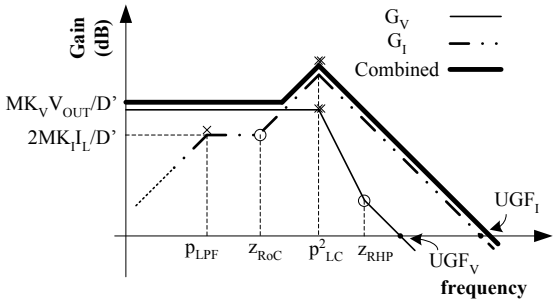

Fig. 3. Composite, current, and voltage ΣΔ Bode plot response.

Eq. (6) presupposes the corner frequency (p_{LPF}) of the averaged inductor current (reference for i_L), which constitutes an out-of-phase feed-forward path, has negligible effects on stability at frequencies of interest. That is, p_{LPF} must be low enough to filter out-of-phase i_l and allow overall negative feedback characteristics to prevail at higher frequencies. In practice, p_{LPF} should fall below zero_{LHP} (z_{RoC} in Fig. 3). In a variable LC environment, both Eq. (6) and the aforementioned p_{LPF} condition must be satisfied under worst-case LC extremes, the result of which is low system bandwidth and consequently slow transient response.

B. Steady-State Error

To regulate DC output voltage V_{OUT}, the ΣΔ loop controls combined parameter S, whose steady-state value is unaffected by the current loop, with a hysteretic comparator (Fig. 2). Including the switching effects of delays t_{d_ON} and t_{d_OFF} in the turn-on and turn-off of switch MN extends the ripple in S (assumed linear) beyond the boundaries set by the hysteresis window (H) (Fig. 4). The average of the resulting triangular signal sets the steady-state accuracy of the circuit.

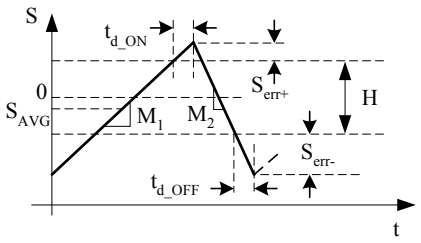

Fig. 4. Effect of switching delays on regulated variable S.

As observed in Fig. 4, steady-state accuracy is worst (average value of S, viz. S_{AVG}, is not zero) when the rising-to-falling slopes ratio is high:

$$S_{AVG} = \frac{H/2 + S_{err+} + \left(-H/2 - S_{err-}\right)}{2} = \frac{1}{2}\left(M_1 t_{d\_ON} - M_2 t_{d\_OFF}\right), \quad (7)$$

where M_1 and M_2 are the rising and falling slopes of S. Assuming K_I at the switching frequency (K_{I_fsw}) is designed to be considerably greater than K_V (K_{V_fsw}) and delays t_{d_ON} and t_{d_OFF} are equal to t_d, Eq. (7) simplifies to

$$S_{AVG} = \frac{t_d}{2} K_{I\_fsw}\left(\left|\frac{di}{dt}\right|_{OFF} - \left|\frac{di}{dt}\right|_{ON}\right) = \frac{K_{I\_fsw} t_d \left(V_{OUT} - 2V_{IN}\right)}{2L}, \quad (8)$$

and equating to the low frequency form of S from Eq. (1), which is

$$S_{AVG} \approx K_{V\_DC}\left(V_{REF} - V_{OUT}\right), \quad (9)$$

where K_{V_DC} is the DC version of K_V, which is assumed to be greater than K_{I_DC} at low frequencies as dictated by design, indicates DC error voltage V_{err} increases with increasing K_{I_fsw} and t_d and decreases with K_{V_DC} and L:

$$V_{err} = V_{OUT} - V_{REF} = \left(\frac{K_{I\_fsw}}{K_{V\_DC}}\right)\left(\frac{t_d}{2L}\right)\left(2V_{IN} - V_{OUT}\right). \quad (10)$$

Arbitrarily decreasing K_I and increasing K_V to reduce V_{err} compromises the stability condition stated in Eq. (6), which is why, to satisfy Eqs. (6) and (10), K_V must be high at DC and low at high frequencies (and K_I the opposite).

C. Switching Frequency

Switching frequency f_{SW} is a function of the times it takes S to traverse hysteresis window H up and down. Since the rising and falling rates of i_L are set by the application (V_{IN}, V_{OUT}, and 1/L), f_{SW} is inversely proportional to H, L, and parasitic MN delay times t_{d_ON} and t_{d_OFF}. From inspection (Fig. 4), the off and on times (t_{OFF} and t_{ON}) of switch MN are governed by the rising and falling rates of S, hysteresis window H, and delay times t_{d_ON} and t_{d_OFF}:

$$t_{OFF} = \frac{H}{|M_1|} + \frac{S_{err-}}{|M_1|} + t_{d\_ON} \quad (11)$$

and

$$t_{ON} = \frac{H}{|M_2|} + \frac{S_{err+}}{|M_2|} + t_{d\_OFF}. \quad (12)$$

Assuming as before that t_{d_ON} and t_{d_OFF} equal t_d and K_I is considerably greater than K_V at f_{SW}, f_{SW} simplifies to

$$f_{SW} = \frac{1}{t_{OFF} + t_{ON}} = \frac{V_{IN}\left(V_{OUT} - V_{IN}\right)}{V_{OUT}^2\left(t_d + \frac{HL}{K_{I\_fsw}}\right)} \propto K_{I\_fsw}. \quad (13)$$

Switching frequency f_{SW} decreases for any increase in input voltage V_{IN} beyond $V_{OUT}/2$, and since t_d is normally small, with increasing inductance values. A change in the switching frequency can be partially offset by varying K_I inversely with frequency, the net result of which is negative feedback with respect to frequency (K_I attempts to increase f_{SW} when f_{SW} decreases as a result of any other parameter change).

IV. Design and Simulation Results

To validate the foregoing ΣΔ boost DC-DC converter circuit (Fig. 1(a)) within the context of a practical system, a 1A lithium-ion supplied portable 5V application is assumed. The main feature of the foregoing design is LC compliance and the targeted range is therefore 1-30μH and 15-350μF. Key design parameters for regulation and stability performance are voltage and current loop gains K_V and K_I and low pass filter LPF, the latter of which attenuates out-of-phase i_L with a pole below 1kHz. As discussed earlier, the objective is for K_V to be higher than K_I at low frequencies to reduce steady-state errors and K_I higher than K_V at high frequencies, near f_{SW}, to set flexible stability conditions. To achieve this (Fig. (5)), low frequency pole p_{KV} (7.5kHz) is added to K_V, which has a DC gain of 40V/V, and higher pole-zero pair p_{KI}-z_{KI} (160kHz and 800kHz) added to K_I, which has 10V/V of DC gain. Parasitic pole p_{par} in K_I limits the bandwidth of K_I at relatively high frequencies (10MHz), past f_{SW}. Table I presents a summary of these parameters.

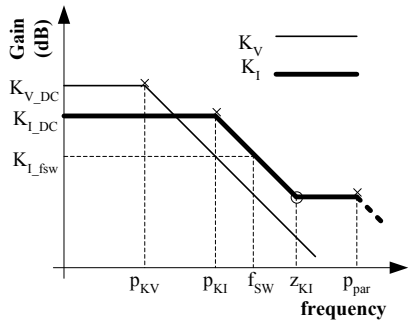

Fig. 5. Frequency-dependent voltage and current loop gains K_V and K_I.

Table I. Design parameters.

Parameter	Value	Parameter	Value
V_{IN} (V)	2.7 – 4.2	V_{OUT} (V)	5 ± 5%
C (μF)	15 – 350	L (μH)	1 – 30
K_{V_DC} (V/V)	40	p_{KV} (kHz)	7.5
K_{I_DC} (V/V)	10	K_{I_HF} (V/V)	2.5
p_{KI} (kHz)	160	z_{KI} (kHz)	800
p_{par} (MHz)	10	I_{OUT} (A)	0.1 – 1

Fig. 6 illustrates the volume space for which the converter was verified to be stable by subjecting the circuit to 0.1-1A load steps. Steady-state output voltage error increases with increasing V_{IN} and decreases with increasing L, as predicted in Eq. 10 and shown in Fig. 8, but remains below 1% of V_{OUT} (error is consistently positive because V_{OUT} is always less than $2V_{IN}$).

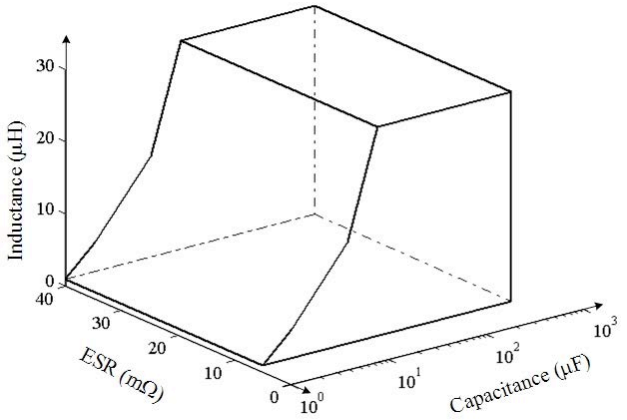

Fig. 6. 3-D volume of stability for the proposed ΣΔ converter.

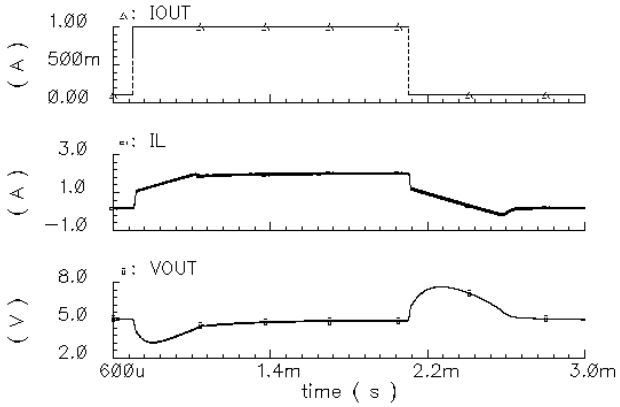

Fig. 7. 0.1-1A load-step response at L = 30 µH, C = 15 µF, V_{IN} = 2.7 V.

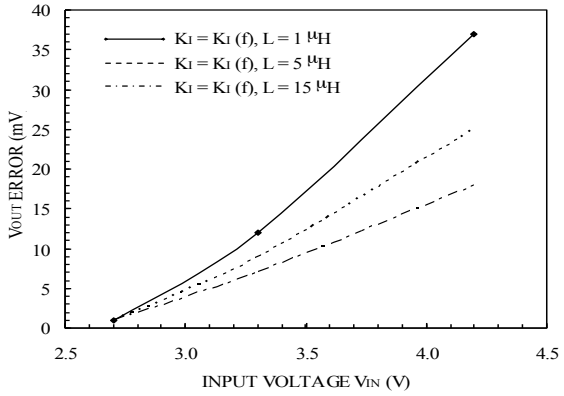

Fig. 8. Variation of steady-state V_{OUT} error with V_{IN} and L.

Switching frequency f_{SW} decreases with increasing inductance and V_{IN} values, as predicted by Eq. 13 and shown in Fig. 9. However, since K_I decreases with frequency, the variation in frequency is 15% lower than it would have been with a constant K_I (Fig. 9), which is typically the case in conventional ΣΔ controller circuits. Steady-state variations in load had little impact on either the steady-state error or f_{SW} because the DC voltage gain is relatively high at low frequencies (low DC errors) and low at high frequencies, when the current loop dominates (current loop is virtually unaffected by the load).

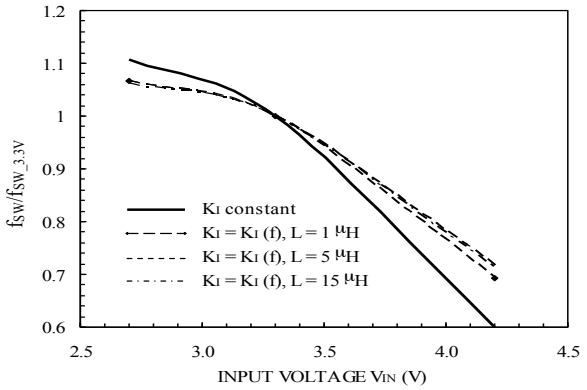

Fig. 9. Switching frequency versus V_{IN} (normalized to its value at 3.3V).

V. Conclusion

A ΣΔ 2.7-4.2V to 5V boost converter with 1% regulation accuracy that is stable for LC values 1-30µH and 15-350µF has been presented and analyzed. Low steady-state errors were achieved by carefully designing voltage-loop gain K_V to be high at low frequencies and stability assured by having current-loop gain K_I dominate at high frequencies, masking the right-hand plane zero and complex-conjugate poles of the voltage loop. The resulting variation in switching frequency f_{SW} with increasing input voltage V_{IN}, which is inherent to asynchronous ΣΔ converters, was reduced by 15% by decreasing the current-loop gain K_I at higher frequencies. The popularity of asynchronous ΣΔ buck converters is increasing because of its inherent stability and high bandwidth characteristics, and achieving similar features with boosting topologies is appealing and especially useful in battery-powered applications.

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