

# A Low Dropout, CMOS Regulator with High PSR over Wideband Frequencies

Vishal Gupta, *Student Member, IEEE*, and Gabriel A. Rincón-Mora, *Member, IEEE*

**Abstract-** Modern System-on-Chip (SoC) environments are swamped in high frequency noise that is generated by RF and digital circuits and propagated onto supply rails through capacitive coupling. In these systems, linear regulators are used to shield noise-sensitive analog blocks from high frequency fluctuations in the power supply. This work presents a low dropout regulator that achieves Power Supply Rejection (PSR) better than -40dB over the entire frequency spectrum. The system has an output voltage of 1.0V and a maximum current capability of 10mA. It consists of operational amplifiers (op amps), a bandgap reference, a clock generator, and a charge pump and has been designed and simulated using BSIM3 models of a 0.5 $\mu$ m CMOS process obtained from MOSIS.

## I. INTRODUCTION

The 21<sup>st</sup> century has witnessed an explosion in the demand for portable applications, such as cellular phones and personal digital assistants (PDAs) [1]. The principal requirements for these applications are low cost, high integration, and small size [2]. These requirements are pushing the design of SoC solutions, where dense analog and digital circuits are fabricated on the same die [3]. These SoC environments are plagued by noise, generated by the switching of digital circuits, RF blocks, and dc-dc converters, that can have amplitudes of the order of hundreds of millivolts and frequency components in the range of tens of kilohertz to hundreds of megahertz [4]-[7]. This noise, propagated onto the supplies through crosstalk, deteriorates the performance of sensitive analog blocks, like the synthesizer and VCO, and manifests itself as jitter in their output [4], [5], [8]-[11]. This jitter, in turn, deleteriously impacts critical system specifications like the selectivity of the receiver, spectral purity of the transmitter, and phase error tolerance of digital circuits [4]. In such an environment, a linear regulator is entrusted with the task of shielding noise-sensitive blocks from high frequency fluctuations in the power supply [3]-[5], [9]-[15]. This makes the design of linear regulators that have a high PSR over a wide frequency range extremely critical for high system performance.

Another important requirement for regulators for SoC applications is low dropout [4]. As supply voltages for portable applications continue to shrink, maintaining PSR performance while reducing a regulator's dropout voltage, the minimum voltage difference between its supply and output for accurate operation, is critical. Further, as systems aggressively

advance towards integration, these state-of-the-art regulators are increasingly integrated "on-chip" and deployed at the point-of-load, with output currents in the range of 10 – 50 mA [9]-[15]. This strategy allows the regulators to be optimized to cater to the specific demands of the sub-systems that load them [4]. Also, on-chip capacitors (10-200 pF) can often be used for frequency compensation [9]-[15], thereby conserving board-space and leading to increasing levels of integration. Since the regulators do not use an external capacitor to establish the dominant low-frequency pole, they are termed "internally compensated regulators".

In this work, the basic linear regulator and current schemes used for obtaining high PSR performance are discussed in Section II. Section III presents the system and circuit level description of the proposed technique. Section IV presents the simulation results. Conclusions are drawn in Section V.

## II. BACKGROUND

### A. Basic Linear Regulator

Fig. 1 depicts the block diagram of a typical internally compensated regulator consisting of an error amplifier, a pass device, and output capacitor  $C_{out}$ , which establishes output pole  $p_{out}$  [3]-[5], [9]-[15]. The amplifier is characterized by its transconductance, output resistance  $R_{o-A}$ , and corresponding bandwidth  $BW_A$ , which determines the dominant pole in internally compensated regulators. The effective capacitance at the output of the error amplifier  $C_{o-A}$  can be produced through Miller compensation or a capacitor to ground for the case of a PMOS or NMOS output stage, respectively. The large series pass device (NMOS or PMOS) has a high transconductance and low drain-source series resistance. Bias resistors  $R_1$  and  $R_2$  are the feedback network and are typically very large for low quiescent power consumption.

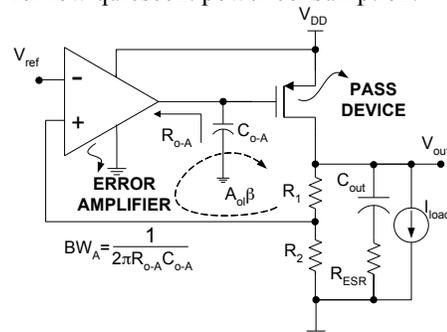


Fig. 1. Block diagram of simple linear regulator (pass device may be PMOS or NMOS).

### B. Current Techniques to Obtain High PSR

The analysis of the PSR of linear regulators follows readily from that of operational amplifiers, which have been analyzed

V. Gupta is with the Georgia Tech Analog and Power IC Design Lab, Georgia Institute of Technology, Atlanta, GA 30318 USA (email: vishalg@ece.gatech.edu, phone: 404 894 1299).

G. A. Rincón-Mora is with the Georgia Tech Analog and Power IC Design Lab, Georgia Institute of Technology, Atlanta, GA 30318 USA (email: rincon-mora@ece.gatech.edu).

in [11], [16]-[18]. In [19], an intuitive, potential-divider-based model for analyzing the PSR of linear regulators over a wide range of frequencies was presented. Curves ‘1’ and ‘2’ in Fig. 2 represent a typical PSR curve of a conventional internally compensated linear regulator, without and with the presence of Equivalent Series Resistance (ESR) of  $C_{out}$  [19]. The model predicted that the PSR at low frequencies, its dominant zero, and two subsequent poles corresponded to the dc open loop gain ( $A_{ol}\beta$ ), the bandwidth of the error amplifier ( $BW_A$ ), the unity-gain frequency of the system (UGF), and the output pole ( $p_{out}$ ), respectively. These curves indicate the worst-case PSR occurs in the vicinity of the UGF of the system, typically in the range of 1-10MHz [9], [10], [16]-[19]. Intuitively, the loop gain provides high supply ripple rejection at low frequencies, while the output capacitor shunts any ripple appearing at the output to ground at very high frequencies.

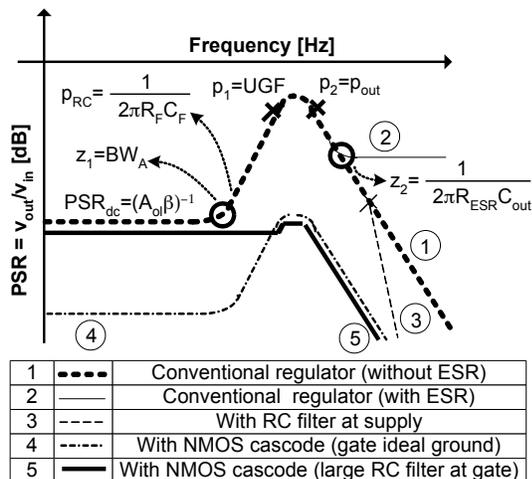


Fig. 2. PSR curve of a linear regulator.

Numerous techniques have been used to improve the PSR of linear regulators. The simplest solution is to place an RC filter in line with the power supply to filter out fluctuations before they reach the regulator [5], as shown in Fig. 3(a). This adds a pole to the PSR curve at the filter’s corner frequency, as shown by curve ‘3’ in Fig. 2. However, for an integrated SoC solution, the high power losses and reduction in voltage headroom caused by this resistor would severely limit its size, pushing the pole to very high frequencies. Another methodology, shown in Fig. 3(b), employs two linear regulators in series to effectively “double” the PSR [5]. This method has the obvious disadvantage of increased power dissipation and voltage headroom. Also, obtaining a high PSR over a wide frequency range is still prohibitive, given that both regulators have similar limitations.

Fig. 3(c) presents a methodology that utilizes an NMOS cascode for the NMOS pass device of the linear regulator, thereby isolating it from the noisy power supply [9]. The gate of the cascoding NMOS and the supply of the error amplifier have been boosted using two charge pumps in order to yield a low dropout voltage. The error amplifier, however, cannot be similarly cascoded since the gate of its NMOS cascode would require a boosted voltage of two gate-source drops above the output, leading to higher circuit complexity. Hence, it uses an

RC filter to suppress fluctuations in the power supply and the systematic fluctuations of the charge pump. Since the error amplifier consumes a significant current for high bandwidth, and the resistor in the RC filter is large for a low corner frequency, the voltage drop across the resistor causes a large droop in the output voltage of the charge pump. Hence, the charge pump has been regulated, thereby adding complexity, layout area, and power consumption.

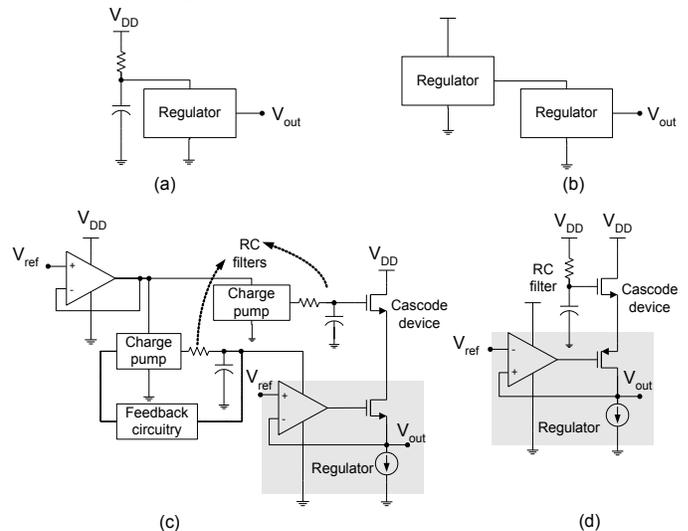


Fig. 3. Previously implemented topologies for high PSR.

In [10], a PSR of -40 dB over a wide frequency range is achieved using an NMOS device to cascode the PMOS pass device of a linear regulator, as shown in Fig. 3(d). Due to relatively high voltage headroom (3.3V) the gate of the NMOS cascode is biased through the supply using a simple RC filter. The high voltage headroom also allows the error amplifier, which is powered directly from the supply, to use cascodes and gain boosting to improve its PSR performance. This increases circuit complexity, dropout voltage, and power consumption. This work presents a topology that achieves a comparable PSR while exhibiting a lower dropout voltage, crucial for low-voltage, portable applications. The topology, described in the next section, is presented in Fig. 4.

### III. SYSTEM DESCRIPTION

#### A. NMOS Cascode

NMOS device  $M_{CAS}$ , shown in Fig. 4, decouples the entire linear regulator from fluctuations in the power supply through its cascoding effect (effective series resistance), thereby increasing PSR over a wide range of frequencies, as shown by curve ‘4’ in Fig. 2. Since the regulator has a low dropout,  $M_{CAS}$  cascodes the error amplifier of the linear regulator along with its pass device, thereby eliminating the need for gain boosting used in [10]. Further, the design uses only one charge pump, as opposed to two in [9], thereby conserving layout area and reducing added noise. The charge pump, described next, boosts the voltage at the gate of  $M_{CAS}$  to yield low dropout performance.

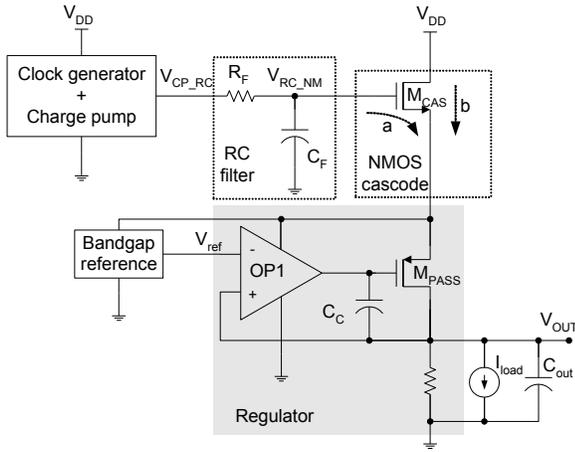


Fig. 4. Block diagram of system.

### B. Charge Pump

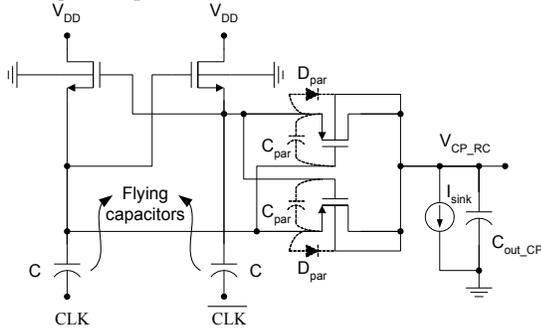


Fig. 5. Schematic of charge pump.

The charge pump boosts the voltage at the gate of the NMOS cascode to an optimal voltage level above the supply, to produce low dropout. The circuit has been optimized, using parasitic capacitors  $C_{par}$  and diodes  $D_{par}$  across the output switches and a very low current sink  $I_{sink}$  at the output, to produce a voltage lower than  $2V_{DD}$  so that  $M_{CAS}$  is operating in saturation [9]. A simplified schematic of the topology implemented is presented in Fig. 5 [20]. The clock generator is an inverter chain, similar to that in [9].

### C. RC Filter

Curve '4' in Fig. 2 is valid if the gate of the cascode  $M_{CAS}$  is an ideal ground. However,  $M_{CAS}$  simply acts as a voltage follower for signals at its gate. Hence, it is absolutely critical to shield its gate from noise in the power supply, as this would be transferred without attenuation to the linear regulator at its source, producing curve '1' in Fig. 2. This function is performed by the RC filter.

Referring to Fig. 4, the RC filter, comprising of  $R_F$  and  $C_F$ , filters out high frequency fluctuations in the power supply to attenuate power supply noise reaching the gate of the NMOS cascode and hence to the regulator through path 'a'. In other words, the RC filter adds a pole to the path 'a', affecting the PSR curve in a manner similar to that of an RC filter in series with the supply. However, since this RC filter is placed in a path that does not carry any dc current, the resistor can be made as large as practically possible, to yield a pole extremely close to dominant zero ( $BW_A$ ) of the PSR curve '1' in Fig. 2. Hence, the effective PSR of the system, following curve '1' at

low frequencies and curve '4' at high frequencies, is traced by curve '5' in Fig. 2. In this topology, the corner frequency of the RC filter is 3KHz, which has been obtained using a 700K $\Omega$  resistor and 70pF capacitor.

The RC filter also suppresses the systematic ripple generated by the charge pump. Since the charge pump is connected the gate of the NMOS cascode through this RC filter and is not supplying current to an active load, it does not exhibit any droop in output voltage and has not been regulated, leading to lower circuit complexity.

### D. Bandgap Reference

A schematic of the CMOS bandgap reference is presented in Fig. 7 [21]. The op amp in this circuit provides a loop gain of 60dB. The PSR of the bandgap reference is important as fluctuations at the output of the reference at frequencies lower than the gain bandwidth of the regulator, when the loop gain is greater than unity, can appear at the output of the regulator. However, the PSR of the bandgap reference can be significantly enhanced by increasing the loop gain of the op amp and by placing a relatively large capacitor  $C_{out\_BG}$  at its output to shunt the output ripple to ground at high frequencies [22], [23]. However this increases startup time of the circuit.

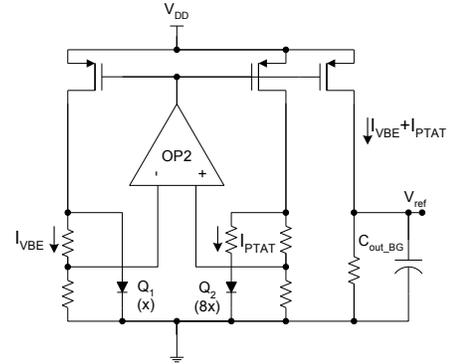


Fig. 6. Schematic of bandgap reference circuit.

### E. Op Amps

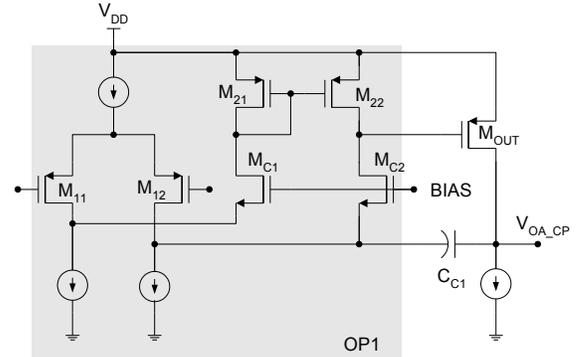


Fig. 7. Schematic of op amp OP2 use in bandgap reference (shaded region shows OP1 used in low dropout regulator).

The two op amps in the system are OP1 and OP2 used in the low dropout regulator, in Fig. 4 and the bandgap reference, in Fig. 6. Their schematics are presented in Fig. 7. The PSR of OP2 has been improved by eliminating the feedforward path of the Miller capacitor by using the grounded gate cascode technique described in [18]. This topology produces a worst-case PSR of 30 dB. However, it is difficult to implement this

topology as a regulator with  $M_{OUT}$  as the pass device since the condition that ensures stability for this circuit requires cascode devices  $M_{C1}$  and  $M_{C2}$  to have a higher transconductance than that output device  $M_{OUT}$ , [18] which is difficult to satisfy if the latter has to source large dc currents. PSR performance at low frequencies can be improved by implementing this op amp as a buffer preceding the charge pump. Op amp OP1 is shown in the shaded region in Fig. 6.

#### IV. SIMULATION RESULTS

This system was simulated using BSIM3 models of AMI's 0.5 $\mu$ m CMOS process, obtained from MOSIS. The system was designed to source an output current of 10mA while maintaining an output voltage at 1.0V. Figs. 8(a) and 8(b) present the output voltage as a function of temperature and load current for various supply voltages. The minimum voltage headroom required by the system is given by

$$V_{DD-min} = \max\{V_{TP} + 4V_{ds-sat}, V_{out} + 2V_{ds-sat}\}, \quad (1)$$

which, given a  $V_{TP}$  of 0.9V for this process, is approximately 1.6V.

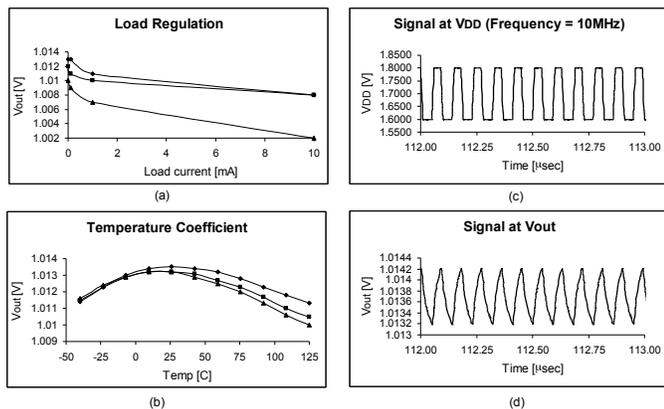


Fig. 8. (a) Temperature coefficient, (b) load regulation, (c) ripple at power supply, and (d) ripple at output of regulator, showing PSR of -40dB.

Figs. 8(c) and 8(d) show that a 10MHz, 200mVpp ripple at the power supply produces a 1mVpp ripple at  $V_{out}$ . This simulation, at the lowest operating supply voltage of 1.6V and maximum load current of 10mA, shows that the worst-case PSR of the system is -40dB. A PSR, comparable to that obtained in [9], [10] has been obtained by cascading the error amplifier and pass device of a low dropout regulator from fluctuations in the power supply.

#### V. CONCLUSIONS

A system that achieves a PSR better than -40dB over a large bandwidth has been designed. The system has an output voltage of 1.0V and can source 10mA of current. It utilizes a simple NMOS cascoding device to shield a low dropout regulator from fluctuations in the power supply. The gate of the NMOS cascode has been boosted to voltages above the supply rail using a charge pump and has been kept free of high frequency supply fluctuations using a simple RC filter and op amp. The system has been simulated in a 0.5 $\mu$ m CMOS process. In conclusion, a low-voltage scheme to obtain high PSR over a large bandwidth for a linear regulator for state-of-

the-art SoC environments has been presented.

#### REFERENCES

- [1] R. Tummala, *Fundamentals of Microsystems Packaging*, New York, NY: McGraw-Hill, 2002.
- [2] K. R. Volk (2002, July 09), "Dealing with noise when powering RF sections in cellular handsets." [Online] Available: [http://www.commsdesign.com/design\\_corner/showArticle.jhtml?articleID=16505374](http://www.commsdesign.com/design_corner/showArticle.jhtml?articleID=16505374)
- [3] S. Bruederle (2002, Nov. 04), "System on Chip: Driver of next generation wireless growth." [Online] Available: <http://www3.gartner.com/pages/story.php.id.2916.s.8.jsp>
- [4] Dallas Semiconductor/Maxim, Appl. Note 898, "Selecting LDO linear regulators for cellphone designs." [Online] Available: [http://www.maxim-ic.com/appnotes.cfm/appnote\\_number/898](http://www.maxim-ic.com/appnotes.cfm/appnote_number/898)
- [5] Dallas Semiconductor/Maxim, Appl. Note 883, "Improved power supply rejection for IC linear regulators." [Online] Available: [http://www.maxim-ic.com/appnotes.cfm/appnote\\_number/883](http://www.maxim-ic.com/appnotes.cfm/appnote_number/883)
- [6] L. R. Zheng, B. X. Li, and H. Tenhunen, "Efficient and accurate modeling of power supply noise on distributed on-chip power networks," in *Proc. IEEE Intl. Symp. Circuits Systems*, Geneva, 2000, pp. II-513-II-516.
- [7] S. Zhao and K. Roy, "Estimation of switching noise on power supply lines in deep sub-micron CMOS circuits," in *Proc. 13<sup>th</sup> Intl. Conf. VLSI Design*, Calcutta, 2000, pp. 168-173.
- [8] P. Larsson, "Power supply noise in future ICs: A crystal ball reading," in *Proc. IEEE Custom Integrated Circuits Conf.*, San Diego, 1999, pp. 467-472.
- [9] C. Lee, K. McClellan, and J. Choma Jr., "A supply-noise-insensitive CMOS PLL with a voltage regulator using dc-dc capacitive converter," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1453-1463, Oct. 2001.
- [10] J. M. Ingino, and V. R. von Kaenel, "A 4-GHz clock system for a high-performance system-on-a-chip design," *IEEE Jour. of Solid-State Circuits*, vol. 36, pp. 1693-1698, Nov. 2001.
- [11] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. New York, NY: Oxford University Press, 2002.
- [12] H. Tanaka, M. Aoki, T. Sakata, S. Kimura, N. Sakashita, H. Hidaka, T. Tachibana, and K. Kimura, "A precise on-chip voltage generator for a gigascale DRAM with a negative word-line scheme," *IEEE Jour. of Solid-State Circuits*, vol. 34, pp. 1084-1090, Aug. 1999.
- [13] V. R. von Kaenel, "A high-speed, low-power clock generator for a microprocessor application," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp. 1634-1639, Nov. 1998.
- [14] G. W. den Besten and B. Nauta, "Embedded 5V-to-3.3V voltage regulator for supplying digital IC's in 3.3V CMOS technology," *IEEE Jour. of Solid-State Circuits*, vol. 33, pp. 956-962, July 1998.
- [15] G. Heftman, "Powering the communications infrastructure." [Online] Available: [http://www.national.com/appinfo/power/files/BasicsDesign\\_HighVoltageComms\\_Feb04.pdf](http://www.national.com/appinfo/power/files/BasicsDesign_HighVoltageComms_Feb04.pdf)
- [16] M. S. J. Steyaert, W. M. C. Sansen, "Power supply rejection ratio in operational transconductance amplifiers," *IEEE Trans. Circuits Sys.*, vol. 37, pp. 1077-1084, Sept. 1990.
- [17] E. Säckinger, J. Goette, W. Guggenbül, "A general relationship between amplifier parameters, and its application to PSRR improvement," *IEEE Trans. Circuits Sys.*, vol. 38, pp. 1173-1181, Oct. 1991.
- [18] D. B. Ribner, and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE Jour. of Solid-State Circuits*, vol. 6, Dec. 1984.
- [19] V. Gupta and G. A. Rincón-Mora, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proc. IEEE SOC Conf.*, Santa Clara, 2004, pp. 311-315.
- [20] P. Favrat, P. Deval, and M. J. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE Jour. Solid-State Circuits*, vol. 33, pp. 410-416, March 1998.
- [21] K. N. Leung and P. K. T. Mok, "A sub-1V 15ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE Jour. Solid-State Circuits*, vol. 37, pp. 526-530, April. 2002.
- [22] G. Giustolisi and G. Palumbo, "A detailed analysis of power-supply noise attenuation in bandgap references," *IEEE. Trans. Circuits Systems*, vol. 50, pp. 185-197, Feb. 2003.
- [23] M. Ozbas, D. Patru, and P. R. Mukund, "Power supply noise coupling in a standard voltage reference circuit," in *Proc. IEEE SOC Conf.*, 2003, pp. 319-322.