Dimming DC–DC LED Drivers: Luminous Efficiency, Power Losses, & Best-in-Class

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Abstract—Light Emitting Diodes (LEDs) have become pervasive in modern lighting and automotive applications. LED drivers regulate LED current which sets their luminous output, where dimming is an important attribute. Dimming techniques fall in one of two categories: "analog" or "duty-cycled" (pulse-width-modulated), and duty-cycled (PWM) dimming decomposes into three further classes: shutdown, shunt- and series-switched. However, a comprehensive analysis of dimming techniques, corresponding power losses, and their dimming capabilities is lacking in the literature. This paper explains and quantifies those in the context of a switched inductor (SL) DC–DC converter. Presented analysis incorporates SL conversion efficiency and models luminous flux, dimming range, and luminous efficiency. This paper reveals and verifies that analog dimming is up to 57% more efficient with the widest dimming range.

Index terms—LED driver, switched inductor, DC–DC, dimming, analog, duty-cycled, PWM, CMOS.

I. DC-SOURCED LED DRIVERS

LEDs, owing to their compact size, high reliability, fast response and high electro-optical conversion efficiency have largely substituted conventional incandescent and chloro-fluorescent lights in high-power (> 1 W) applications [1]–[2]. These include AC-sourced lighting, and battery-operated automotive applications [2]–[6]. Since LEDs operate on DC currents, AC-powered LED driver systems constitute an intermediate AC–DC conversion step followed by a DC–DC regulation stage. Which depending on the topology can power reverse, inverting and non-inverting load configurations [3] as Fig. 1 illustrates.

Fig. 1: LED driver system.

Thermal constraints in these high-power compact systems demand high efficiency. Luminous efficiency \( \eta_L \) which is light delivered per unit input power \( P_{IN} \) constitutes \( \eta_C \), a fraction of \( P_{IN} \) delivered to the load. Linear regulators, even with low dropouts (LDO), fail to meet expectations owing to their poor \( \eta_C \) at typical > 100 mA loads. Furthermore, LDOs cannot supply LED voltages greater than input. SL converters which on-the-other-hand can provide greater than 85% \( \eta_C \) and can boost \( V_{IN} \) are best suited for LED driver applications [3]–[4].

LED drivers regulate DC-output current \( i_O \) instead of voltage because LED’s brightness is proportional to \( i_O \) [7]–[8]. Controlling \( i_O \) to vary the brightness is referred to as dimming, a vital feature of LED drivers. Dimming techniques are classified into two categories, analog and duty-cycled (or PWM) [9]. In analog, \( i_O \) is varied continuously whereas in duty-cycled, it is pulse-width modulated to an average during a fixed period. Dimming range captures the dimming capability of a driver.

State-of-the-art dimming fails to consider effects of power stage \( \eta_C \) in \( \eta_L \) [9]–[10], does not analyze dimming range [7]–[9] and lacks a quantitative comparison of dimming techniques [11]. This research models and validates those using SPICE simulations. Furthermore, an analysis reveals the best-in-class technique. Section II introduces analog dimming in the context of a SL LED driver, while Section III explains the state-of-the-art PWM dimming techniques. Section IV compares and assesses the techniques, and Section V concludes the paper.

II. ANALOG DIMMERS

A. Operation

Figure 2 depicts a typical SL buck-boost LED driver power stage consisting of power switches \( M_{BI}, M_{EG}, M_{DG}, M_{DO} \), their corresponding gate drivers, and four series-connected power LEDs [12]–[13]. Switches \( M_{BE} \) and \( M_{EG} \) energize the inductor \( L_X \) from input \( V_{IN} \) during \( t_E \), and \( M_{DG} \) and \( M_{DO} \) de-energize to output \( V_O \) during \( t_D \). This occurs during the conduction period \( t_C \), which is equal to switching period \( t_{SW} \) in Continuous Conduction Mode (CCM) as Fig. 3 shows. A drain duty-cycled fraction \( i_{DO} \) of inductor current \( i_L \) is delivered to the output, which the capacitor \( C_O \) filters to \( i_{O(AVG)} \).

Energizing and drain duty cycles \( d_E \) and \( d_D \) are a \( t_E \) and \( t_D \) fraction of \( t_C \). The average output LED current \( i_{O(AVG)} \) is a \( d_D \) translation of the average inductor current, \( i_{O(AVG)} = i_{O(AVG)} \),

\[
d_E = \frac{t_E}{t_C} = 1 - d_D = 1 - \frac{V_{IN}}{V_{IN} + V_O}, \quad (1)
\]

\[
i_{O(AVG),CCM} = i_{O(AVG)} = i_{O(AVG)} \cdot d_D. \quad (2)
\]

Fig. 2: Switched inductor buck-boost LED driver power stage.

Fig. 3: Simulated CCM operation.
SL transitions to Discontinuous Conduction Mode (DCM) as \(i_0\) decreases. \(L_x\) energizes during \(t_e\), transfers energy during \(t_d\) and stops conducting as Fig. 4 shows. Varying \(t_{SW}\) with fixed \(i_0\) energy packets dims the average \(i_0\). Like CCM, \(C_0\) filters the drain current ripple (\(\Delta i_L = i_{L(PK+)}\)) in DCM:

\[
i_{(AVG,DCM)} = i_{(AVG,PK)} = i_{(AVG,PK)}(\frac{t_c}{t_{SW}}) = \frac{(i_{(PK)})}{d_D}.
\]

(3)

Sensing and controlling \(i_{(AVG)}\) and \(i_{(AVG)}\) over their entire range dims the LEDs as Figs. 3 and 4 shows. Since sparse \(i_c\) pulses can be delivered to the LEDs in DCM, the resulting \(i_{(AVG)}\) in (3) can be infinitesimally small. Therefore, analog dimming theoretically has a 0-100% dimming range.

**B. Luminous Efficiency**

Luminous efficiency \(\eta_L\) is light delivered per unit input power \(P_{IN}\). Measured in lumens-per-watt, it is a cascaded measure of SL’s \(\eta_{C}\) and LED’s electro-optical efficiency \(\eta_{LED}\):

\[
\eta_L = \eta_{C} \eta_{LED} = \left( \frac{P_{O}}{P_{IN}} \right) \left( \frac{\phi_L}{\phi_k} \right),
\]

(4)

where \(P_{O}\) is the fraction of power that SL delivers. As a result, quantifying \(\eta_L\) calls for modeling the luminous output \(\phi_L\) and electrical parameters \(P_{O}\), \(\eta_{C}\), and \(P_{IN}\). As Fig. 5 shows, \(\phi_L\) (extracted from datasheet) varies exponentially with LED current \(i_0\):

\[
\phi_L \approx N_D \phi_k \left( 1 - e^{-i_0/i_k} \right),
\]

(5)

where \(N_D\) is the number of series-connected LEDs (i.e., 4), and \(\phi_k = 356\) and \(i_k = 1.07\) are the modeled LED-dependent constants for cool-white CREE XP-E2 LED [14]. (5) can be rewritten as a logarithmic function of \(\phi_L\) as:

\[
i_{(PK)} = \frac{1}{i_k} \ln \left( \frac{\phi_L}{N_D \phi_k} \right).
\]

(6)

This non-linearity is also reflected in \(\eta_L\) as shown in Fig. 9. \(\eta_L\) falls at high \(\phi_L\)’s because disproportionately higher \(P_{IN}\) is needed to deliver same \(\Delta \phi_L\). At low loads, SL power losses overwhelm \(P_{O}\) and eventually \(\eta_L\) peaks and drops.

**III. DUTY-CYCLED DIMMERS**

Duty-cycled or pulse-width modulated (PWM) dimming is another way to dim the LEDs. Unlike analog, PWM achieves dimming by duty-cycling a fixed \(i_0\) at frequency much lower
than SL’s switching frequency \( f_{SW} \). Typically, this duty-cycled frequency \( f_{PWM} \) is on the order of 0.1–1 kHz [3]–[4]. Based on how it is achieved, it can be categorized as shutdown and its modified versions, shunt- and series-switched.

### A. Shutdown Operation

The simplest way to PWM-dim is by disabling the power-stage during PWM-OFF time \( t_{PWM(OFF)} \) using an external dimming signal \( v_{DIM} \) [16]–[17]. This means opening \( M_{EI} \) and \( M_{EG} \) and draining the inductor via closed \( M_{DG} \) and \( M_{DO} \). Exponentially decreasing \( i_{O} \) discharges \( C_O \), turning the LEDs OFF as Fig. 10 shows. Note that primed variables are regulated non-dimmed currents and voltages.

![Fig. 10: Shutdown duty-cycled dimming operation.](image)

The average output current is a PWM duty cycle \( d_{PWM} \) fraction of duty-cycled average \( i_{O}' \):

\[
i_{O(AVG)} = d_{PWM} i_{O(AVG)}' = d_{PWM} i_{I(LAVG)}',
\]

where \( i_{O}' \) is the regulated inductor current. The power stage is then enabled with \( v_{DIM} \), charges \( C_O \) linearly and operates normally during PWM-ON time \( t_{PWM(ON)} \).

**Dimming Range**: Dimming range for PWM is like analog in a way that it is defined as minimum to maximum luminous \( \phi_L \).

\[
\phi_L \propto i_{O(AVG)}, \text{ which in PWM depends on minimum } d_{PWM}:
\]

\[
d_{PWM} \geq \frac{t_F}{t_{PWM}},
\]

where \( t_R \) and \( t_F \) are the \( i_O \) rise and fall times respectively. \( t_{PWM} \) is the total period of the external PWM dimming signal \( v_{DIM} \).

\( t_R \) and \( t_F \) consist of two components, inductor current slew \( t_L \) and output capacitor voltage slew \( t_C \). When \( v_{DIM} \) turns on, SL switches and \( L_X \) slews to its regulation point \( i_{O}' \), a reverse \( d_0 \) translation of \( i_{O} \). Following this, SL transfers energy to the output and charges \( C_O \). Similarly, at \( t_{PWM(OFF)} \) instance \( L_X \) de-energizes to zero, followed by \( C_O \) discharge. Both \( t_R \) and \( t_F \) are represented by:

\[
t_{R/F} = t_L + t_C = \frac{L_X}{v_L} \left( \frac{i_{O}'}{d_0} \right) + \frac{C_O \Delta V_O}{i_{I(AVG)}'},
\]

where \( v_L \) is the \( L_X \) voltage \( v_{IN} \) during energizing and \( v_O \) during the de-energizing phase and \( k \) is the charging or discharging \( C_O \) current. \( \Delta V_O \) is established from (7). Over \( t_R \), average \( i_{C(B)} \) is composed of the duty-cycled charging \( i_{O}' \) and discharging LED current \( i_{O} \):

\[
i_{C(R)(AVG)} = i_{O(AVG)}' - i_{O(R)(AVG)} \approx i_{I(LAVG)}' d_0 - \Delta i_{O(R)(AVG)}'.
\]

Fig. 11: \( t_{R/F} \) approximations for shutdown.

**Power-Loss Analysis**: Power stage conversion efficiency loss \( \eta_{PSL} \) is common to both analog and duty-cycled dimming. Since \( \eta_L \) tends to saturate at higher \( i_O \)s (from Fig. 5), duty-cycled dimming suffers from additional PWM power loss \( \Delta P_{PWM} \):

\[
\Delta P_{PWM} = P_{IN(PWM)} - P_{IN(A)} = P_{IN(A,PK)} d_{PWM} - P_{IN(A)},
\]

where \( P_{IN(A,PK)} \) is the analog input power at peak \( i_{O}' \) (i.e., 1 A). \( \Delta P_{PWM} \) is zero at both \( i_O \) extremes because analog and PWM dimming consume the same zero and peak \( P_{IN} \) as Fig. 12 shows.

![Fig. 12: Input power and \( P_{PWM} \) vs. luminous flux.](image)

Because duty-cycled dimming has a fixed bias point at regulated \( i_O' \), the corresponding \( \eta_L \) is 90% throughout the dimming range as Fig. 7 shows. All power losses are summarized in Fig. 13. Analysis reveals that \( \Delta P_{PWM} \) dominates SL’s power losses in both analog and PWM during majority of the dimming range, highlighting its inefficiency.

![Fig. 13: Breakdown of power losses in analog and PWM dimming.](image)
B. Shunt-Switched

Shunt-switched PWM dimming technique modifies shutdown by incorporating switch MPWM in parallel to the LEDs as Fig. 14 shows. Closing MPWM along with disabling SL discharges CO to ground, therefore turning-off the LEDs. Similarly, at the PWM-ON instance MPWM opens and SL charges CO which resumes normal LED operation as shown in Fig. 15.

![Fig. 14: SL LED driver for shunt-switched dimming.](image)

**Additional Power Losses:** Since MPWM eventually shunts CO to ground SL needs to recharge CO during PWM cycle. Therefore, leading to a capacitor energy PC loss of:

\[
P_C \approx \frac{1}{2} C_O \left( V_{O(AVG)} \right)^2 f_{PWM}. \tag{15}
\]

SL delivers remnant LX power PL to CO while turning-OFF, which is eventually shunted and dumped to ground:

\[
P_L \approx \frac{1}{2} L_X \left( i_{L(AVG)} \right)^2 f_{PWM}. \tag{16}
\]

Furthermore, closing MPWM consumes gate-charge power PG that \(V_{DD}\) supplies with charge \(q_G\). \(q_G\) is the charge that overlap capacitance \(C_{OL}\) and channel capacitance \(C_{CH}\) which constitute gate-drain and gate-source capacitances, need to close MPWM:

\[
P_G = v_{DD} \left( \frac{q_G}{f_{PWM}} \right) = v_{DD} q_G f_{PWM}, \tag{17}
\]

\[
q_G \approx C_{OL} \left( 2 v_{DD} + v_O \right) + C_{CH} \left( v_{DD} + \frac{v_{TN}}{4} \right). \tag{18}
\]

These losses constitute the total additional power loss \(\Delta P_{SH}\) in shunt-switched, which is miniscule as compared to the prominent \(P_{SL}\) and \(\Delta P_{PWM}\) in Fig. 13. Fig. 16 depicts a breakdown of these additional losses. As shown, \(P_C\) overwhelms \(P_L\) and makes up the majority of \(\Delta P_{SH}\).

![Fig. 16: Breakdown of power losses in shunt-switched PWM dimming.](image)

**Dimming Range:** Like shutdown, \(t_F\) determines the minimum dimming range in shunt-switched PWM. Opening MPWM while switching SL pushes regulated \(i_O\) to initially shunted CO. LEDs conduct when CO is sufficiently charged, i.e., enough to allow 1\%\(i_O\). \(t_D\), therefore constitutes LX’s \(i_L(t_L)\) and CO’s \(v_O(t_C)\):

\[
t_F = t_L + t_C \approx \frac{L_X}{v_L} \left( \frac{i_o'}{d_o} \right) + \frac{C_O}{v_O} \left( AV_{DS(90-10\%)} + AV_{DS(90-90\%)} \right). \tag{19}
\]

\(v_O\)’s slew is divided into two components, when \(i_O\) rises from 0-1\%\(i_O\) and 1-90\%\(i_O\) as Fig. 17 shows. That is, one where drain duty-cycled \(i_o'\) flows just to CO and when it is shared with LEDs as \(i_O\) rises. The latter’s \(i_{AVG}\) is approximated from (13). \(v_O\)’s steep increase during the former causes \(d_D\) to vary from 100% to 55% as per (1), which averaged over this duration is 73%. \(i_{AVG}\) is therefore \(d_{AVG}\):(19).

\[
M_{PWM} \text{ closes in saturation because } V_O(V_{DS}) \text{ is higher than a } V_T \text{ subtracted from } V_{DD}(V_{GS}). \text{ Ten times } i_O \text{ discharges CO and hence steers current away from LEDs. } M_{PWM} \text{’s parameters } W_N \text{ and } L_{X} \text{ that support } 10i_O \text{ can therefore be designed accordingly:}
\]

\[
t_F = \frac{C_O}{v_O} \left( AV_{DS(10-10\%)} \right) \left( i_{AVG} \right)^2. \tag{20}
\]

Consequently, \(t_F\) is the time in which 10\%\(i_O\) discharges CO by \(\Delta v_O(DF)\) to when \(i_O\) falls by 90%:

\[
\frac{C_O}{v_O} \left( AV_{DS(10-10\%)} \right) \left( i_{AVG} \right)^2. \tag{21}
\]

Calculated \(t_D\) and \(t_F\) are 118 \(\mu s\) and 1.65 \(\mu s\) which are within 8% and 3% of simulations. This puts dimming range of 1.15% within 4% of its simulations.

![Fig. 17: \(t_D\) for shunt-switched PWM.](image)

C. Series-Switched

Series-switched PWM dimming is another modification to SL shutdown [18]. In addition to the power stage shutdown, series-connected PMOS MPWM switches \(i_O\) with \(V_{DIM}\) as shown in Figs. 18 and 19.

![Fig. 18: SL LED driver for series-switched dimming.](image)

At PWM-ON instance, SL switches to energize LX to its \(i_L'\). Followed by an energizing \(L_X\) slow delay \(t_{PRE}\), MPWM connects SL to the LED load:

\[
t_{PRE} \approx \left( \frac{L_X}{V_{IN}} \right) \left( i_L(AVG) \right). \tag{22}
\]
This SL pre-charge mechanism \([19]\) in-tandem with \(C_O\)’s \(v_{CO}\) preservation (discussed later) during \(t_{PWM(OFF)}\) allows instantaneous LED current rise. Like shunt-switched, SL is disabled when \(M_{PWM}\) disconnects, which limits \(C_O\) overcharge.

**Fig. 19:** Series-switched PWM operation.

### Additional Power Losses:
SL delivers remnant \(L_X\) power \(P_L\) to \(C_O\) while turning-OFF which can lead to an overcurrent spike at the \(t_{PWM(ON)}\) instance, stressing the LEDs and other output-connected circuitry. A solution is to maintain output capacitor voltage \(v_{CO}\) during \(t_{PWM(OFF)}\). Variations of this concept have been implemented in modern LED drivers \([18]\)–\([24]\). Maintaining \(v_{CO}\) implies excess \(P_L\) in (16) is disregarded. Additionally, \(M_{PWM}\)’s ohmic loss \(P_{R(SW)}\) contributes to the overall \(\Delta P_{SE}\) loss, i.e.,

\[
P_{RSW} = (i_{OAVG})^2 R_{PWM} \Delta t_{PWM},
\]

\[
P_{PWM} = R_{CH} = \frac{1}{K_{T'} \left( \frac{W}{L_F} \right) \left( v_{TD} - |v_{TP}| \right) \left( v_{DD} - |v_{TP}| \right)}.
\]

For a typical 100 m\(\Omega\) resistance \(P_{RSW}\) is 100 mW at peak \(i_o'\) of 1 A. An inductor power loss \(P_L\) of 1.1 mW and gate charge loss \(P_G\) of 14.9 nW are further lost as per (17)-(18) as Fig. 20 shows.

**Fig. 20:** Breakdown of power losses in series-switched PWM dimming.

### Dimming Range:
\(M_{PWM}\) instantaneously connects SL power stage to the LEDs as soon as \(L_X\) slews to its regulation point. Larger \(C_O\) reduces \(\Delta v_{CO}\) because of \(L_X\) energy transfer during this connection instance. Therefore limiting \(\Delta i_O\) such that peak \(i_o\) is always within 10%\(i_o'\) as Fig. 21 shows. Eventually, switching dynamics of \(M_{PWM}\) determine the \(t_k\) and \(t_f\), which can be as low as a few nanoseconds providing a dimming capability of up to 0% for a 100 Hz dimming signal.

**Fig. 21:** \(t_{OE}\) for series-switched PWM.

### D. Luminous Efficiency
Since luminous output and drawn \(P_N\) are the same duty-cycled fraction of the peak biasing point \(i_o'\), \(\eta_L\) is constant across the dimming range as Fig. 9 shows. Furthermore, PWM dimming draws more power for the same amount of light as Fig. 12 shows reducing its luminous efficiency. Revealing that analog dimming is up to 57% more efficient over PWM.

### IV. DISCUSSION

Table I provides an overview and compares analog and duty-cycled dimming techniques. Analog dimming yields the highest \(\eta_L\), up to 57% more, over most of the luminous range as Fig. 9 shows. However, at low loads when SL losses outpace power delivered, \(\eta_L(PWM)\) overtakes. Hybrid dimming approaches where LED driver can modulate \(i_o'\) during PWM have been proposed to improve PWM \(\eta_L\) but it complicates control and requires additional current channels \([9]\)–\([10]\), \([25]\). Therefore, reducing its popularity.

Although analog dimming technique theoretically promises up to 0% dimming, in practice it’s a function of \(i_o\) or \(i_L\) sensing accuracy, noise and offsets, which can be improved by design \([12]\), \([26]\). Furthermore, it also depends on LED’s luminous characteristics. That is, if they can emit light at low enough \(i_o\).

 Shutdown dimming technique is often used in buck SLs where large \(C_{GS}\) are not needed to supply \(i_o\) during \(t_E\) \([27]\)–\([29]\). Therefore, reducing its \(t_{OE}\) and improving the dimming range. In boost SLs, \(L_X\)’s DC-short and body-diode conduction of \(M_{DO}\) eventually forces \(v_O\) to \(v_{IN}\) when shutdown. However, since typical boost SL’s \(v_O\) is 2-4x when operational \([18]\), \([20]\) and because of LEDs exponential I-V relationship \(i_o\) is negligible.

Shunt- and series-switched PWM dimming can also be extended to buck and boost SL topologies as Figs. 22(a)-(d) show. Dimming in boost using series-switched as depicted in Fig. 22(a) operates in the exact same way as buck-boost. However, grounding \(S_{PWM}\) during shunt-switched PWM would undesirably energize \(L_X\) via body-diode \(D_{DO}\) as Fig. 22(b) depicts. Directly shunting to \(v_{IN}\) instead of ground counters this.

**Fig. 22:** Buck and boost implementations of series- and shunt-switched PWM.

Buck topologies operate like their boost-based counterparts when series-switched as shown in Fig. 22(c). \(C_O\) absorbs additional \(P_L\) when \(S_{PWM}\) reconnects, limiting \(\Delta v_{CO}\) and \(\Delta i_O\). Contrary to buck-boost, bucks need not shutdown when shunt-switched \([30]\)–\([31]\). This is because they can de-energize to ground when \(S_{PWM}\) closes in Fig. 22(d). Not shutting SL also improves their dimming capabilities since \(L_X\) need not slew when SL restarts. However, this costs additional \(S_{PWM}\)’s ohmic and SL’s switching and ohmic power during \(t_{PWM(OFF)}\).
This paper reviews, analyses and assesses analog and duty-cycled (PWM) dimming techniques and its variations in DC–DC SL LED drivers. An example of buck-boost power-stage has been demonstrated which is 2% accurate for $\eta_L$, $P_{IN}$ and $\eta_L$ and 5% accurate for the dimming range when validated against SPICE simulations. Overall, analog dimming outperforms PWM in power losses, majority of $\eta_L$ and achieves 0-100% dimming range matching its best PWM dimming counterpart, emerging as the best-in-class.

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