Dimming DC–DC LED Drivers: Luminous Efficiency, Power Losses, & Best-in-Class

Vasu Gupta, *Graduate Student Member*, *IEEE* and Gabriel A. Rincón-Mora, *Fellow*, *IEEE*
Georgia Institute of Technology, Atlanta, Georgia 30332 U.S.A.
E-Mail: vasugupta@gatech.edu and Rincon-Mora@gatech.edu

***Abstract*— Light Emitting Diodes (LEDs) have become pervasive in modern lighting and automotive applications. LED drivers regulate LED current which sets their luminous output, where dimming is an important attribute. Dimming techniques fall in one of two categories: "analog" or "duty-cycled" (pulse-width-modulated), and duty-cycled (PWM) dimming decomposes into three further classes: shutdown, shunt- and series-switched. However, a comprehensive analysis of dimming techniques, corresponding power losses, and their dimming capabilities is lacking in the literature. This paper explains and quantifies those in the context of a switched inductor (SL) DC–DC converter. Presented analysis incorporates SL conversion efficiency and models luminous flux, dimming range, and luminous efficiency. This paper reveals and verifies that analog dimming is up to 57% more efficient with the widest dimming range.**

***Index terms*— LED driver, switched inductor, DC–DC, dimming, analog, duty-cycled, PWM, CMOS.**

I. DC-Sourced LED Drivers

LEDs, owing to their compact size, high reliability, fast response and high electro-optical conversion efficiency have largely substituted conventional incandescent and chloro-florescent lights in high-power (> 1 W) applications [1]–[2]. These include AC-sourced lighting, and battery-operated automotive applications [2]–[6]. Since LEDs operate on DC currents, AC-powered LED driver systems constitute an intermediate AC–DC conversion step followed by a DC–DC regulation stage. Which depending on the topology can power reverse, inverting and non-inverting load configurations [3] as Fig. 1 illustrates.

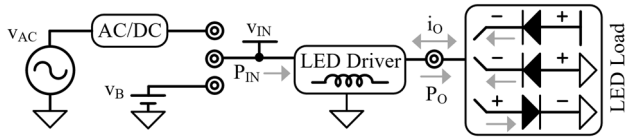

Fig. 1: LED driver system.

Thermal constraints in these high-power compact systems demand high efficiency. Luminous efficiency η_L which is light delivered per unit input power P_{IN} constitutes η_C, a fraction of P_{IN} delivered to the load. Linear regulators, even with low dropouts (LDO), fail to meet expectations owing to their poor η_C at typical > 100 mA loads. Furthermore, LDOs cannot supply LED voltages greater than input. SL converters which on-the-other-hand can provide greater than 85% η_C and can boost v_{IN} are best suited for LED driver applications [3]–[4].

LED drivers regulate DC-output current i_O instead of voltage because LED's brightness is proportional to i_O [7]–[8]. Controlling i_O to vary the brightness is referred to as dimming, a vital feature of LED drivers. Dimming techniques are classified into two categories, analog and duty-cycled (or PWM) [9]. In analog, i_O is varied continuously whereas in duty-cycled, it is pulse-width modulated to an average during a fixed period. Dimming range captures the dimming capability of a driver.

State-of-the-art in dimming fails to consider effects of power stage η_C in η_L [9]–[10], does not analyze dimming range [7]–[9] and lacks a quantitative comparison of dimming techniques [11]. This research models and validates those using SPICE simulations. Furthermore, an analysis reveals the best-in-class technique. Section II introduces analog dimming in the context of a SL LED driver, while Section III explains the state-of-the-art PWM dimming techniques. Section IV compares and assesses the techniques, and Section V concludes the paper.

II. Analog Dimmers

A. Operation

Figure 2 depicts a typical SL buck-boost LED driver power stage consisting of power switches (M_{EI}, M_{EG}, M_{DG}, M_{DO}), their corresponding gate drivers, and four series-connected power LEDs [12]–[13]. Switches M_{EI} and M_{EG} energize the inductor L_X from input v_{IN} during t_E, and M_{DG} and M_{DO} de-energize to output v_O during t_D. This occurs during the conduction period t_C, which is equal to switching period t_{SW} in Continuous Conduction Mode (CCM) as Fig. 3 shows. A drain duty-cycled fraction i_{DO} of inductor current i_L is delivered to the output, which the capacitor C_O filters to $i_{O(AVG)}$.

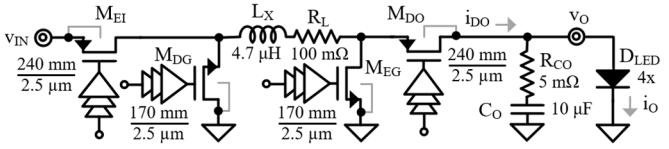

Fig. 2: Switched inductor buck-boost LED driver power stage.

Energizing and drain duty cycles d_E and d_D are a t_E and t_D fraction of t_C. The average output LED current $i_{O(AVG)}$ is a d_D translation of the average inductor current, *i.e.*:

$$d_E \equiv \frac{t_E}{t_C} = 1 - d_D = 1 - \frac{v_{IN}}{v_{IN} + v_O}, \quad (1)$$

$$i_{O(AVG,CCM)} = i_{DO(AVG)} = i_{L(AVG)} d_D. \quad (2)$$

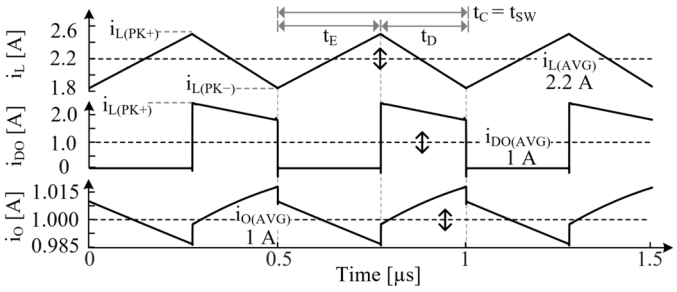

Fig. 3: Simulated CCM operation.

SL transitions to Discontinuous Conduction Mode (DCM) as i_O decreases. L_X energizes during t_E, transfers energy during t_D and stops conducting as Fig. 4 shows. Varying t_{SW} with fixed i_L energy packets dims the average i_O. Like CCM, C_O filters the drain current ripple ($\Delta i_L = i_{L(PK+)}$) in DCM:

$$i_{O(AVG,DCM)} = i_{DO(AVG)} = i_{L(AVG)} d_D = \left(\frac{i_{L(PK)}}{2}\right)\left(\frac{t_C}{t_{SW}}\right) d_D . \quad (3)$$

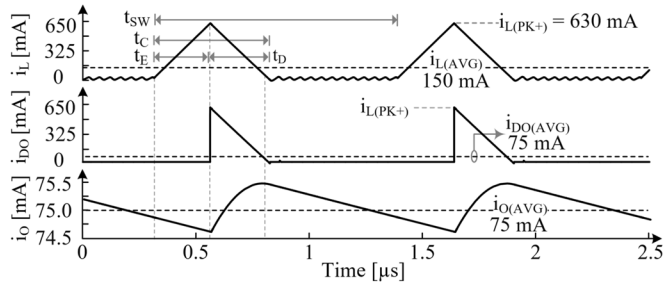

Fig. 4: Simulated DCM operation.

Sensing and controlling $i_{L(AVG)}$ and $i_{O(AVG)}$ over their entire range dims the LEDs as Figs. 3 and 4 shows. Since sparse i_L pulses can be delivered to the LEDs in DCM, the resulting $i_{O(AVG)}$ in (3) can be infinitesimally small. Therefore, analog dimming theoretically has a 0-100% dimming range.

B. Luminous Efficiency

Luminous efficiency η_L is light delivered per unit input power P_{IN}. Measured in lumens-per-watt, it is a cascaded measure of SL's η_C and LED's electro-optical efficiency η_{LED}:

$$\eta_L = \eta_C \eta_{LED} = \left(\frac{P_O}{P_{IN}}\right)\left(\frac{\phi_L}{P_O}\right), \quad (4)$$

where P_O is the fraction of power that SL delivers. As a result, quantifying η_L calls for modeling the luminous output ϕ_L and electrical parameters P_O, η_C, and P_{IN}. As Fig. 5 shows, ϕ_L (extracted from datasheet) varies exponentially with LED current i_O:

$$\phi_L \approx N_D \phi_k \left(1 - e^{-i_O/I_k}\right), \quad (5)$$

where N_D is the number of series-connected LEDs (*i.e.,* 4), and ϕ_k = 356 and I_k = 1.07 are the modeled LED-dependent constants for cool-white CREE XP-E2 LED [14]. (5) can be re-written as a logarithmic function of ϕ_L as:

$$i_O = \frac{1}{I_k} \ln\left(1 - \frac{\phi_L}{N_D \phi_k}\right)^{-1} . \quad (6)$$

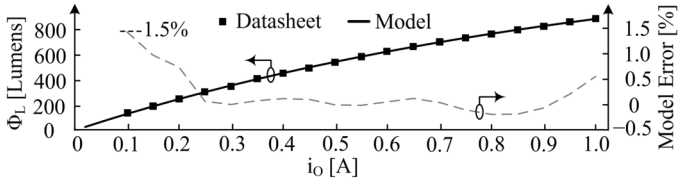

Fig. 5: Luminous flux vs. output current for four CREE XP-E2 LEDs.

Since LEDs are electrically modeled as diodes [8], output voltage v_O as shown in Fig. 6 is a logarithmic and linear R_D translation of i_O:

$$v_O = N_D\left(v_D + v_R\right) = N_D\left(n_I v_T \ln\frac{i_O}{I_S} + i_O R_D\right), \quad (7)$$

where v_D is diode voltage, v_R is the voltage across LED parasitic resistance R_D, n_I is the diode non-ideality factor and I_S is the reverse saturation current.

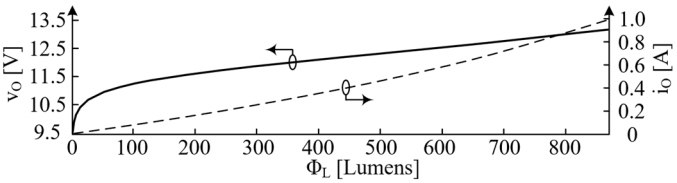

Fig. 6: Output voltage and current vs. luminous flux.

Power conversion efficiency η_C for the buck-boost SL in Fig. 2 is shown in Fig. 7 [13]. When lightly loaded in DCM, the i_O that sets P_O is so low that controller (P_Q) and gate-charge (P_G) losses swamp all other losses. In this region η_C climbs because these losses do not scale with i_O. η_C peaks as power stage's ohmic losses (P_R) match and surpass P_Q and P_G [15]. Power drawn P_{IN} is $1/\eta_C$ translation of P_O which is derived from (6), (7):

$$P_{IN} = \frac{P_O}{\eta_C} = \frac{v_O i_O}{\eta_C} \approx \frac{N_D\left(v_D + v_R\right)}{\eta_C}\left[-\frac{1}{I_k}\ln\left(1 - \frac{\phi_L}{\phi_k}\right)\right]. \quad (8)$$

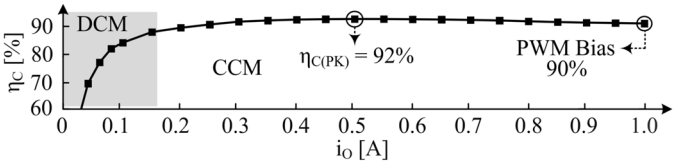

Fig. 7: Simulated conversion efficiency vs. output current.

Simulated and modeled P_{IN}, which are within 1.5% of each other are depicted in Fig. 8. LED's ϕ_L climbs non-linearly with i_O as shown in Fig. 5. Therefore, a disproportionately higher P_O (and hence P_{IN}) are drawn to maintain a consistent increase in ϕ_L as Fig. 8 highlights.

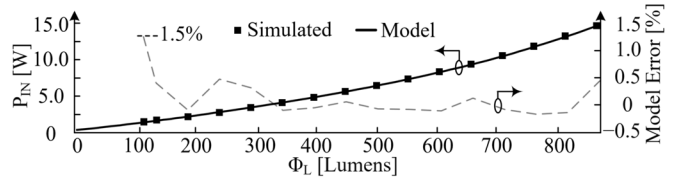

Fig. 8: Modeled and simulated input power vs. luminous flux

This non-linearity is also reflected in η_L as shown in Fig. 9. η_L falls at high ϕ_Ls because disproportionately higher P_{IN} is needed to deliver same $\Delta\phi_L$. At low loads, SL power losses overwhelm P_O and eventually η_L peaks and drops.

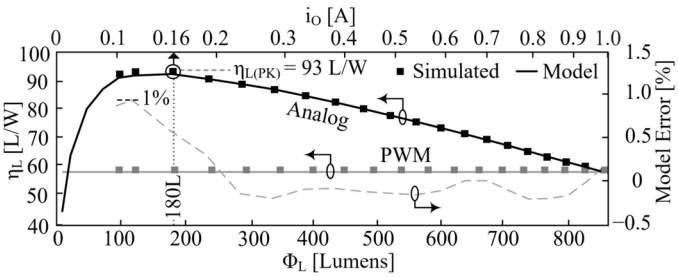

Fig. 9: Modeled and simulated luminous efficiency vs. luminous flux.

III. Duty-Cycled Dimmers

Duty-cycled or pulse-width modulated (PWM) dimming is another way to dim the LEDs. Unlike analog, PWM achieves dimming by duty-cycling a fixed i_O at frequency much lower

than SL's switching frequency f_{SW}. Typically, this duty-cycled frequency f_{PWM} is on the order of 0.1-1 kHz [3]–[4]. Based on how it is achieved, it can be categorized as shutdown and its modified versions, shunt- and series-switched.

A. Shutdown Operation

The simplest way to PWM-dim is by disabling the power-stage during PWM-OFF time $t_{PWM(OFF)}$ using an external dimming signal v_{DIM} [16]–[17]. This means opening M_{EI} and M_{EG} and draining the inductor via closed M_{DG} and M_{DO}. Exponentially decreasing i_O discharges C_O, turning the LEDs OFF as Fig. 10 shows. Note that primed variables are regulated non-dimmed currents and voltages.

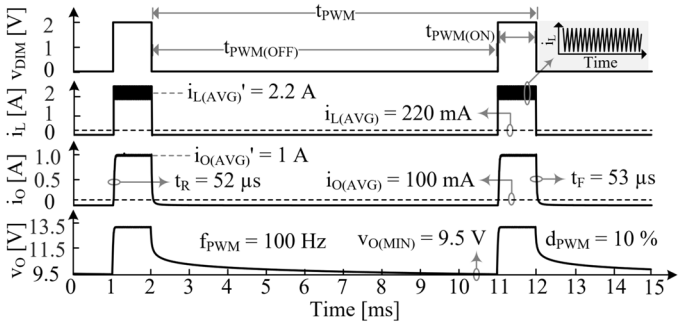

Fig. 10: Shutdown duty-cycled dimming operation.

The average output current is a PWM duty cycle d_{PWM} fraction of duty-cycled average i_O':

$$i_{O(AVG)} = d_{PWM} i_{O(AVG)}' = d_{PWM} d_D i_{L(AVG)}', \tag{9}$$

where i_L' is the regulated inductor current. The power stage is then enabled with v_{DIM}, charges C_O linearly and operates normally during PWM-ON time $t_{PWM(ON)}$.

Dimming Range: Dimming range for PWM is like analog in a way that it is defined as minimum to maximum luminous output. ϕ_L is proportionate to $i_{O(AVG)}$, which in PWM depends on minimum d_{PWM}:

$$d_{PWM} \geq \frac{t_R + t_F}{t_{PWM}}, \tag{10}$$

where t_R and t_F are the i_O rise and fall times respectively. t_{PWM} is the total period of the external PWM dimming signal v_{DIM}.

t_R and t_F consist of two components, inductor current slew t_L and output capacitor voltage slew t_C. When v_{DIM} turns on, SL switches and L_X slews to its regulation point i_L', a reverse d_D translation of i_O'. Following this, SL transfers energy to the output and charges C_O. Similarly, at $t_{PWM(OFF)}$ instance L_X de-energizes to zero, followed by C_O discharge. Both t_R and t_F are represented by:

$$t_{R/F} = t_L + t_C = \left(\frac{L_X}{v_L}\right)\left(\frac{i_O'}{d_D}\right) + \frac{C_O \Delta v_O}{i_{C(AVG)}}, \tag{11}$$

where v_L is the L_X voltage v_{IN} during energizing and v_O during the de-energizing phase and i_C is the charging or discharging C_O current. Δv_O is established from (7). Over t_R, average $i_{C(R)}$ is composed of the duty-cycled charging i_O' and discharging LED current i_O:

$$i_{C(R)(AVG)} = i_{O(AVG)}' - i_{O(R)(AVG)} \approx i_{L(AVG)}' d_D - \Delta i_{O(R)(AVG)}. \tag{12}$$

i_O is modeled as a straight line between 1-90% of average i_O' as shown in Fig. 11. During t_F, the $i_{C(F)}$ which is equivalent to i_O is exponentially modeled till i_O falls by 90%:

$$\begin{aligned} i_{C(F)(AVG)} &\approx i_{O(F)(AVG)} \\ &\approx \left(\frac{i_{O(AVG)}'}{2.3\tau}\right)\int_0^{2.3\tau} e^{-t/\tau} dt = i_{O(AVG)}'\left(\frac{1-e^{-2.3}}{2.3\tau}\right), \\ &= 39\% i_{O(AVG)}' \end{aligned} \tag{13}$$

where τ is the decaying time constant. Calculated t_R and t_F are over- and under-estimated as 58 µs and 43.6 µs which are within 18% of their simulated values. t_R's and t_F's inaccuracies systemically track and cancel each other. Consequently from (10) the minimum duty cycle is 1.05%, within 2% of simulations. Insightfully, larger C_O limits (dis-)charging rate and higher N_Ds increase Δv_O thereby increasing $t_{R/F}$ proportionately.

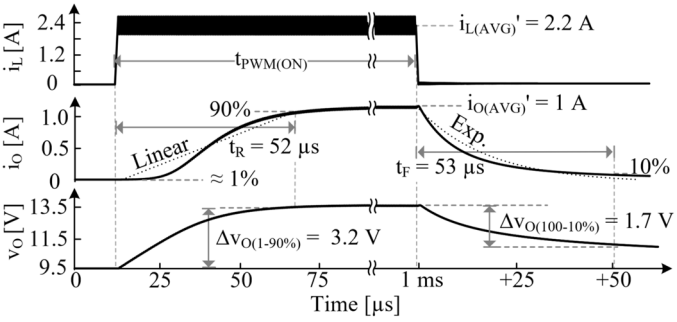

Fig. 11: $t_{R/F}$ approximations for shutdown.

Power-Loss Analysis: Power stage conversion efficiency loss P_{SL} is common to both analog and duty-cycled dimming. Since ϕ_L tends to saturate at higher i_Os (from Fig. 5), duty-cycled dimming suffers from additional PWM power loss ΔP_{PWM}:

$$\Delta P_{PWM} = P_{IN(PWM)} - P_{IN(A)} = P_{IN(A,PK)} d_{PWM} - P_{IN(A)}, \tag{14}$$

where $P_{IN(A,PK)}$ is the analog input power at peak i_O' (*i.e.*, 1 A). ΔP_{PWM} is zero at both i_O' extremes because analog and PWM dimming consume the same zero and peak P_{IN} as Fig. 12 shows.

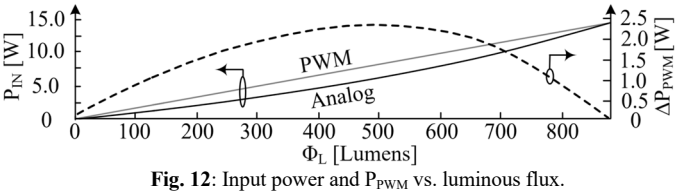

Fig. 12: Input power and P_{PWM} vs. luminous flux.

Because duty-cycled dimming has a fixed bias point at regulated i_O', the corresponding η_C is 90% throughout the dimming range as Fig. 7 shows. All power losses are summarized in Fig. 13. Analysis reveals that ΔP_{PWM} dominates SL's power losses in both analog and PWM during majority of the dimming range, highlighting its inefficiency.

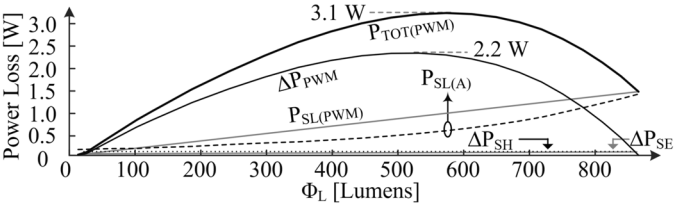

Fig. 13: Breakdown of power losses in analog and PWM dimming.

B. Shunt-Switched

Shunt-switched PWM dimming technique modifies shutdown by incorporating switch M_{PWM} in parallel to the LEDs as Fig. 14 shows. Closing M_{PWM} along with disabling SL discharges C_O to ground, therefore turning-off the LEDs. Similarly, at the PWM-ON instance M_{PWM} opens and SL charges C_O which resumes normal LED operation as shown in Fig. 15.

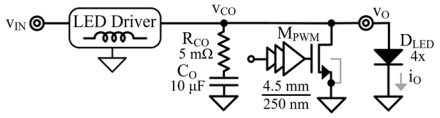

Fig. 14: SL LED driver for shunt-switched dimming.

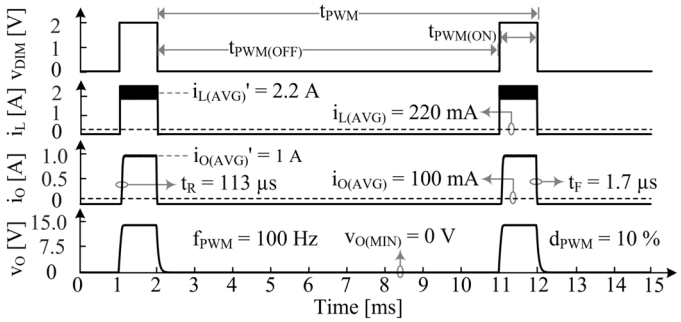

Fig. 15: Shunt-switched PWM operation.

Additional Power Losses: Since M_{PWM} eventually shunts C_O to ground SL needs to recharge C_O to its regulated v_O' during $t_{PWM(ON)}$, which repeats every PWM cycle. Therefore, leading to a capacitor energy P_C loss of:

$$P_C \approx \frac{1}{2} C_O \left(v_{O(AVG)}' \right)^2 f_{PWM} . \quad (15)$$

SL delivers remnant L_X power P_L to C_O while turning-OFF, which is eventually shunted and dumped to ground:

$$P_L \approx \frac{1}{2} L_X \left(i_{L(AVG)}' \right)^2 f_{PWM} . \quad (16)$$

Furthermore, closing M_{PWM} consumes gate-charge power P_G that v_{DD} supplies with charge q_G. q_G is the charge that overlap capacitance C_{OL} and channel capacitance C_{CH}, which constitute gate-drain and gate-source capacitances, need to close M_{PWM}:

$$P_G = v_{DD} \left(\frac{q_G}{t_{PWM}} \right) = v_{DD} q_G f_{PWM} , \quad (17)$$

$$q_G \approx C_{OL} \left(2 v_{DD} + v_O \right) + C_{CH} \left(v_{DD} + \frac{v_{TN}}{4} \right) . \quad (18)$$

These losses constitute the total additional power loss ΔP_{SH} in shunt-switched, which is miniscule as compared to the prominent P_{SL} and ΔP_{PWM} in Fig. 13. Fig. 16 depicts a breakdown of these additional losses. As shown, P_C overwhelms P_L and P_G and makes up the majority of ΔP_{SH}.

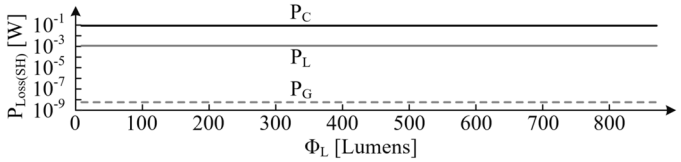

Fig. 16: Breakdown of power losses in shunt-switched PWM dimming.

Dimming Range: Like shutdown, $t_{R/F}$ determines the minimum dimming range in shunt-switched PWM. Opening M_{PWM} while switching SL pushes regulated i_L' to initially shunted C_O. LEDs conduct when C_O is sufficiently charged, *i.e.*, enough to allow $1\% i_O'$. t_R, therefore constitutes L_X's i_L (t_L) and C_O's v_O slew (t_C):

$$t_R = t_L + t_C \approx \frac{L_X}{v_L} \left(\frac{i_O'}{d_D} \right) + \frac{C_O \Delta v_{O(0\text{-}1\%)}}{i_{C(AVG)(0\text{-}1\%)}} + \frac{C_O \Delta v_{O(1\text{-}90\%)}}{i_{C(AVG)(1\text{-}90\%)}} . \quad (19)$$

v_O's slew is divided into two components, when i_O rises from 0-1%i_O' and 1-90%i_O' as Fig. 17 shows. That is, one where drain duty-cycled i_L' flows just to C_O and when it is shared with LEDs as i_O rises. The latter's $i_{C(AVG)}$ is approximated from (13). v_O's steep increase during the former causes d_D to vary from 100% to 55% as per (1), which averaged over this duration is 73%. $i_{C(AVG)(0\text{-}1\%)}$ is therefore $d_{D(AVG)} i_{L(AVG)}'$.

M_{PWM} closes in saturation because v_O (v_{DS}) is higher than a v_{TN} subtracted from v_{DD} (v_{GS}). Ten times i_O' discharges C_O and hence steers current away from LEDs. M_{PWM}'s parameters W_N and L_N that support $10 i_O'$ can therefore be designed accordingly:

$$i_{C(F)} \approx i_{PWM(SAT)} \equiv 10 i_{O(AVG)}' = \frac{1}{2} K_N' \left(\frac{W_N}{L_N} \right) \left(v_{DD} - v_{TN} \right)^2 . \quad (20)$$

Consequently, t_F is the time in which $10 i_O'$ discharges C_O by $\Delta v_{O(F)}$ to when i_O falls by 90%:

$$t_F \approx \frac{C_O \Delta v_{O(100\text{-}10\%)}}{i_{C(F)}} . \quad (21)$$

Calculated t_R and t_F are 118 µs and 1.65 µs which are within 8% and 3% of simulations. This puts dimming range of 1.15% within 4% of its simulations.

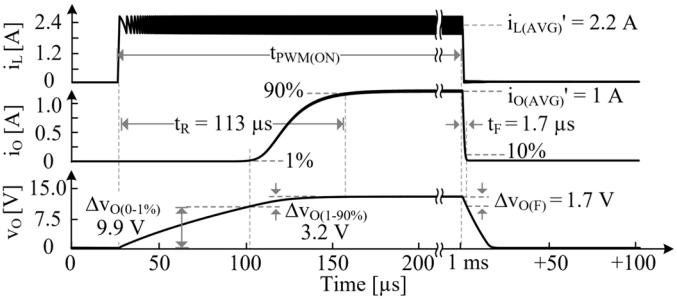

Fig. 17: $t_{R/F}$ for shunt-switched PWM.

C. Series-Switched

Series-switched PWM dimming is another modification to SL shutdown [18]. In addition to the power stage shutdown, series-connected PMOS M_{PWM} switches i_O with v_{DIM} as shown in Figs. 18 and 19.

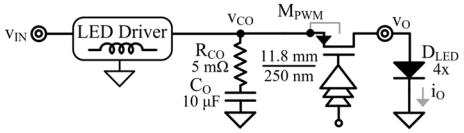

Fig. 18: SL LED driver for series-switched dimming.

At PWM-ON instance, SL switches to energize L_X to its i_L'. Followed by an energizing L_X slew delay t_{PRE}, M_{PWM} connects SL to the LED load:

$$t_{PRE} \approx \left(\frac{L_X}{v_{IN}} \right) i_{L(AVG)}' . \quad (22)$$

This SL pre-charge mechanism [19] in-tandem with C_O's v_{CO} preservation (discussed later) during $t_{PWM(OFF)}$ allows instantaneous LED current rise. Like shunt-switched, SL is disabled when M_{PWM} disconnects, which limits C_O overcharge.

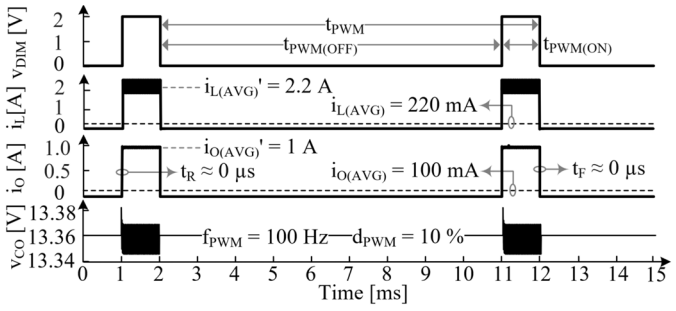

Fig. 19: Series-switched PWM operation.

Additional Power Losses: SL delivers remnant L_X power P_L to C_O while turning-OFF which can lead to an overcurrent spike at the $t_{PWM(ON)}$ instance, stressing the LEDs and other output-connected circuitry. A solution is to maintain output capacitor voltage v_{CO} during $t_{PWM(OFF)}$. Variations of this concept have been implemented in modern LED drivers [18]–[24]. Maintaining v_O implies excess P_L in (16) is disregarded. Additionally, M_{PWM}'s ohmic loss $P_{R(SW)}$ contributes to the overall ΔP_{SE} loss, *i.e.*,

$$P_{R(SW)} = \left(i_{O(AVG)}'\right)^2 R_{PWM} d_{PWM}, \tag{23}$$

$$R_{PWM} \equiv R_{CH} = \frac{1}{K_P'\left(\frac{W_P}{L_P}\right)\left(v_{DD} - \left|v_{TP}\right|\right)}. \tag{24}$$

For a typical 100 mΩ resistance $P_{R(SW)}$ is 100 mW at peak i_O' of 1 A. An inductor power loss P_L of 1.1 mW and gate charge loss P_G of 14.9 nW are further lost as per (17)-(18) as Fig. 20 shows.

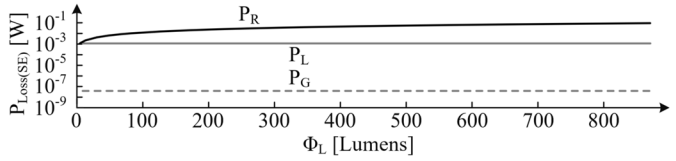

Fig. 20: Breakdown of power losses in series-switched PWM dimming.

Dimming Range: M_{PWM} instantaneously connects SL power stage to the LEDs as soon as L_X slews to its regulation point. Larger C_O reduces Δv_{CO} because of L_X energy transfer during this connection instance. Therefore limiting Δi_O such that peak i_O is always within 10%i_O' as Fig. 21 shows. Eventually, switching dynamics of M_{PWM} determine the t_R and t_F, which can be as low as a few nanoseconds providing a dimming capability of up to 0% for a 100 Hz dimming signal.

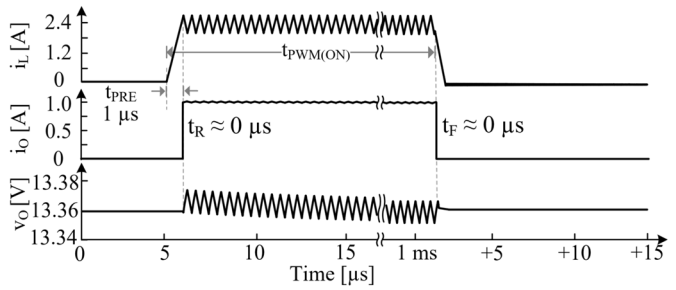

Fig. 21: $t_{R/F}$ for series-switched PWM.

D. Luminous Efficiency

Since luminous output and drawn P_{IN} are the same duty-cycled fraction of the peak biasing point i_O', η_L is constant across the dimming range as Fig. 9 shows. Furthermore, PWM dimming draws more power for the same amount of light as Fig. 12 shows reducing its luminous efficiency. Revealing that analog dimming is up to 57% more efficient over PWM.

IV. Discussion

Table I provides an overview and compares analog and duty-cycled dimming techniques. Analog dimming yields the highest η_L, up to 57% more, over most of the luminous range as Fig. 9 shows. However, at low loads when SL losses outpace power delivered, $\eta_{L(PWM)}$ overtakes. Hybrid dimming approaches where LED driver can modulate i_O' during PWM have been proposed to improve PWM η_L but it complicates control and requires additional current channels [9]–[10], [25]. Therefore, reducing its popularity.

Although analog dimming technique theoretically promises up to 0% dimming, in practice it's a function of i_O or i_L sensing accuracy, noise and offsets, which can be improved by design [12], [26]. Furthermore, it also depends on LED's luminous characteristics. That is, if they can emit light at low enough i_Os.

Shutdown dimming technique is often used in buck SLs where large C_Os are not needed to supply i_O during t_E [27]–[29]. Therefore, reducing its $t_{R/F}$ and improving the dimming range. In boost SLs, L_X's DC-short and body-diode conduction of M_{DO} eventually forces v_O to v_{IN} when shutdown. However, since typical boost SL's v_O is 2-4x when operational [18], [20] and because of LEDs exponential I-V relationship i_O is negligible.

Shunt- and series-switched PWM dimming can also be extended to buck and boost SL topologies as Figs. 22(a)-(d) show. Dimming in boost using series-switched as depicted in Fig. 22(a) operates in the exact same way as buck-boost. However, grounding S_{PWM} during shunt-switched PWM would undesirably energize L_X via body-diode D_{DO} as Fig. 22(b) depicts. Directly shunting to v_{IN} instead of ground counters this.

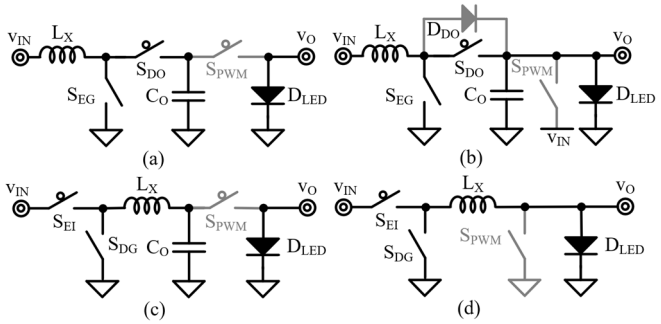

Fig. 22: Buck and boost implementations of series- and shunt-switched PWM.

Buck topologies operate like their boost-based counterparts when series-switched as shown in Fig. 22(c). C_O absorbs additional P_L when S_{PWM} reconnects, limiting Δv_{CO} and Δi_O. Contrary to buck-boost, bucks need not shutdown when shunt-switched [30]–[31]. This is because they can de-energize to ground when S_{PWM} closes in Fig. 22(d). Not shutting SL also improves their dimming capabilities since L_X need not slew when SL restarts. However, this costs additional S_{PWM}'s ohmic and SL's switching and ohmic power during $t_{PWM(OFF)}$.

TABLE I. Comparison

Parameter	Analog	Duty-cycled (PWM)		
		Shutdown	Shunt-SW	Series-SW
η_L	45-93 L/W	59 L/W		
Space	—	Same as Analog	Additional M_{PWM}	
i_O's $t_R + t_F$	N/A	≤ 100 µs	≤ 120 µs	≤ 10 ns
Dim. Range	0-100%	1-100%	1.2-100%	≈ 0-100%
SL η_C Loss	0.18-1.4 W	≤ 1.4 W		
ΔPWM Loss	No loss	≤ 2.2 W		
Add. Losses	N/A		$P_C + P_L + P_G$	$P_R + P_L + P_G$
References	[12]–[13]	[17]	[30]–[31]	[18]–[24]

v_{IN} = 12 V, N_D = 4, $v_O \approx$ 13.3 V, $f_{SW(CCM)}$ = 2 MHz, v_{DD} = 2 V, L_X = 4.7 µH, C_O = 10 µF, f_{PWM} = 100 Hz, K_N' = 200 µA/V^2, K_P' = 100 µA/V^2, $|v_{TN/P}|$ = 0.4 V

V. Conclusions

This paper reviews, analyses and assesses analog and duty-cycled (PWM) dimming techniques and its variations in DC–DC SL LED drivers. An example of buck-boost power-stage has been demonstrated which is 2% accurate for ϕ_L, P_{IN} and η_L and 5% accurate for the dimming range when validated against SPICE simulations. Overall, analog dimming outperforms PWM in power losses, majority of η_L and achieves 0-100% dimming range matching its best PWM dimming counterpart, emerging as the best-in-class.

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