A Lossless, Accurate, Self-Calibrating Current-Sensing Technique for DC–DC Converters

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***Abstract*— High-performance, state-of-the-art applications demand smart power supplies to be adaptive, power efficient, and reliably accurate, which is why monitoring inductor current flow in a lossless fashion is not only desirable but also critical for protection and feedback control. Filter-based lossless current-sensing technique use a tuned filter across the inductor to estimate current flow, and its accuracy is dependent on the inductance and equivalent series resistance (ESR) of the device. Because of process-related tolerances, errors as high as ±28% are reported, even when the nominal inductor value is known, which is not the case for the IC designer, whose errors will then grossly exceed this value. A technique is proposed to boost the accuracy of these current-sensing filters by automatically adjusting their bandwidth and gain via phase and gain feedback control loops. The proposed scheme essentially measures the inductance and ESR values during startup and power-on reset events. Because the filter is automatically tuned to the inductor, the current during normal operation can be measured accurately by simply sensing the voltage across the inductor. A PCB prototype implementation of the proposed technique achieved overall dc and ac gain errors of 2.3% and 5% at full load, respectively, when lossless, state-of-the-art schemes achieve 20-40% error.**

***Index Terns*— power management, switching regulators, dc-dc converters, current sensing, lossless, gm-C filter.**

I. INTRODUCTION

Current-sensing circuits are one of the more critical and essential building blocks used for control and protection of switching power supplies, i.e., dc-dc converters. Every switching regulator includes an over-current detection circuit, which protects the system against over-current events. What is more, the sensed inductor current is a prolific source of information for the operating state of the system, which is exploited in current-mode controllers and especially so in multi-phase converters [1-3], not to mention a growing number of dynamically adaptive supplies where the operating region is dependant on the load current for enhanced power efficiency performance [2, 4].

The conventional and simple series sense resistor incurs unacceptable power losses, unfortunately. Since current flow in dc-dc converters is high (e.g., in the order of amperes), even small resistors cause significant losses, severely reducing the overall power efficiency of the system (e.g., by 2-10%). And reducing the series resistance (e.g., 1mΩ for 1A) is prohibitive because the detection accuracy is overwhelmed by noise and offsets, which is why the series resistor technique is unacceptable in today's high-performance converters, such as those used in portable applications where more than 90% efficiency is required over the entire load-current range [5].

A handful of lossless current-sensing techniques are available but their accuracies are significantly lower than the traditional sense resistor scheme [6]. The MOSFET R_{on} [7], current-sensing FET (sense-FET) [7-13], and filter [7, 14] schemes are among the more popular techniques (Table 1). The MOSFET R_{on} technique, for instance, estimates the current from the drain-source voltage of a MOSFET switch and its accuracy therefore hinges on the on-resistance value of the MOSFET, which varies significantly with temperature, process, and supply voltage (e.g., 50-200%). In the case of the sense-FET technique, a mirror transistor is used to source a fraction of the switch current, and its accuracy relies on the matching performance of the current mirror, whose mirroring ratio is in the order of 1,000 and its operating region is in triode (i.e., ohmic/non-saturated). Although accuracies of ±4% are reported [13], the mismatch and process variations cause errors as large as ±20% (3σ spreads), a result of the high device size spread between the sense-FET and the power-FET in the mirror [15]. Moreover, the sense-FET technique is only practical if power switches are implemented on-chip, or if specially matched MOSFETs are available. Also, given the switching nature of these devices and their inherent switching noise (both in the MOSFET R_{on} and sense-FET techniques), their use in switching feedback control applications is limited.

The filter technique, which measures the inductor current by applying a low-pass filter across the inductor, is inherently less susceptible to switching noise and is therefore better suited for current-mode controllers with high switching frequencies [7, 14]. Nevertheless, its accuracy is dependent on the inductance and matching a filter to it is critical. Even when the inductance is known and the filter is well matched, component tolerances and operating point variations can cause up to ±28% error (±15% initial inductor tolerance, ±11% ESR variance, and a temperature range of 70°C) [14]. In practice, lower accuracies are expected to occur in wide temperature range applications (e.g., commercial range for power supply chips is from -10 to 125 °C).

Table 1. Summary of state-of-the-art lossless current-sensing techniques.

Method	Description	Disadvantages
MOS R_{on}	Sense the power MOSFET's drain-source voltage.	- Low accuracy - Discontinuous and noisy
Sense-FET	Mirror a fraction of the load current with a small sense MOSFET.	- Low-accuracy - Only feasible for on-chip switches - Discontinuous and noisy
Filter	Low-pass filter the inductor voltage.	- Only for off-chip applications - Low accuracy (dependence on inductance)

The accuracy of lossless current-sensing techniques degrades if an integrated circuit (IC) current-sensing solution is required for use in dc-dc controller applications. Theoretically, lossless current-sensing circuits must only sense voltages because sensing current implies additional series devices and therefore further power losses. Estimating the current flowing through an already existing device from only voltages requires knowledge of the device impedance (i.e., series resistance, inductance, and capacitance). For a switching power supply, the inherent series path elements are the inductor, output capacitor, and power switches, which are normally off-chip and are selected by the end user, not the IC designer. Therefore, the IC designer is not cognizant of these off-chip components during the IC design cycle. Consequently, for any lossless current-sensing technique to be accurate, the circuit should somehow measure one of the current-carrying elements in its path and sense the voltage across the same (i.e., Ohm's law: I=V/R), which is the driving force behind the proposed current-sensing technique.

II. Proposed System

The proposed technique overcomes the accuracy limitations of lossless techniques by automatically measuring the off-chip component values during startup. The acquired information is used to adjust the sensing circuit to estimate the current accurately during regular operation. The filter technique is adopted because of its high power efficiency, low susceptibility to switching noise, and compatibility with high switching frequency applications.

The block diagram of the reported filter technique is shown in Fig. 1 [7, 14], which is vastly used in industry. If an equivalent filter is designed to match the series impedance of the inductor and its equivalent series resistor (ESR) and the same voltage is applied to its inputs, the replica filter's output mimics the current flowing through the inductor. From Fig. 1, sense voltage (V_{sense}) and inductor current (I_L) are low-pass filter versions of inductor voltage:

$$V_{sense} = g_{m1}R_2\left(\frac{1}{1+sR_2C}\right)V_L \qquad (1)$$

and

$$I_L = \frac{1}{R_L + sL}V_L, \qquad (2)$$

where V_L is the voltage across inductor, L is the inductance, R_L is the inductor's ESR, C is the filter capacitor, R_2 is filter resistor, and g_{m1} is the transconductance of the G_m-C filter. If R_2 is tuned to ensure L/R_L equals R_2C, the current-sensing filter output is directly proportional to inductor current I_L,

$$V_{sense} = (g_{m1}R_2)R_L I_L. \qquad (3)$$

Additionally, if $(g_{m1}R_2)R_L$ is 1Ω, the estimated current is

$$V_{sense} = I_L. \qquad (4)$$

In Equation 1, varying R_2 changes the cutoff frequency while adjusting g_{m1} modulates the filter gain, which are the automatic adjustments proposed in this paper.

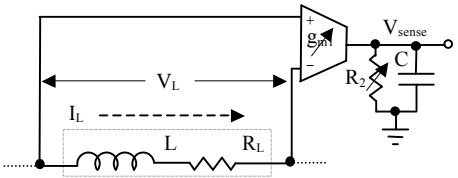

Fig. 1. Block diagram of Current-sensing filter technique.

The accuracy of the filter technique, in its basic form, is low because of its dependence to inductance. The filter is therefore designed separately for each application, using off-chip capacitors and resistors [7, 14], since the inductor specifications are determined by the end user, not the IC designer. Moreover, the inductor and filter component tolerances and temperature variations reduce the accuracy of the system to approximately ±28%, even for special application where the nominal value of the inductor is known [14].

The proposed system introduces *tuning* and *calibration* procedures during the startup and power-on reset events of dc-dc converters to automatically adjust the filter gain and bandwidth and consequently enhance the current-sensing accuracy of the system (Fig. 2). During the tuning operation, the low-pass filter's cutoff frequency is adjusted via a feedback loop, until it matches the power inductor's cutoff frequency, which is R_L/L ($f_c=R_L/L$). Then, during calibration, the gain of the low-pass filter is adjusted against a reference resistor until the test current matches the predicted value (Equation 4). When tuning and calibration are completed, the low-pass filter is set and ready to project accurate estimates of the inductor current (i.e., $R_2C=L/R_L$ and $g_{m1}R_2=1\Omega$).

During each power-on reset, at first, tuning and calibration circuits are activated to adjust the current-sensing filter parameters, and the switching supply is kept disabled. Once the proper tuning and calibration parameters are set, they are stored and the dc-dc converter is then allowed to start-up and operate normally. Since the tuning and calibration circuits are only active during startup, they incur no power losses during regular operation.

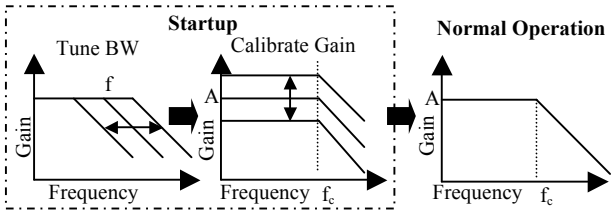

Fig. 2. Proposed start-up sequence: tuning, calibration, and normal operation.

Fig. 3 shows how the proposed scheme is applied to a buck dc-dc converter. During startup, switches M_1 and M_2 are off, and switches M_a and M_b are on. Therefore, test current I_{test} flows entirely through the inductor, which makes the measurement of inductor characteristics possible by measuring the voltage across it. Since the test current is just a fraction of the main current (in this case, $I_{loadmax}/20$) switches M_a and M_b do not require a large area. During normal operation, switches M_a and M_b are turned off and the current-sensing filter resumes its normal operation. The current-

sensing filter and proposed tuning and calibration circuits are described in Section III.

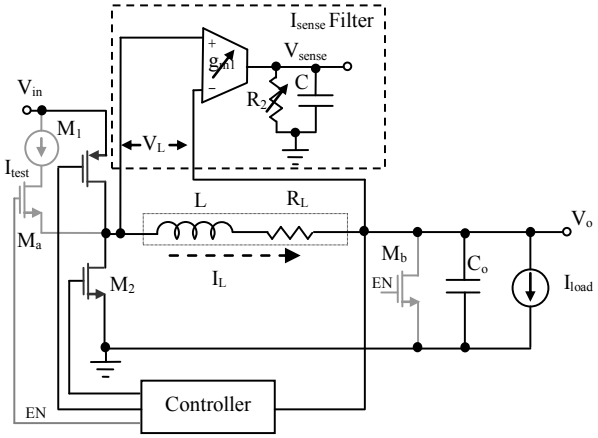

Fig. 3. Adapting the proposed technique to a buck dc-dc converter.

III. Proposed Circuit

A. Current-Sensing Filter

The current-sensing filter is implemented with a g_m-C circuit (Fig. 4). Transconductance cell g_{m2} is used in a shunt feedback configuration to realize the variable loading resistor R_2 (Figs. 1 and 3) and buffer Op1 isolates the loading effects of the g_{m2}-R circuit (Fig. 4) on g_{m1}. Intersil®'s CA3280 g_m cells were used since their transconductances are externally adjustable via their bias current. The differential pair-based g_m cells have good linearity but only for a limited differential voltage range (±50mV), which is why a resistor divider network with a ratio of 1/820 was used to increase the range for which the cells are linear (0.15% linear over a ± 3.3V range). The linearity of the g_m cell is important to prevent systematic offsets in the system, which is discussed in more detail in Section IV. The resistor divider, unfortunately, increases the effective input-referred offset of the g_m cells by a factor equal to the divider ratio (i.e., by 820, in this case). Other feedback linearization schemes can be employed when designing the circuits at die level (IC), but their feasibility in a discrete-level design is limited.

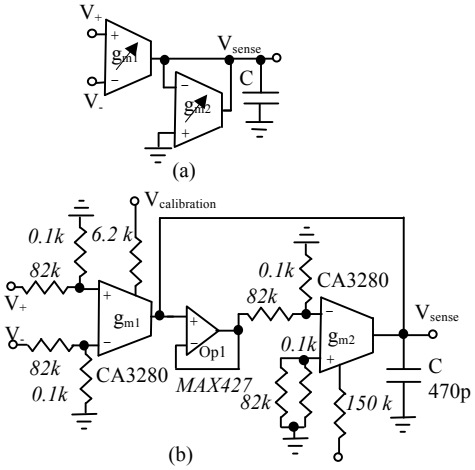

Fig. 4. G_m-C filter design: (a) basic concept and (b) detailed circuit.

B. Start-up Hardware Implementation

1. Tuning the Circuit

In the tuning phase, the low-pass filter's cutoff frequency is adjusted via a phase-mixed feedback control loop, until it matches the power inductor's cutoff frequency (i.e., $f_c=R_L/L$). A sinusoidal voltage signal at frequency f_{ref} forces a sinusoidal current into the inductor, since reference resistor R_{ref} (100Ω) is much greater than the inductor's equivalent series resistor R_L, which is approximately 45mΩ, and the current through R_{ref} is therefore linearly proportional to the voltage signal (Fig 5). The tuning operation is not sensitive to signal frequency f_{ref} and it can range from 100Hz to 1kHz because the circuit will simply use it as a reference phase signal. A low-offset amplifier (MAX427: V_{os} is less than 15μV) is then used to amplify the voltage across the inductor. This amplified voltage (V_3) has a phase lead of $\tan^{-1}(2\pi f_{ref}L/R_L)$ with respect to the reference sinusoidal signal because of inductor behavior. The g_m-C filter then introduces a phase lag of $\tan^{-1}(2\pi f_{ref}C/g_{m2})$, producing a total phase shift of

$$\text{Phase}(V_{sense}) = \text{Tan}^{-1}(2\pi f_{ref}L/R_L) - \text{Tan}^{-1}(2\pi f_{ref}C/g_{m2}). \quad (5)$$

The phase detection process is performed by converting the sinusoidal input and output signals to square waves (V_{1s} and V_4) and synchronizing their rising edges. A frequency divider slows down V_4 and generates the *clock* signal for the circuit. V_{1s} is then sampled at the rising edge of the clock signal via a flip flop. The output of the flip flop is one, if the current-sensing output leads the input test signal; otherwise, it is zero. At the onset of the tuning operation, the counter, which controls the tuning voltage, is reset to g_{m2}(min) and the output of flip flop is one, which starts the count. The bias current of g_{m2} is gradually increased as the counter counts up, consequently raising g_{m2}, until the phase difference is eliminated, at which point the counter stops and g_{m2} is set:

$$\text{Tan}^{-1}(2\pi f_{ref}L/R_L) \approx \text{Tan}^{-1}(2\pi f_{ref}C/g_{m2}) \quad (6)$$

or

$$L/R_L \approx C/g_{m2}. \quad (7)$$

Fig. 6 illustrates the phase response of V_{sense} and V_1 for various g_{m2} values, and how their difference is eliminated once a proper value for g_{m2} is reached.

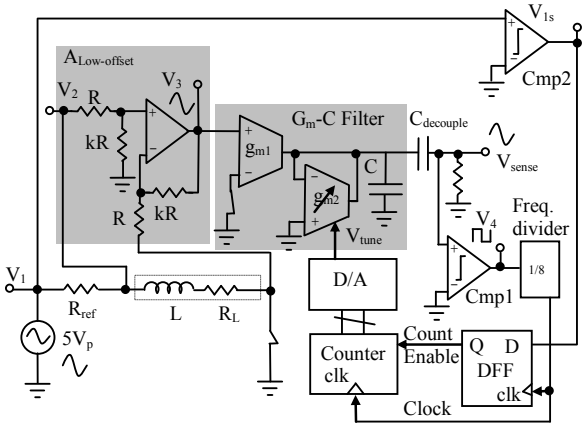

Fig. 5. Tuning circuit.

The counter *clock* frequency (Fig 5) should be several times lower than the sinusoidal reference frequency to allow the circuit to reach its steady-state operation after each new bias current setting, as the bias current is incremented by the counter. For reliability and robustness, a clock frequency of $f_{ref}/8$ was used, which, theoretically, allows the system to reach 99.96% of its steady-state value before the onset of the following clock signal (i.e., after eight time constants).

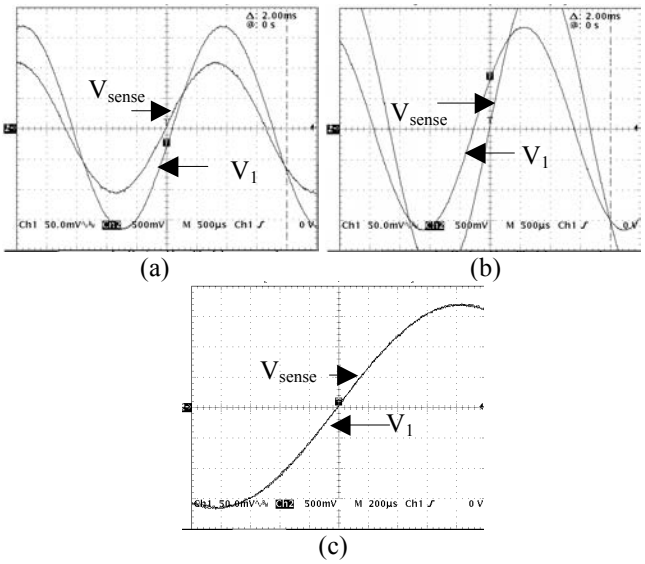

Fig. 6. Output V_{sense} versus reference V_1 phase response at f_{ref}=300Hz with (a) maximum, (b) minimum, and (c) tuned g_{m2} values.

Decoupling capacitor $C_{decouple}$ is used to filter out the dc part of the signal, thereby canceling the offset effects associated with the g_m cells. The phase lag incurred by the low-offset amplifier should be negligible, which implies that the bandwidth of the amplifier must be greater than the frequency of the tuning reference signal (e.g., $f_{3dB\text{-}amp}$ is greater than $50f_{ref}$ for a 1° phase error). Frequencies f_{ref} and $f_{3dB\text{-}amp}$ are therefore selected to be 300 Hz and 15 kHz, respectively. For a constant gain of 20V/V, this results in a unity-gain-bandwidth product of 300 kHz for the amplifier, which is feasible. Depending on the number of bits used for tuning, a few hundred milli seconds may be required for the tuning operation to be completed. A successive binary search, instead of the implemented linear search, would substantially reduce the time required to tune the circuit.

2. Calibration Phase

In the calibration phase (Fig. 7.a), the gain of the low-pass filter is adjusted against the current running through a reference resistor. A constant reference voltage forces a constant dc current through the inductor, assuming R_{ref} is much greater than R_L (See II.B.1). A low-offset amplifier (the same amplifier used in the tuning phase) amplifies the voltage across the inductor and, after resetting the counter, g_{m1} is adjusted with each count, from its minimum to its maximum value, while holding g_{m2} constant, which keeps the bandwidth constant. The counter stops when V_{sense} reaches reference target voltage V_C, resulting in

$$V_C = I_{ref} R_L k \frac{g_{m1}}{g_{m2}}; \quad (8)$$

therefore, the estimated current during normal operation is

$$V_{sense} = I_L R_L \frac{g_{m1}}{g_{m2}} = I_L \frac{V_C}{kI_{ref}}. \quad (9)$$

If constant $V_c/(kI_{ref})$ is defined to be 1, the current-sensing gain is 1Ω, as in Equation (4).

The problem, as stated in subsection II.A, is the offset introduced by the resistor dividers, which were used for linearization. If the g_m-cell bias currents were constant, the offset would also have been constant and easily eliminated. However, the input-referred offset of the g_m-cell varies with its bias current since the offset of a differential stage is proportional to its transconductance. Thus, an offset cancellation technique is required during the calibration period for accurate operation. The effects of variable offsets can be eliminated in the tuning phase by using a large decoupling capacitor. The same fix cannot be used during the calibration because the information needed is in the dc part of the signal.

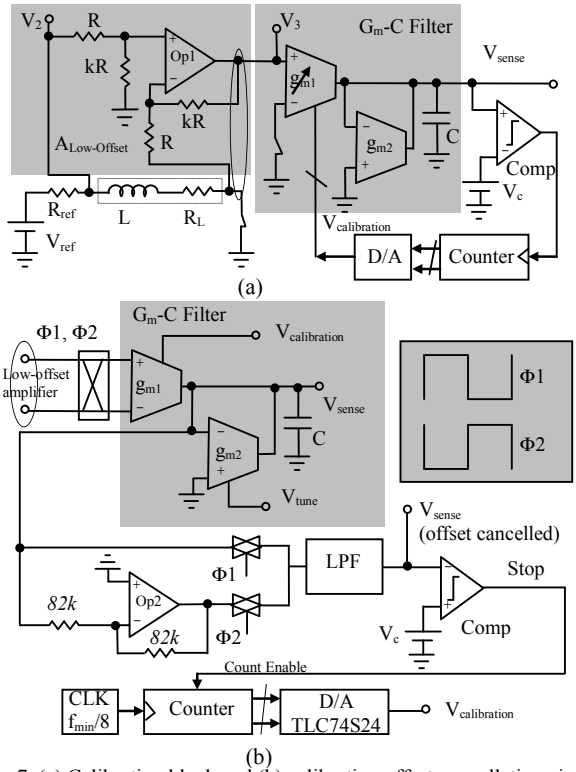

Fig. 7. (a) Calibration block and (b) calibration offset-cancellation circuit.

Therefore, a chopper-stabilized offset-cancellation [16] technique was adapted for the calibration phase (Fig. 7.b). Another amplifier (Op2) is added to the circuit to generate an inverting output voltage. During phase Φ1, the output of the g_m-C filter is $A(V_{in}+V_{os})$, where V_{in} is the input voltage, V_{os} is the input-referred offset voltage, and A is the gain from the input to the output of the g_m-C filter. During phase Φ2, the g_m-C filter output is $A(V_{in}-V_{os})$. Hence, if a low-pass filter is used at the output of the g_m-C filter, the average output is AV_{in}, which has no offset errors.

IV. EXPERIMENTAL RESULTS

A prototype implementation of the system was designed using discrete components and experimental results verified the effectiveness of the proposed concept. A 20μH inductor with 45mΩ of ESR was used and a desired current-sensing gain was set to 0.5Ω (i.e., $I_L=V_{sense}/0.5\Omega$). The system was tuned and calibrated, first, by using the discussed tuning and calibration algorithms and normal operation was then tested.

The family of curves for the measured dc currents versus the actual dc values is shown in Fig. 8. Filter gain was varied by adjusting g_{m1} bias current, and the estimated current (filter output) for current loads from 0-1A were measured for various filter gains. The thick bold line is the targeted 0.5V/A gain and the thin bold trace is the experimental result for calibrated g_{m1} for 0.5V/A gain. The calibrated curve follows the targeted trace from 0-0.1A. Then, it slightly separates from ideal curve as current rises from 0.1A to 0.2A. The difference between the calibrated and targeted curves becomes a constant offset change (about 18mV) for the remaining 0.2-1A range where 0.2A current corresponds to the boundary of the buck converter's continuous- and discontinuous-conduction modes (CCM and DCM). This effect is a systematic offset caused by the nonlinearity of the g_m cells.

The systematic offset essentially results because of the common-mode range dependence of the transconductance of the g_m cells. The signal at the g_m-C filter input during normal operation is rectangular by nature - for a buck converter operating in CCM, the voltage at the junction of the power switches is V_{in} when the high-side switch is on and zero when the low-side switch is on. The voltage at the output of converter, on the other hand, is V_{out} and is approximately constant because the output ripple voltage is significantly smaller. Therefore, the common-mode range of the filter is wide enough to cause transconductance errors to occur, which ultimately distorts output sense voltage V_{sense}. Changing g_{m1} from g_{m1} to $g_{m1}+\Delta g_{m1}$ when the input voltage changes from zero to V_{in} changes the output sense voltage by

$$V_{systematicoffset} = \Delta g_{m1}\left(\frac{1}{g_{m2}}\right)D(V_{in} - V_o) \qquad (10)$$

or equivalently

$$V_{systematicoffset} = \left(\frac{\Delta g_{m1}}{g_{m1}}\right)\left(\frac{g_{m1}}{g_{m2}}\right)D(V_{in} - V_o), \qquad (11)$$

where D is duty cycle. The systematic offset is considerable if the gain (g_{m1}/g_{m2}) and nonlinearity ($\Delta g_{m1}/g_{m1}$) are high. For the case of the prototype, where g_{m1}/g_{m2} is 12.5, V_{in} is 5V, V_{out} is 3.3V, D is 66%, and $\Delta g_{m1}/g_{m1}$ is 0.15% for the resistor division factor of 820, Equation (10) predicts 21mV of offset, which is close to the experimental value of 18mV. Cells with higher linearity can be designed to limit the systematic offset to a minimum value, but at the cost of more complex g_m cells. For DCM buck converter operation (e.g., current below 0.2A in Fig. 8), a lower systematic offset occurs because the oscillations at the positive inductor port during the high-side switch "on" time [2]. Therefore, the dc accuracy is function of both gain error resulted from calibration loop limitations and systematic offset error due to gm-cell non-linearity. Although, the total error is the sum of gain error and systematic offset errors, the systematic offset error is not inherent and can be eliminated using higher performance circuits. In Fig 8, the measured current gain calibrated for 0.5V/A gain (thinner bold trace) has 10% gain error from 0 to 0.2A and 2.3% gain error from 0.2A-1A. The total error, including systematic offset error, is 21% at 0.2A and 7.7% at 1A.

A continuous real-time measurement of the inductor current is another important goal of the proposed technique. The experimental continuous output ripple current response of the circuit matches the actual ripple current with an ac error of less than 5%, as shown in Fig. 9. The actual inductor current was derived from the output ripple voltage, since output capacitor relatively large ESR (0.15Ω) mostly defines the ripple voltage across it, which is then linearly proportional to the inductor ripple current. The reference current can also be measured using a relatively high series sense resistor (e.g., 0.1Ω - the traditional current-sensing method).

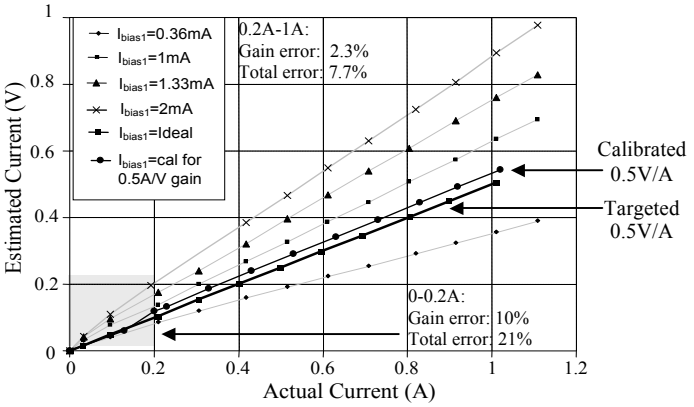

Fig. 8. Experimental family of curves of the estimated current as g_{m1} is changed. The thick bold trace is the targeted 0.5V/A gain and the thin bold trace is the calibrated gain.

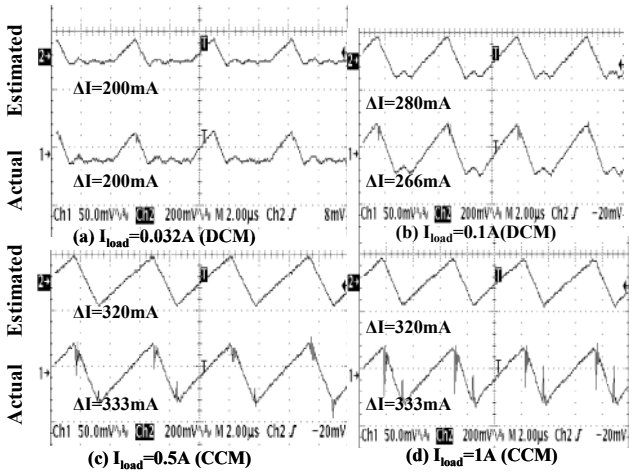

Fig. 9. Estimated and actual ac inductor currents during normal operation and under various loading conditions.

V. Discussion

The proposed technique increases the accuracy of the filter-measuring technique by essentially ascertaining the value of the inductor and its ESR during a start-up and power-on reset phase. As a result, the circuit adjusts itself to whatever loading condition (i.e., inductor/ESR combination) is established, thereby eliminating component tolerance errors. The proposed technique is also IC compatible since all the corresponding circuits can be integrated on chip.

Inductance and ESR values may drift from their initially measured state because of current and temperature variations, which is why the tuning and calibration process should be performed during each power-on reset cycle. However, if power-on reset events are not periodic, errors will occur in this technique and all others that rely on these values. The effects of various operating conditions on the accuracy of filter technique are discussed in detail in [14], which found the variations of ESR with temperature to be the only significant errors. The inductor ESR's temperature coefficient (TC) is approximately 3900ppm/°C (copper's TC). As a result, using equation (3), a ±50°C temperature change causes ±20% error. Fortunately, this error is systematic and can be nulled or compensated in applications requiring high operating temperature ranges. The idea is simply to make the bias current of the g_{m2} cell a linear function of temperature. The design of a circuit to compensate for this error is currently under investigation.

VI. Conclusion

A lossless and accurate current-sensing technique compatible for switching dc-dc converters that is insensitive to the values of the inductors selected by end users was presented and experimentally verified. The technique basically measures the inductance and ESR values during start-up and power-on reset events by tuning the gain and bandwidth of the g_m-C to the filter response of the L-ESR inductor, i.e., by measuring the L and ESR. As a result, the circuit adjusts itself to whatever L-ESR combination exists and the corresponding errors of component tolerances are therefore eliminated. As a result, a power-efficient current-sensing technique with less than 10% gain error is achieved. The proposed technique can be fully integrated because all of its building blocks are IC compatible, even when off-chip switches are used. Even though the circuit solution shown was implemented in a switching buck converter, the technique extends to most, if not all, inductor-based switching regulator topologies, such as boost and buck-boost converters.

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