Self-Stabilizing, Integrated, Hysteretic Boost DC–DC Converter

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Abstract: In portable, battery-powered applications, integration of switching dc-dc converters is crucial to reap maximum benefits in size, cost, and design ease. The frequency compensation circuit, whose design varies with off-chip, passive filter (L-C) components, forms a critical hurdle to obtaining a fully integrated solution. Surveying state-of-the-art control techniques in literature, hysteretic control in buck converters, which in a single loop, controls inductor current ripple indirectly while regulating the output voltage, is observed to be the simplest, fastest, and needing no compensation circuit, thus being best suitable for integration. However, the technique is not readily applied to boost converters. This paper proposes a novel technique to harness voltage-mode hysteretic control in boost converters by controlling inductor current and output voltage through separate loops. The proposed circuit designed for V_{IN}=1.2 V (nom), V_{OUT}=3.3 V ± 5%, I_{OUT}=0.1 to 1 A shows excellent voltage regulation and transient response (±150 mV), without the use of any compensation circuit.

I. INTRODUCTION

In low power, battery-operated, portable applications, like cell phones, PDAs, digital cameras, etc., an integrated dc-dc converter circuit solution offers several advantages in terms of cost, size, and design complexity. A critical hurdle in obtaining a fully integrated solution is the frequency compensation circuit, which has to be designed based on the values of external passive filter components (L-C) and associated parasitic elements, like the capacitor equivalent series resistance (ESR). The values of these off-chip components vary due to manufacturing tolerances, parameter drift, and, more significantly, various design requirements. Capacitor ESR, besides being loosely specified, can vary by orders of magnitude, based on whether the capacitor is electrolytic or ceramic, not to mention its variation across temperature. The dependence of dynamic performance on external parameters limits the application of control ICs to converters using L-C values specified within a narrow design range. As such, a DC-DC controller IC, which can provide adequate control and stable operation with widely varying passive component values, is not only desired, but also required.

In voltage-mode hysteretic control [5-8] for buck converters, the regulated output voltage includes inductor current ripple information indirectly through capacitor ESR, thus simplifying the loop characteristics. This circuit displays an inherently stable performance, irrespective of passive filter components. Any change in L-C values is accommodated through a change in the converter switching frequency, maintaining stable operation without the use of frequency compensation circuits. However, in boost converters, which are widely used in portables for stepping up single or dual cell battery voltages for 3.3 V or 5 V applications, the technique is not readily applicable because the inductor current and output voltage ripples are out of phase. The purpose of this paper is to propose a novel circuit and control technique that overcomes this inherent limitation and incorporates voltage-mode hysteretic control in boost converters.

The rest of the paper is organized as follows. Section II briefly discusses the benefits and disadvantages of various techniques studied in the literature, targeted at alleviating or eliminating the effects of L-C filter components as related to specific issues in the converter performance. Section III provides a comparative evaluation of the studied techniques. Section IV describes the proposed method in detail and shows circuit simulation results. Finally, section V summarizes the key conclusions in the paper.

II. BACKGROUND STUDY

Control techniques reported in the literature, which attempt to mitigate the effects of L-C filter components and related parasitics on dc-dc converter operation, control loop and compensation requirements, are briefly discussed below.

A. Masking the Effect of Capacitor ESR Zero [1, 2]

The effect of output capacitor ESR on converter performance is reduced or eliminated by the addition of a feedforward path (FF) from the input of the L-C filter to the error amplifier (EA), as shown in Fig. 1(a).

The net low frequency gain is determined by the main path (KG_PY_1) because its gain is much larger as shown in Fig. 1(b). At frequencies higher than z_{FF}, the feedforward gain (KA_{FF}) dominates. The resulting zero (z_{FF}) thus introduced by the feedforward path ensures a crossover frequency and phase margin independent of ESR zero (z_{ESR}). The main drawback of this technique is increased high frequency output impedance, because beyond z_{FF}, output voltage is determined by the feedforward gain and shunt feedback is no longer present at V_O.
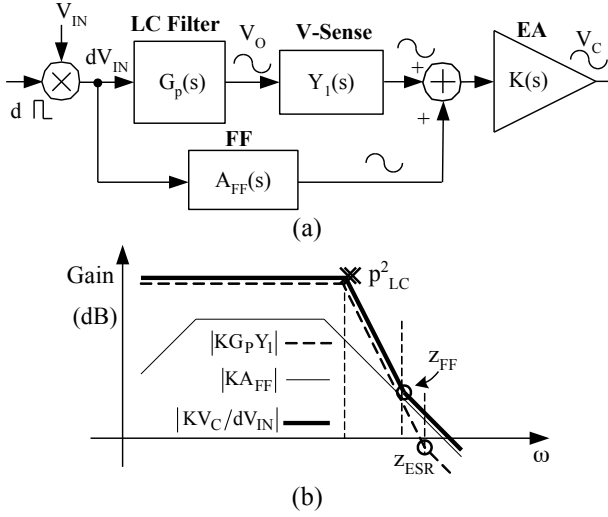
Fig. 1. Voltage mode buck converter with feedforward.

Elegant Embodiment of Feedforward Control [3-4]: The circuit for this implementation is shown in Fig. 2. In a buck converter with hysteretic control [5-8], the variation of switching frequency with capacitor ESR is eliminated by the addition of a feedforward signal from the input of the L-C filter to the hysteretic comparator. The combination R_F-C_F gives a triangular signal larger than the output ripple thereby determining the feedforward control and establishing the switching frequency irrespective of the capacitor ESR.

B. Elimination of the RHP Zero in Boost/Buck-Boost Converters

In boost and buck-boost converters, the capacitor discharging time increases (V_O initially decreases) with an increase in duty cycle, as a result of an RHP zero in the control loop gain, the location of which depends on the values of inductor L and load resistance R [20]. Two reported techniques that remove the RHP zero are discussed below.

I. Constant Capacitor Discharge Control [10, 11]: The RHP zero is eliminated by keeping the total capacitor discharging time constant. As shown in Fig. 3, when the auxiliary switch S_{AUX} is turned on for a portion of the off time of the main switch S_M, the inductor current freewheels, letting the capacitor C discharge through the load. Thus, an additional discharging time is introduced. The total capacitor discharge time, which is the sum of on times of switches S_M and S_{AUX}, is kept constant by
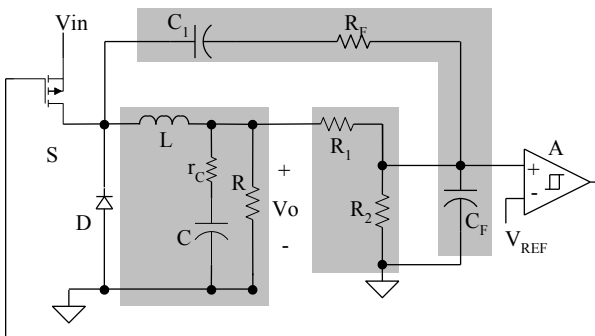

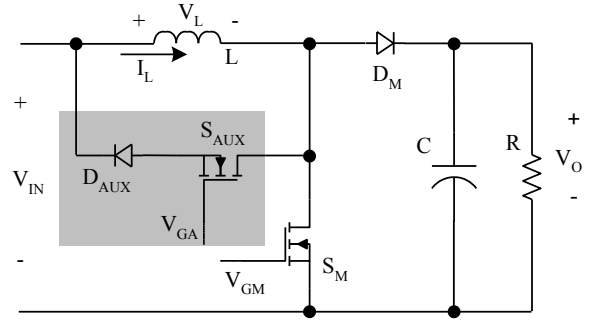Fig. 2. Hysteretic control with modified sensing.

Fig. 3. Boost circuit with auxiliary switch.

modulating the on time of switch S_{AUX} to match changes in the on-time (duty cycle) of switch S_M. The extra freewheeling period leads to a higher average inductor current, causing an increase in switching and conduction losses, which is a drawback of this technique.

II. Peak Output Voltage Detection [12]: The output voltage of a boost DC-DC converter, including output capacitor ESR ripple, is shown in Fig. 4. If the capacitor ESR is sufficiently high, then the peak output voltage (point E) does not exhibit RHP zero, as does the trough (point D). In that case, the peak voltage is fed back rather than the average value, eliminating the adverse effects of the RHP zero in control loop gain. However, an impractically large ESR value is required for the method to be effective. Additionally, in order to feed back *instantaneous* output voltage, the feedback loop must have high bandwidth, making the system more susceptible to noise.

C. Compensating for L-C Filter Variations

I. Constant LCR Load [13-15]: From Fig. 5, the control signal to the converter power stage is generated by adding a *separate weighted error signal* to the error amplifier output, which itself is based on preset nominal values of LCR filter elements.
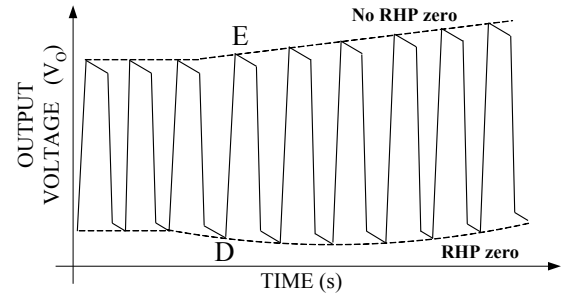
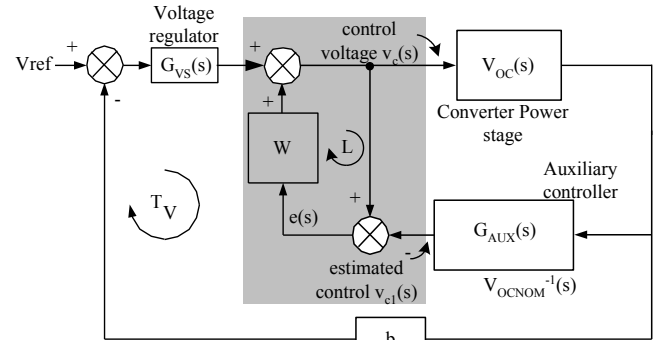

Fig. 4. Boost converter output voltage transient.

Fig. 5. Schematic of constant LCR control.

Any variation of the actual LCR values from the preset ones is accommodated only by modulating the weighted error signal such that error amplifier output is invariant to LCR variations. The error signal is obtained as the difference between the actual converter control signal and the control signal that would be required if the LCR values equaled the preset ones. The drawbacks of this technique are circuit complexity and potential introduction of additional instabilities in boost and buck-boost type converters, because of the RHP zero in these converters.

II. Multiple Operating Points [16-18]: Typical DC-DC converter control is based on the small-signal linearization around the operating point. For large-signal variations, this proves inaccurate. Grid point control tackles the issue by partitioning the total operation space into different regions, each characterized by a single operating point called grid point. Each grid point and its respective control equations are designed independently to yield optimal performance. The disadvantage of this technique is that system stability during changeover between grid spaces is intricate and complex.

III. Digital: Digital control, which provides adaptive control and system-level power management capabilities, takes multiple clock cycles to process information thereby limiting its ability to respond quickly. Hence, despite its advantages in terms of versatility, transient response is poor [19] as compared to typical averaged analog control techniques and hysteretic control.

III. COMPARATIVE EVALUATION

Table I shows a qualitative comparison of the studied techniques based on various criteria, like system complexity, transient response, power losses, magnitude of output ripple (accuracy), stability in a variable LCR environment, and versatility of application to various converter topologies. Schemes (2) and (3), based on averaged feedback control though effective in eliminating the RHP zero and the adverse effects of L-C variations respectively, are complex, inefficient, and/or slow. On the other hand, voltage-mode hysteretic control as applied to buck converters is fast, simple, and impervious to L-C variations, thus being most suitable for IC implementation. However, the technique is less versatile and has yet to be a solution for boost and buck-boost converters.

IV. PROPOSED TECHNIQUE

Hysteretic control can be readily applied in buck converters, where the output voltage has to be regulated to a value between the input voltage V_{IN}, which is the equilibrium output voltage with switch closed, and zero, which is the equilibrium output voltage with switch held open. An intermediate voltage $(0 \leq V_{OUT} \leq V_{IN})$ between the two extremes can be obtained by regulating the switch duty cycle between one and zero. However, in a boost converter, the output voltage needs to be regulated at a value higher than its equilibrium values with the switch open and closed $(V_{OUT} \geq V_{IN})$. Hence, hysteretic control cannot be achieved by monitoring the output voltage alone.

The proposed technique, the circuit for which is shown in Fig. 6, solves the problem by adding an auxiliary switch S_A across the inductor L. The average inductor current I_L is raised above the minimum value required to support load current I_O. The excess inductor current tends to charge the capacitor C beyond the desired output voltage. This is prevented by the turn-on of switch S_A, which enables the inductor current to freewheel shutting diode D off and letting the capacitor voltage discharge. The hysteretic problem is thus defined to regulate the output voltage to a desired value between zero, which is its equilibrium value with switch S_A closed, and $I_D(V_{OUT}/I_O)$, which is its equilibrium value with switch S_A open. This regulation is performed by controlling the duty cycle D_A of switch S_A. At the appropriate duty cycle D_A, the diode current I_D, *averaged over a switching cycle of S_A*, equals the load current I_O, and average V_{OUT} is stabilized to equal V_{REF}. Inductor current I_L is independently regulated through a separate hysteretic loop, containing the main switch S_M.

The fallout of higher inductor current is an increase in conduction power loss. The additional loss is kept low by maintaining the inductor current only 5% above the minimum required value ($I_{L\ (MIN)}$). This is achieved by deriving a representative inductor current reference (V_{IREF}) from duty cycle D_A, by means of a charge-pump-based duty-cycle-to-voltage demodulator in Fig. 7. Capacitor C_1 is charged and discharged by complementary switching current sources I_1 and I_2, which are gated by the controlling signal of switch S_A. The average capacitor current equals zero and the voltage V_{IREF} stabilizes when the total charge injected into capacitor by I_1 during the off time of switch S_A balances the total charge removed by I_2 during the on time of switch S_A. By choosing I_2 to be 19 times larger than I_1, V_{IREF} reaches steady state only when the off time of S_A (I_1 charging C_1) is 19 times greater than the on time of S_A (I_2 discharging C_1) i.e., duty cycle D_A is 5%.
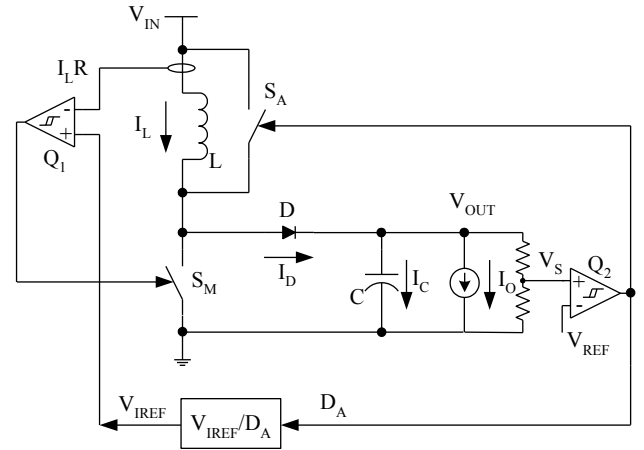

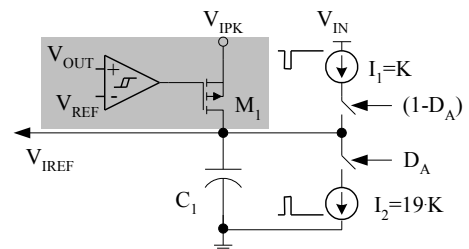Fig. 6. Simplified schematic of proposed system.

Fig. 7. Duty cycle D_A to V_{IREF} demodulator.

Table I. Comparison of stabilization techniques studied

| Characteristic | Masking LCR (and/or ESR) Parameters | | | RHP Zero Elimination | | Adaptive control | | Boundary control |
	Feedforward	Modified Hysteretic	Constant LCR load	Constant capacitor discharge	Output peak control	Multiple operating point	Digital control	Voltage hysteretic control
Complexity	Medium	Low	Highest	Medium	Medium	High	High	**Lowest**
Response	Slowest	Fast	Medium	Medium	Slow	Slow	Slow	**Fastest**
Power losses	**Low**	Medium	**Low**	Highest	**Low**	**Low**	**Low**	**Low**
Output ripple	Low	**Lowest**	Low	Low	High	Low	Low	Low
Stable – LCR variation	Medium	**Highest**	High	Low	Lowest	High	High	High
Versatility	**Highest**	Medium	Low	Low	Low	High	High	Medium

A fast, large increase in load current causes the output voltage to drop sharply because the inductor current is not high enough to support the increased load. The comparator in Fig. 7 senses this voltage drop and turns on switch M_1, thereby raising the inductor current reference to the level required to support the maximum designed load current. The inductor current rises, in a single cycle of switch S_M, to the new reference and then charges the output capacitor, in a single cycle of switch S_A, to V_{REF}. Once the output voltage reaches V_{REF}, switch M_1 turns off and the inductor current reference V_{IREF} decays until the duty-cycle D_A reaches the 5% limit. The comparator is designed with an asymmetrical hysteresis, being narrower than that of Q_2 (Fig. 6) on the positive side and wider than that of Q_2 on the negative side.

Inductor current can be sensed in a variety of ways as described in [19]. Resistive sensing, though the simplest technique, adds additional I^2R power losses to the system. Lossless techniques, like R_{DS} sensing or the one proposed in [19], are feasible alternatives at the expense of accuracy and/or design simplicity.

A. DC Analysis

Steady-state analysis of the proposed circuit can be performed using capacitor charge balance. When switch S_A is open, the converter operates as a standard boost converter, and the average diode current is given by

$$I_D = I_O + I_C = I_L(1-D_M) , \qquad (1)$$

where D_M is the duty cycle of switch S_M. When switch S_A is closed, the diode current I_D is zero and the capacitor C supplies I_O. Then, the diode current, averaged over a switching cycle of S_A, is given by

$$I_D(avg) = I_O = I_L(1-D_M)(1-D_A) . \qquad (2)$$

Thus, for a given load current I_O, the average inductor current is given by

$$I_L(avg) = \frac{I_O}{(1-D_M)(1-D_A)} . \qquad (3)$$

For a standard boost converter, switch S_A is absent; hence D_A reduces to zero in equations (2) and (3) giving,

$$I_{L(MIN)} = \frac{I_O}{(1-D_M)} . \qquad (4)$$

In the proposed converter, D_A is set to 5%, thereby increasing the average inductor current by approximately 5%. Note that functionally, the on time of switch S_A is a portion of the off time of switch S_M. In practice, care must be exercised to ensure that the on-times of S_A and S_M do not overlap. Therefore, dead time must be added between the switching instants of switches S_A and S_M.

B. Design of L-C filter parameters

Hysteretic regulation of the output voltage is based on the requirement that the inductor current be regulated, as seen by the voltage loop. For this to be true, the current control loop must have a higher bandwidth than that of the voltage loop. In hysteretic control, the unity-gain bandwidth is at the switching frequency of the switch element in the loop [7]. Therefore, the switching frequency of switch S_M must be higher than that of switch S_A. The on time of switch S_M is

$$t_{ON} = \frac{H_I}{(di/dt)_{ON}(R_S)} = \frac{H_I L}{V_{IN} R_S} , \qquad (5)$$

where H_I is the hysteretic band in volts for the comparator in the current loop and R_S is the current-sensing resistor. The magnitude of output voltage ripple during t_{ON} is

$$\Delta V_O = t_{ON}\left(\frac{dV}{dt}\right)_{ON} = \frac{H_I L}{V_{IN} R_S}\left(\frac{I_O}{C}\right). \qquad (6)$$

To satisfy the bandwidth requirement,

$$\Delta V_O = \frac{H_I L}{V_{IN} R_S}\left(\frac{I_O}{C}\right) \leq \frac{H_V}{M} , \qquad (7)$$

where H_V is the hysteretic band for the comparator in the voltage loop and M is the voltage divider ratio at the output. Inequality (7) is simplified using ideal boost converter relations [20] to

$$C \geq \frac{H_I}{H_V} \text{x} \frac{I_O M L}{V_O R_S (1-D_M)} (= C_{MIN}). \qquad (8)$$

Inequality (8) gives the absolute minimum value of capacitor C for a given designed value of inductor L. In practice, the value typically used is much higher than C_{MIN} to satisfy load transient response requirements. For example, under the set of conditions in Table II, the value of C_{MIN} is 7 µF.

C. *Simulations and discussion*

The proposed circuit was designed and simulated under the set of conditions summarized in Table II. Fig. 8(a) shows the steady-state waveforms of the output voltage, inductor current, the gate voltage of switch S_A, and the reference voltage for the sensed inductor current. The average output voltage of 3.297 V has a small, high frequency ripple during the off time of switch S_A, corresponding to switching of S_M, superimposed on a low frequency ripple of ±35 mV corresponding to the switching of S_A. Similarly, the inductor current has a high frequency ripple of ±250 mA superimposed on a low frequency ripple of ±50 mA, the latter being a reflection of the voltage ripple on V_{IREF}. The recorded switching frequencies (1.6 MHz for S_M and 7.4 kHz for S_A) easily satisfy the conditions as required for inequality (7). Fig. 8(b) shows the freewheeling (switch S_A on) and switching (switch S_A off) periods of the inductor current.

Transient response of the simulated circuit, for a load step of 0.3 to 0.6 A in 10 ns, is shown in Fig. 9. The inductor current rises in a single step to about 3.4 A, which is slightly larger than the 3.2 A required to support a full load current of 1 A. Decay in the inductor current is also observed, once the output voltage reaches 3.3 V.

The simulated efficiency of the proposed solution was compared to that of a standard boost converter with the same operating conditions and parameters, but without the auxiliary switch (Fig. 10). Since the drop in efficiency is due to higher I^2R loss related to the inductor current, efficiency degrades up to approximately 2.5 % from that of a standard boost converter at 1 A load. Generally, higher inductor current also leads to increased losses in the input source resistance [21]. High load currents are therefore undesirable and usually avoided when the voltage transfer ratio is large, thereby keeping the inductor current close to the load current. At low loads (at or below 100 mA), however, where efficiency is crucial in portable applications, the proposed circuit has simulated efficiency within 1% of the standard boost solution.

Table II. Converter parameters and operating conditions.

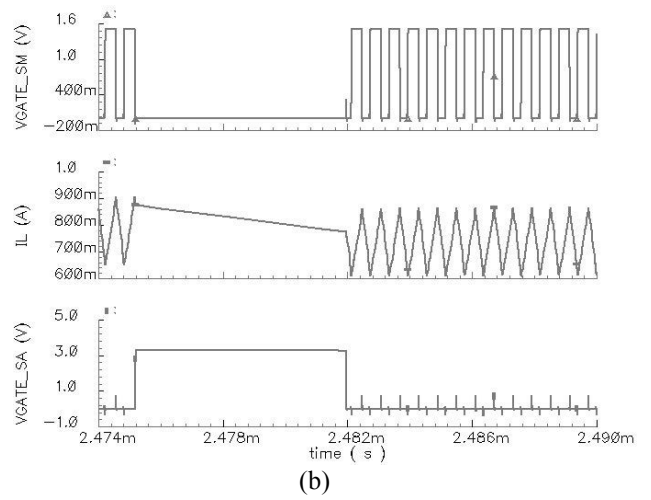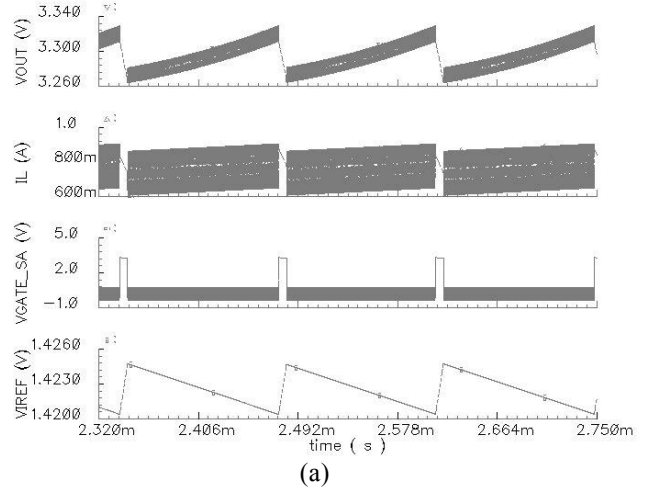| Parameter	Value	Parameter	Value
V_{IN}	1-1.5 V	V_O	3.3±5%
I_O	0.1-1 A	L	2 μH
C	44 μF	ESR_C	20mΩ
S_M (N-ch) R_{ON}	0.1 Ω	S_A (N-ch) R_{ON}	0.1 Ω
D (P-ch) R_{ON}	0.15 Ω	I_1	1 μA
I_2	19 μA	C_1	10 nF
V_{OUT} H_V	36 mV	I_L hysteresis H_I	40 mV
M	0.364	R_S	0.1 Ω
Simulator	Spectre-S	Technology	0.5μ CMOS

(a)

(b)

Fig. 8. Steady state waveforms for the proposed circuit at V_{IN}=1.5 V, I_O=0.3 A, V_{OUT}=3.3 V, f_{SW} (S_A) =7.4 kHz, $f_{SW}(S_M)$ =1.6 MHz showing (a) three switching cycles of switch S_A and (b) detailed view in one cycle of switch S_A.
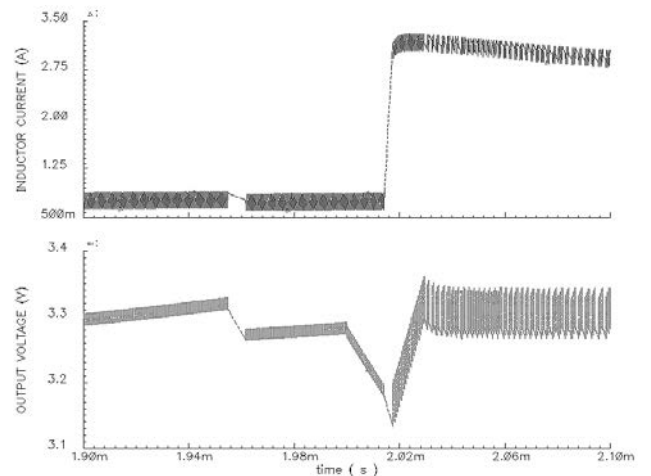

Fig. 9. Transient waveforms: step load 0.3 to 0.6 A, V_{IN}=1.5 V, V_{OUT} = 3.3 V.
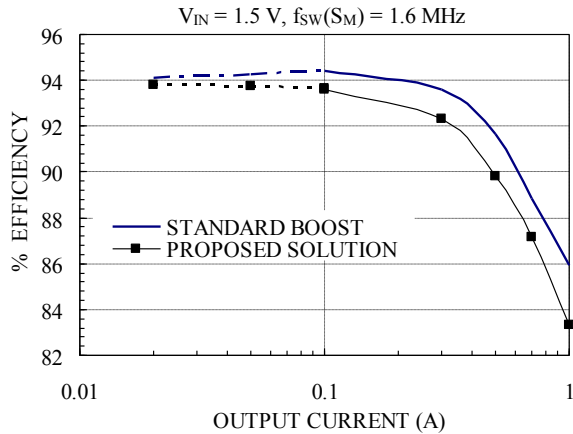
Fig. 10. Efficiency comparison for standard boost converter and the proposed solution.

V. CONCLUSION

State-of-the-art techniques reported in literature for improving the stability of switching DC-DC converters were reviewed and evaluated. Hysteretic control in buck converters, which in regulating the output voltage also indirectly controls the inductor current ripple, is simple and fast, requiring no compensation circuit. A novel technique was presented to harness these advantages of voltage mode hysteretic control in boost converters, again by hysteretically regulating both the output voltage and inductor current, albeit through separate control loops. System level simulations for a boost DC-DC converter designed for V_{IN} = 1-1.5 V, V_{OUT} = 3.3 V ± 5%, and I_{OUT} = 0.1 to 1 A, with the proposed technique showed that the circuit met design specifications without the need of any compensation circuit. The efficiency was slightly degraded at high loads (1.5% from standard boost at 0.5 A load) because of increased inductor current, but this effect was kept small by maintaining the inductor current nominally 5% above the minimum required value. With this choice, reduction in efficiency for low loads, which is critical in battery-powered applications because of higher probability of operation at low loads, was within 1% of a standard boost converter. The technique thus provides a fully integrable (except L-C) boost DC-DC converter solution, most suited for compact, low cost, low power, portable applications.

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