# Understanding and Quantifying $i_{DS}$-$v_{DS}$ Overlap Losses in Switched-Inductor Power Supplies

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***Abstract*—IV-overlap power losses play an important role in the overall conversion efficiency of a switched-inductor power supply, which is why a clear understanding of its mechanism is necessary. This paper proposes an insightful model with device-based expressions. The model accounts for the non-linear and dynamic behavior of gate capacitances in switching MOSFETs and reverse-recovery effects produced by interconnected diodes, which are largely absent in the state of the art. Calculated and simulated overlap losses with and without reverse recovery are within ±10%.**

***Index Terms*—Switched inductor, power MOSFETs, power converter, DC–DC power supply, switching IV-overlap loss, CMOS.**

## I. CMOS Power Supplies

CMOS power supplies, such as switched inductor voltage regulators, are widely integrated in electronic devices used in a broad range of applications. Power-conversion efficiency $\eta_C$ is the fraction of input power $P_{IN}$ that the input $v_{IN}$ delivers to the output $v_O$ in Fig. 1. $P_{IN}$ also supplies power losses $P_{LOSS}$, for instance $P_{IV}$. So $P_O$ outputs the difference $P_{IN}$ – $P_{IV}$, fractional loss $k_{IV}$ is the fraction of $P_{IN}$ lost in $P_{IV}$, and $\eta_C$ is below 100% by the amount $k_{IV}$ sets.

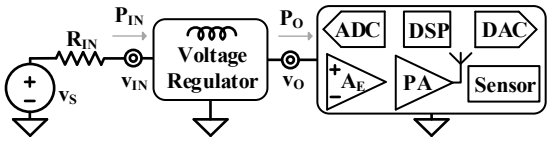


**Fig. 1**. Electronic system with power supply and load.

IV overlap loss $P_{IV}$ is due to the internal switching mechanisms of MOSFETs, when both drain source voltage $v_{DS}$ and channel current $i_{DS}$ are not zero during a short amount of time, leading to an overlap loss. It is composed of 2 terms: a voltage term $P_V$ when $v_{DS}$ is switching, and a current term $P_I$ when $i_{DS}$ is rising or decreasing [1]. $P_{IV}$ is directly proportional to output current $i_O$. Therefore, it climbs with $i_O$, and become increasingly more significant.

A good estimation of efficiency would be to fall below 0.5% of simulated results, that is why achieving 0.1% error in fractional loss estimation is desirable. Majority of state of the art papers falls within 20% of experimental or simulated results [2]—[7]. Moreover, state of the art models for $P_{IV}$ rely on empirical data-based expressions that IC designers cannot use [2], [3], [5], [8], [9]. Besides, a few of the models proposed do not consider dynamic gate capacitances [7], [10], [11], while others do not consider reverse recovery effect [12]–[15]. The contribution of this paper is a model which relies on insightful device-based expressions, that IC designers can use. Besides, the theory derived in this paper matches simulated results within 10%, which is better than the state of the art. Section II describes the gate capacitances model, while Section III, IV and V covers how $P_{IV}$ differs in the following three situations: when the switch is closed, open, and closed considering reverse recovery effect. Section VI presents an example with an asynchronous boost voltage regulator, and Section VII concludes the paper.

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## II. Gate Capacitances

### A. Composition

A cross section of an NMOS can been seen below on Fig. 2. The oxide defines capacitance per unit area $C_{OX}$", which defines, with gate and channel dimensions, the channel capacitance $C_{CH}$ and overlap capacitance $C_{OL}$:

$$C_{CH} = C_{OX}"W_{CH}(L_{CH} - 2L_{OL}). \quad (1)$$

$$C_{OL} = C_{OX}"W_{CH}L_{OL}. \quad (2)$$

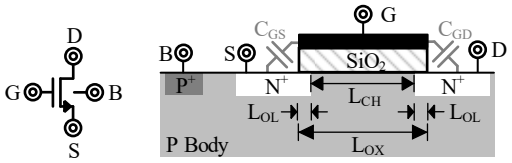



**Fig. 2**. N-channel MOSFET.

MOSFETs parasitic capacitances playing a key role in $P_{IV}$ mechanism are the gate source capacitance $C_{GS}$ and the gate drain capacitance $C_{GD}$. Both $C_{GS}$ and $C_{GD}$ include one $C_{OL}$ and share $C_{CH}$ as channel forms and pinches.

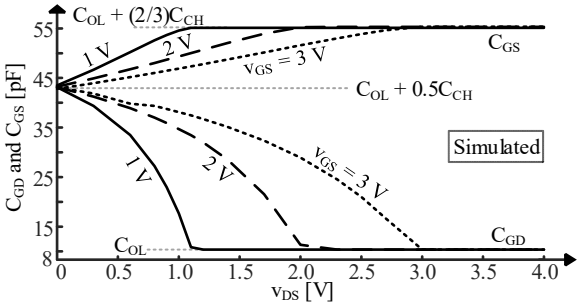



**Fig. 3**. Gate capacitances.

### B. $v_{DS}$ Model

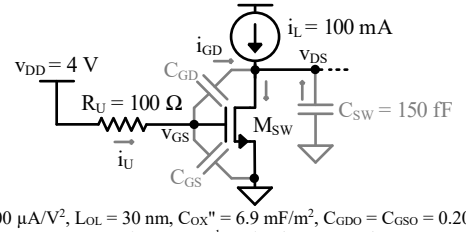
Figure 3 shows the evolution of the fraction of $C_{CH}$ that $C_{GS}$ and $C_{GD}$ share as the transistor goes from triode to saturation.

$C_{GS}$'s and $C_{GD}$'s $0.5C_{CH}$ scales with $v_{DS}$. Both $C_{GS}$ and $C_{GD}$ initially carry $0.5C_{CH}$ in triode. As the transistor enters saturation, $C_{GD}$'s $C_{CH}$ fraction progressively decreases to reach 0 in triode. $C_{GS}$'s $C_{CH}$ fraction progressively increases to reach $(2/3)C_{CH}$ in saturation [16].

## III. Closing MOSFET

### A. Power

$i_{DS}$ and $v_{DS}$ transitions occur quickly. Therefore, a boost voltage regulator circuit can be simplified by approximating the inductor to a constant current source, as shown below in Fig. 4. The NMOS ground switch $M_{SW}$ is closed by a driver with a pull-up resistance $R_U$.




$K_N' = 200\ \mu A/V^2$, $L_{OL} = 30$ nm, $C_{OX}'' = 6.9$ mF/m$^2$, $C_{GDO} = C_{GSO} = 0.207$ nF/m, $V_{T0} = 0.4$ V, $\lambda = 0.05$ m$^{-1}$, and W/L = 50 mm/250 nm.

**Fig. 4**. Simplified schematic for closing a switch.

When closing $M_{SW}$, $v_{GS}$ and later $i_{DS}$ climb as $R_U$ charges $C_{GS}$ and $C_{GD}$. $v_{DS}$ falls when $i_{DS}$ is high enough to sink $i_L$ plus the charge $C_{GD}$ and other capacitances $C_{SW}$ need to decrease $v_{DS}$, as shown in Fig. 5:

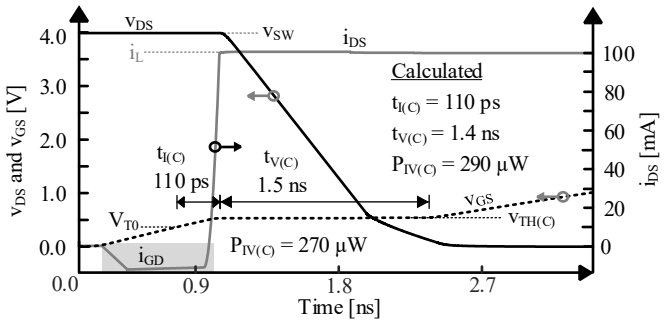



**Fig. 5.** Simulated waveforms for closing a switch.

When $i_{DS}$ rises, $v_{DS}$ stays at $v_{SW}$. As $M_{SW}$ is in inversion, $i_{DS}$ scales with $v_{GS}^2$, so $i_{DS}$ averages about a third of $i_L$ across $t_{I(C)}$. $M_{SW}$ burns a power $P_{I(C)}$ across $t_{I(C)}$:

$$P_{I(C)} = \frac{1}{t_{I(C)}}\int_0^{t_{I(C)}} i_{DS}v_{DS}dt = \left(\frac{1}{t_{I(C)}}\int_0^{t_{I(C)}} i_{DS}dt\right)v_{SW}$$
$$= \left[\frac{1}{t_{I(C)}}\int_0^{t_{I(C)}}\left(\frac{i_L}{t_{I(C)}^2}\right)t^2\,dt\right]v_{SW} \approx \left(\frac{i_L}{3}\right)v_{SW}. \quad (3)$$

When $v_{DS}$ starts to drop, $i_{DS}$ already reached $i_L$. As $v_{DS}$ drops linearly, $v_{DS}$ averages about a half of $v_{SW}$ across $t_{V(C)}$. $M_{SW}$ burns $P_{V(C)}$ across $t_{V(C)}$:

$$P_{V(C)} = \frac{1}{t_{V(C)}}\int_0^{t_{V(C)}} i_{DS}v_{DS}dt$$
$$\approx i_L\left(\frac{1}{t_{V(C)}}\int_0^{t_{V(C)}} v_{DS}dt\right) \approx i_L\left(\frac{v_{SW}}{2}\right). \quad (4)$$

Total overlap loss $P_{IV(C)}$ burned by $M_{SW}$ during closing is simply the sum of $P_{I(C)}$ and $P_{V(C)}$ averaged over the switching period $t_{SW}$:

$$P_{IV(C)} = P_{I(C)}\left(\frac{t_{I(C)}}{t_{SW}}\right) + P_{V(C)}\left(\frac{t_{V(C)}}{t_{SW}}\right)$$
$$\approx i_L v_{SW}\left(\frac{t_{I(C)}}{3t_{SW}} + \frac{t_{V(C)}}{2t_{SW}}\right). \quad (5)$$

### B. Delays

$i_{DS}$ reaches $i_L$ when $v_{GS}$ reaches the threshold voltage $v_{TH(C)}$ required for $M_{SW}$ to sustain $i_L + i_{GD}$. Usually, $i_{GD}$ is negligible compared to $i_L$:

$$v_{TH(C)} = v_{GS}|_{i_L+i_{GD}} = V_{TN0} + v_{DS(sat)}|_{i_L+i_{GD}}$$
$$\approx V_{TN0} + \sqrt{\frac{2(i_L+i_{GD})}{K_N'\left(\frac{W}{L}\right)}} \approx V_{TN0} + \sqrt{\frac{2i_L}{K_N'\left(\frac{W}{L}\right)}}. \quad (6)$$

$t_{I(C)}$ is the time required for the driver to charge $C_{GS}$ and $C_{GD}$ through $R_U$, as $v_{GS}$ goes from $V_{T0}$ to $v_{TH}$. Since the power supply $v_{DD}$ of the gate driver and $R_U$ require RC time $t_X$ to charge $C_{GS}$ and $C_{GD}$ to $v_X$, $t_X$ and $t_{I(C)}$ are:

$$t_X = \tau_{RC}\ln\left(\frac{v_{DD}}{v_{DD}-v_X}\right). \quad (7)$$

$$t_{I(C)} \approx t_{TH(C)} - t_{T0} = \tau_{RC}\ln\left(\frac{v_{DD}-V_{T0}}{v_{DD}-v_{TH}}\right). \quad (8)$$

where $\tau_{RC}$ is the time constant of $R_U$, $C_{GS}$, and $C_{GD}$ in saturation (as shown in Fig. 3, $C_{GS} = C_{OL} + (2/3)C_{CH}$ and $C_{GD} = C_{OL}$ in saturation):

$$\tau_{RC} = R_U(C_{GS} + C_{GD}) = R_U\left[2C_{OL} + \left(\frac{2}{3}\right)C_{CH}\right]. \quad (9)$$

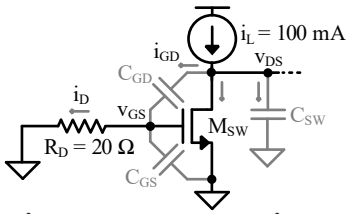
$t_{V(C)}$ is the time required for $v_{DS}$ to collapse, as $R_U$ limits current $i_U$ that feeds $C_{GD}$. $C_{GD}$ slews at the $v_{GS}$ that sustains $i_L + i_{GD}$. Across $t_{V(C)}$, $M_{SW}$ transitions from saturation to triode, so $C_{GD}$ starts to carry $0.5C_{CH}$ when $v_{DS}$ matches $v_{GS}$'s $v_{TH}$ (as shown in Fig. 3), which averages to $0.5(0.5C_{CH})$ across $v_{TH(C)}$, so $t_{V(C)}$ is:

$$t_{V(C)} \approx \left(\frac{\Delta v_{CGD}}{i_U}\right)C_{GD}$$
$$\approx \left(\frac{R_U}{v_{DD}-V_{TH(C)}}\right)\left[v_{SW}C_{OL} + v_{GS}\left(\frac{0.5C_{CH}}{2}\right)\right]$$
$$\approx \left(\frac{R_U}{v_{DD}-V_{TH(C)}}\right)\left[v_{SW}C_{OL} + v_{TH(C)}\left(\frac{C_{CH}}{4}\right)\right]. \quad (10)$$

## IV. Opening MOSFET

### A. Power

For the closing of the switch, the same approximations than in previous section are made. $M_{SW}$ is open by a driver with a pull-down resistance $R_D$, as shown below in Fig. 6:




$K_N' = 200\ \mu A/V^2$, $L_{OL} = 30$ nm, $C_{OX}'' = 6.9$ mF/m$^2$, $C_{GDO} = C_{GSO} = 0.207$ nF/m, $V_{T0} = 0.4$ V, $\lambda = 0.05$ m$^{-1}$, and W/L = 50 mm/250 nm.

**Fig. 6**. Simplified schematic for opening a switch.

During opening, $v_{DS}$ starts to rise when $v_{GS}$ reaches the voltage $v_{TH}$ required for $M_{SW}$ to sustain $i_L$ in saturation. Then, $i_{DS}$ drops, as shown in Fig. 7, leading to the following equation for $P_{IV(O)}$, which is similar to the one in Section III:

$$P_{IV(O)} = P_{I(O)}\left(\frac{t_{I(O)}}{t_{SW}}\right) + P_{V(O)}\left(\frac{t_{V(O)}}{t_{SW}}\right)$$

$$\approx i_L v_{SW}\left(\frac{t_{I(O)}}{3t_{SW}}+\frac{t_{V(O)}}{2t_{SW}}\right). \quad (11)$$

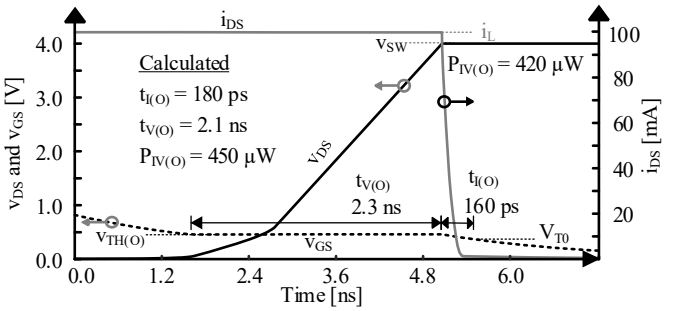



**Fig. 7**. Simulated waveforms for opening a switch.

## B. Delays

$t_{V(O)}$ and $v_{TH(O)}$ for opening is calculated similarly to $t_{V(C)}$ and $v_{TH(C)}$, except that $M_{SW}$ has to sink $i_L$-$i_{GD}$:

$$v_{TH(O)} = v_{GS}|_{i_L-i_{GD}} = V_{TN0} + v_{DS(sat)}|_{i_L-i_{GD}}$$
$$\approx V_{TN0} + \sqrt{\frac{2(i_L-i_{GD})}{K_N'\left(\frac{W}{L}\right)}} \approx V_{TN0} + \sqrt{\frac{2i_L}{K_N'\left(\frac{W}{L}\right)}}. \quad (12)$$

$$t_{V(O)} \approx \left(\frac{\Delta v_{CGD}}{i_D}\right) C_{GD}$$
$$\approx \left(\frac{R_D}{V_{TH(O)}}\right)\left[v_{SW}C_{OL} + v_{TH(O)}\left(\frac{C_{CH}}{4}\right)\right]. \quad (13)$$

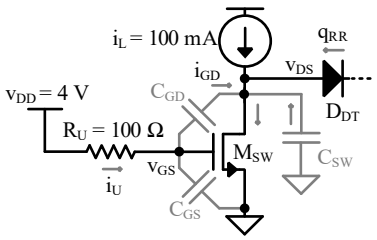
$t_{I(O)}$ is calculated as in Section III, except that during opening, the gate is driven by a pull-down resistance connected to ground:

$$t_{I(O)} \approx t_{T0} - t_{TH} = \tau_{RC}\ln\left[\frac{v_{DD}-(v_{DD}-v_{TH(O)})}{v_{DD}-(v_{DD}-V_{T0})}\right]$$
$$= \tau_{RC}\ln\left(\frac{v_{TH(O)}}{V_{T0}}\right). \quad (14)$$

$$\text{With } \tau_{RC} = R_D(C_{GS}+C_{GD}) = R_D\left[2C_{OL}+\left(\frac{2}{3}\right)C_{CH}\right]. \quad (15)$$

## V. Reverse Recovery

When the ground switch is off during dead-times, the body diode of the high side switch is conducting, as shown in Fig. 8. Forward-biased in-transit charge across PN junctions reverses direction when diodes reverse-bias. This diode carries this reverse-recovery charge $q_{RR}$ when conducting $i_L$. $q_{RR}$ is the charge in the junction that $i_L$ feeds and forward transit time $\tau_F$ across the junction sets to $i_L\tau_F$.




$K_N'$ = 200 µA/V$^2$, $L_{OL}$ = 30 nm, $C_{OX}$" = 6.9 mF/m$^2$, $C_{GDO}$ = $C_{GSO}$ = 0.207 nF/m, $V_{T0}$ = 0.4 V, λ = 0.05 m$^{-1}$, W/L = 50 mm/250 nm, $I_S$ = 1 fA, $\tau_F$ = 300 ps, n = $10^{-3}$.

**Fig. 8**. Simplified schematic for closing a switch with reverse recovery.

In Fig. 8, for example, dead-time diode $D_{DT}$ conducts $i_L$ when $M_{SW}$ is open. So for $v_{DS}$ to fall when $M_{SW}$ closes, $i_{DS}$ must first rise to a peak $i_{DS(RR)}$ that sinks $i_L$ and recovers $q_{RR}$ held in $D_{DT}$, as shown in Fig. 9. And a higher $i_{DS}$ dissipates more $P_{IV}$.

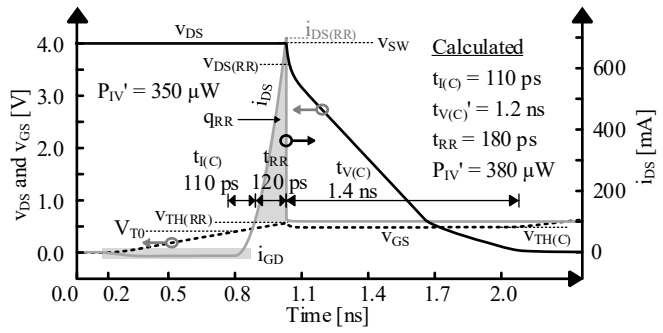



**Fig. 9**. Simulated waveforms for closing a switch with reverse recovery.

## A. Power

$P_{IV}$ considering reverse recovery is the same than in Section III, with the following two exceptions: $v_{DS}$ is steady at $v_{SW}$ across $t_{I(C)}$ and $t_{RR}$, so $P_I'$ is the power $i_{DS(RR)}$'s average 33%$i_{DS(RR)}$ burns with $v_{SW}$, and since $i_{DS}$ is steady at $i_L$ across $t_{V(C)}'$, $P_V'$ is the power $i_L$ burns with $v_{DS(RR)}$'s average 50%$v_{DS(RR)}$. And $P_{IV}'$ is a $t_{SW}$ fraction of $P_I'$ and $P_V'$:

$$P_{IV}' = P_I'\left(\frac{t_{I(C)}+t_{RR}}{t_{SW}}\right) + P_V'\left(\frac{t_{V(C)}'}{t_{SW}}\right)$$
$$\approx \left(\frac{i_{DS(RR)}}{3}\right)v_{SW}\left(\frac{t_{I(C)}+t_{RR}}{t_{SW}}\right) + i_L\left(\frac{v_{DS(RR)}}{2}\right)\left(\frac{t_{V(C)}'}{t_{SW}}\right). \quad (16)$$

## B. Delays

As $M_{SW}$ closes, $i_{DS}$ climbs with $v_{GS}$ after $v_{GS}$ overcomes $V_{T0}$. $i_{DS}$ reaches $i_L$ after $v_{GS}$ reaches $v_{TH(C)}$. Approximating $i_{DS}$'s rise past $i_L$ to be linear with the slope $di_{DS}/dt$ that $i_{DS}$'s $(i_L/t_{I(C)}^2)t^2$ reaches at $t_{I(C)}$, $i_{DS}$ requires another $t_{RR}$ to reach a level that can sink $q_{RR}$:

$$q_{RR} = \int_0^{t_{RR}} i_{DS}\,dt \approx \int_0^{t_{RR}} \frac{di_{DS}}{dt}\Big|_{t_{I(C)}} tdt$$
$$\approx \int_0^{t_{RR}} \left(\frac{2i_L}{t_{I(C)}}\right)tdt = \left(\frac{i_L}{t_{I(C)}}\right)t_{RR}^2 = i_L\tau_F. \quad (17)$$

This means that $t_{RR}$ is roughly a squared-root translation of $t_{I(C)}$ and $\tau_F$:

$$t_{RR} \approx \sqrt{t_{I(C)}\tau_F}. \quad (18)$$

and $i_{DS(RR)}$ is a corresponding $t_{RR}$ extension of $i_L$:

$$i_{DS(RR)} \approx i_L + \left(\frac{2i_L}{t_{I(C)}}\right)t_{RR} = i_L\left(1+2\sqrt{\frac{\tau_F}{t_{I(C)}}}\right). \quad (19)$$

The $v_{GS}$ that $M_{SW}$ requires to sink this $i_{DS(RR)}$ is $v_{TH(RR)}$:

$$v_{TH(RR)} = V_{TN0} + v_{DS(sat)}|_{i_{DS(RR)}}$$
$$\approx V_{TN0} + \sqrt{\frac{2i_{DS(RR)}}{K_N'\left(\frac{W}{L}\right)}}. \quad (20)$$

After $i_{DS}$ recovers $q_{RR}$, $i_{DS(RR)}$ sinks more than $i_L$ supplies, so $i_{DS}$ discharges $C_{GD}$ and $C_{SW}$. The $i_{GD}$ that $i_{DS(RR)}$ and $i_L$ avail is so much greater than $i_U$ that $i_{GD}$ discharges $C_{GS}$. $C_{GD}$, $C_{SW}$, and $C_{GS}$ discharge this way until $i_{DS}$ falls to $i_L$, which happens when $v_{GS}$ reaches $v_{TH}$. Since $i_U$ is much lower than $i_{GD}$, $C_{GS}$ supplies the charge $\Delta q_{GS}$ that largely discharges $C_{GD}$ across $\Delta v_{DG}$ or $\Delta v_{DS} - \Delta v_{GS}$:

$$\Delta q_{GD} = C_{GD}\Delta v_{DG} = C_{GD}(\Delta v_{DS} - \Delta v_{GS})$$
$$= C_{GD}(v_{SW} - v_{DS(RR)} - \Delta v_{GS})$$

$$\approx \Delta q_{GS} = C_{GS}\Delta v_{GS} = C_{GS}\left(v_{TH(RR)} - v_{TH}\right)$$
$$= C_{GS}\Delta v_{TH}. \quad (21)$$

where $C_{GS}$ discharges across $\Delta v_{GS}$ and $\Delta v_{TH}$ from $v_{TH(RR)}$ to $v_{TH}$ and $v_{DS}$ falls across $\Delta v_{DS}$ from $v_{SW}$ to $v_{DS(RR)}$. Solving (20) for $v_{DS(RR)}$ leads to:

$$v_{DS(RR)} = v_{SW} - \left(\frac{C_{GS}}{C_{GD}} + 1\right)\Delta v_{TH}. \quad (22)$$

$v_{SW} = v_O + v_D$, where $v_D$ is the voltage dropped by the diode $D_{DT}$. This transition to $v_{DS(RR)}$ is quick because $i_{GD}$ is substantial. After $i_{DS}$ falls to $i_L$, $i_U$ discharges $C_{GD}$ across the $t_{V(C)}'$ that collapses $v_{DS(RR)}$. $t_{V(C)}'$ is shorter than $t_{V(C)}$ because $v_{DS}$ collapses $v_{DS(RR)}$, which is lower than $v_{SW}$:

$$t_{V(C)}' = \left(\frac{R_U}{v_{DD} - v_{TH(C)}}\right)\left[v_{DS(RR)}C_{OL} + v_{TH}\left(\frac{C_{CH}}{4}\right)\right]. \quad (23)$$

## VI. Asynchronous Boost Example

In this section, an example of a boost converter is studied to compare theoretical parameters with simulated ones, as shown below in Fig. 10. An asynchronous circuit has been chosen here for the sake of simplicity, but the switching mechanics of the ground switch described in this paper still hold for a synchronous architecture with the body diode of the high side conducting during dead time before the ground switch turns on. The table further below compares simulations with theory with and without reverse recovery.

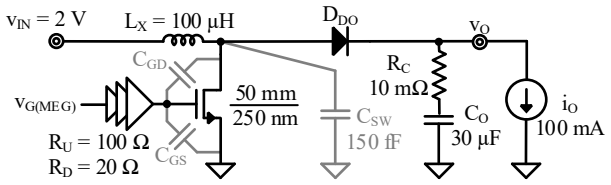



**Fig. 10**. Simulated asynchronous boost dc–dc converter schematic.

**TABLE I**. Performance Comparison.

| Parameters | Calculated | Simulated | Error |
|---|---|---|---|
| $t_{I(C)}$ | 170 ps | 180 ps | –10 ps |
| $t_{I(O)}$ | 270 ps | 280 ps | +10 ps |
| $t_{V(C)}$ | 1.6 ns | 1.6 ns | 0 ns |
| $t_{V(O)}$ | 2.2 ns | 2.3 ns | +0.1 ns |
| $P_{IV}$ | 2.1 mW | 1.9 mW | –200 µW |
| $k_{IV}$ | 0.5% | 0.4% | –0.1% |
| RR: $t_{V(C)}'$ | 1.4 ns | 1.5 ns | +0.1 ns |
| $t_{RR}$ | 220 ps | 160 ps | +60 ps |
| $P_{IV}'$ | 2.3 mW | 2.1 mW | –200 µW |
| $k_{IV}'$ | 0.5% | 0.4% | –0.1% |

$d_E$ = 55 %, $f_{SW}$ = 1 MHz, $K_N'$ = 200 µA/V², $L_{OL}$ = 30 nm, $C_{OX}''$ = 6.9 mF/m², $C_{GDO} = C_{GSO}$ = 0.207 nF/m, $V_{T0}$ = 0.4 V, $\lambda$ = 0.05 m$^{-1}$, $I_S$ = 1 fA, n = 0.8, $\tau_F$ = 300 ps.

Interestingly, $q_{RR}$ not only raises the $i_{DS}$ that consumes $P_I'$ (to $i_{DS(RR)}$) and extends the time $P_I'$ burns (by $t_{RR}$) but also reduces the $v_{DS}$ (to $v_{DS(RR)}$) that burns $P_V'$. The rise in $i_{DS}$, however, normally raises $P_I'$ more than the fall in $v_{SW}$ reduces $P_V'$. So reducing $q_{RR}$ usually saves power.

## VII. Conclusion

An insightful device-based model was derived for predicting $P_{IV}$ in switching inductor power supplies. The expressions derived in this article are device-based, not data-based like in the state of the art. A simple model to estimate reverse recovery losses has also been proposed. Calculated and simulated overlap losses with and without reverse recovery are within ±10%. Predicting this loss and its effect on efficiency with calculations is critical when designing a power supply, especially when considering this loss scales with output power.

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