Stability Analysis & Design of Hysteretic Current-mode Switched-inductor Buck DC–DC Converters

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***Abstract*—Battery-supplied systems demand fast, power efficient, and compact power supplies. Although linear regulators are quick and small, tiny batteries cannot sustain their losses for long. Pulse-width-modulated (PWM) switchers are considerably more efficient, but also slower. Luckily, hysteretic converters can respond within one switching cycle. Stabilizing the system for maximum speed with a hysteretic inductor-current loop, however, which is not linear, is not straightforward. This paper shows how load dumps delay the response of the hysteretic oscillator that the current loop implements. Knowing the worse-case dump and the delay it causes reveals the lowest output capacitance that maintains stable operation at maximum speed. The converter designed here can therefore recover, as predicted, from 100-mA load dumps in 2 µs with 10 µF and 45° of phase margin.**

***Index Terms*—Hysteretic current-mode control, design, analysis, dc–dc switching converter, stability, high bandwidth**

I. Switched-inductor Converters

Cellular phones, tablets, and other portable electronics today include on-demand functions like data conversion, telemetry, and others that require fast-responding and power-efficient supplies. Low-dropout (LDO) regulators are fast and compact, but not as efficient as their switched-inductor counterparts. Pulse-width-modulated (PWM) supplies are therefore popular, except they require several clock cycles to respond to load dumps. Luckily, hysteretic loops respond when their controlled variables surpass their window limits, so they react within one switching cycle [1].

Unfortunately, understanding the nonlinear feedback dynamics of hysteretic converters is arduous. Phase-plot portraits [2], sliding-mode theory [3]–[5], state-space averaging [6]–[7], and circuit averaging [8]–[12] help, but the equations they generate are often abstract and difficult to relate to circuit operation, to inductor-current and output-voltage ripples, response time, and others. This is why engineers ultimately over-size inductors or capacitors, and in so doing, counter their own miniaturization efforts.

This paper analyses hysteretic current-mode buck dc–dc converters from the perspective of a circuit-design engineer. In this light, as Section II explains, the hysteretic current loop implements an oscillator, whose closed-loop gain and delay Section III describes and quantifies. Section IV later discusses how the oscillator block affects the feedback dynamics of the voltage loop. Section V then verifies the analysis and design strategy for maximum speed and Section VI draws relevant conclusions.

II. Design Strategy

With enough equivalent series resistance (ESR) in the output capacitor, hysteretic buck converters can be simple and widely stable. This is because ESRs save some of the phase inductors and capacitors lose with the poles they establish. Unfortunately, state-of-the-art systems cannot afford to accommodate the voltage these ESRs produce when responding to sudden load dumps. So, with little to no ESR, engineers resort to removing the influence of inductors in other ways.

Current-mode control turns the inductor L_O into a current source by "regulating" L_O's current i_L [13]. In the hysteretic case, however, which Fig. 1 illustrates, a relaxation oscillator keeps L_O's i_L rippling about i_L's average $i_{L(AVG)}$ between the hysteretic limits that CP_{OSC} and R_S set. This way, L_O's ripple Δi_L is constant and the oscillator is a transconductor block inside the voltage loop that outputs $i_{L(AVG)}$ according to $v_{O.EA}$.

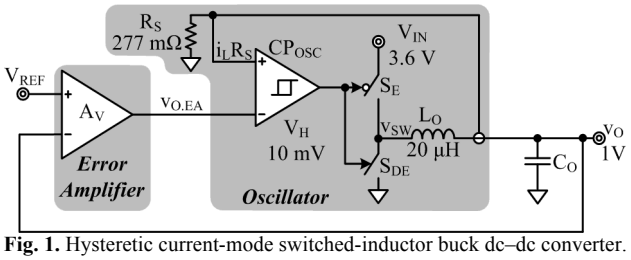

Fig. 1. Hysteretic current-mode switched-inductor buck dc–dc converter.

So, as with any regulator, the design of a hysteretic current-mode buck converter starts with load requirements. Response time, for example, determines system bandwidth f_{0dB}, which together with loop gain A_{LG}, as another section will show, sets output capacitance C_O. Stability or phase margin PM and f_{0dB} then defines the bandwidth $f_{BW.I}$ of the oscillating block. Next, $f_{BW.I}$, worst-case load-dump Δi_O, input voltage V_{IN}, and the targeted output V_O constrain L_O. In the end, with C_O in hand, output-ripple requirement Δv_O sets the ripple current Δi_L and period T_{OSC} of the oscillator.

III. Current Loop: Hysteretic Oscillator

A. Operation

Since the system regulates v_O and v_O's ripple Δv_O is miniscule with respect to v_O, v_O for the oscillator is practically constant at V_O. As such, i_L in Fig. 1 and the voltage $i_L R_S$ that i_L generates across R_S rise linearly when switch S_E energizes L_O from V_{IN} to v_O with voltage V_E at $V_{IN} - V_O$ at di_L^+/dt or V_E/L_O, as Fig. 2 shows. When $i_L R_S$

surpasses CP_{OSC}'s upper threshold, CP_{OSC} trips and opens S_E and closes S_{DE}, which drains L_O to v_O. With a negative de-energizing voltage $-V_{DE}$ at $-V_O$ across L_O, i_L and i_LR_S reverse direction at di_L^-/dt or $-V_{DE}/L_O$ until i_LR_S reaches CP_{OSC}'s lower threshold. This way, i_LR_S rises and falls to traverse CP_{OSC}'s hysteresis V_H across energizing and de-energizing times T_E and T_{DE}, and together, across T_{OSC}, so

$$\Delta i_L = \frac{V_H}{R_S}, \tag{1}$$

$$T_E = \left(\frac{L_O}{V_E}\right)\Delta i_L \approx \left(\frac{L_O}{V_{IN} - V_O}\right)\left(\frac{V_H}{R_S}\right), \tag{2}$$

$$T_{DE} = \left(\frac{L_O}{V_{DE}}\right)\Delta i_L \approx \left(\frac{L_O}{V_O - 0}\right)\left(\frac{V_H}{R_S}\right), \tag{3}$$

and

$$f_{OSC} = \frac{1}{T_{OSC}} = \frac{1}{T_E + T_D}, \tag{4}$$

In short, Δi_L is constant and traverses across V_H/R_S every T_{OSC} period.

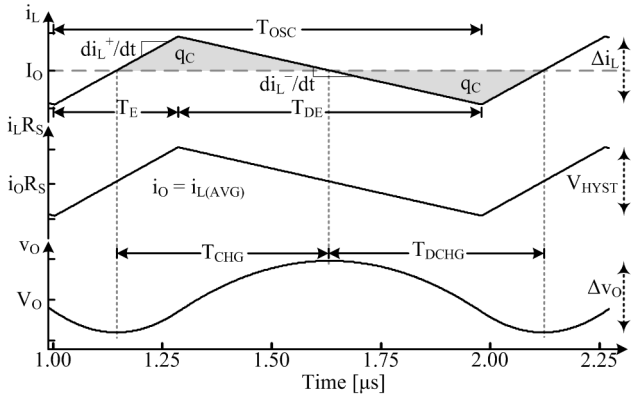

Fig. 2. Simulated steady-state waveforms of the hysteretic buck converter.

Since the load sinks $i_{L(AVG)}$, i_L's ripple Δi_L flows entirely into C_O to establish how much the output v_O ripples in steady state. The charge q_C that Δi_L sources and sinks across every half period $0.5T_{OSC}$ is basically the area under Δi_L about $i_{L(AVG)}$. So, since Δi_L is a triangular waveform, C_O's ripple Δv_O reduces to

$$\Delta v_O = \frac{q_C}{C_O} = \frac{(0.5)(0.5\Delta i_L)(0.5T_{OSC})}{C_O} = \frac{\Delta i_L T_{OSC}}{8C_O}. \tag{5}$$

B. Gain and Bandwidth

To the overall system, the oscillator is simply a block that outputs and adjusts $i_{L(AVG)}$ in response to a voltage $v_{O.EA}$. To see this, recall that CP_{OSC}'s hysteresis V_H is about its input $v_{O.EA}$. This means $v_{O.EA}$ is the center voltage $i_{L(AVG)}R_S$ about which i_LR_S oscillates. In other words, the block's low-frequency transconductance gain A_{G0} or $i_{L(AVG)}/v_{O.EA}$ is:

$$A_{G0} \equiv \left.\frac{i_{L(AVG)}}{v_{O.EA}}\right|_{\text{Low frequency}} = \frac{1}{R_S}. \tag{6}$$

Since bandwidth essentially describes response time, the time t_R the oscillator requires to adjust $i_{L(AVG)}$ to a new value is a measure of its bandwidth $f_{BW.I}$. In this light, since variations in $v_{O.EA}$, as Fig. 3 shows at 0.5 and 2 µs, shift CP_{OSC}'s thresholds, i_L's rising and falling rates di_L^+/dt at V_E/L_O and di_L^-/dt at $-V_{DE}/L_O$ determine t_R. Since the RC-equivalent bandwidth that corresponds to reaching 98% of i_L's target is $1/2\pi R_{EQ}C_{EQ}$ from i_L^* in Fig. 3 and

$$t_R \equiv R_{EQ}C_{EQ}\ln\left(\frac{1}{1-0.98}\right) = 4R_{EQ}C_{EQ} \equiv \frac{4}{2\pi f_{BW.I}}, \tag{7}$$

$1/2\pi R_{EQ}C_{EQ}$ is a linear equivalent that can model $f_{BW.I}$.

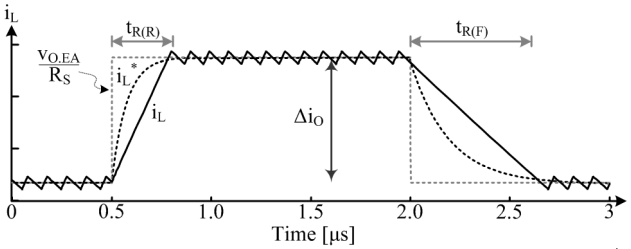

Fig. 3. Step response of inductor current i_L and its $R_{EQ}C_{EQ}$ equivalent i_L^*.

Although i_L slews to 98% of its target and its linear counterpart i_L^* rises exponentially, both reach 98% at the same time. Since i_L^* slows as it nears its ultimate target and the actual does not, modeling i_L to 80% with i_L^* means i_L^* requires more time to reach its final value than i_L. This is a pessimistic expectation that results in an over-sized C_O. As simulations will later prove, modeling the response to 98% predicts the oscillator's bandwidth and response fairly well.

For $i_{L(AVG)}$ to traverse across $\Delta i_{L(AVG)}$, i_L must rise or fall by an equivalent amount. Since quasi-constant voltages V_E and V_{DE} energize and de-energize L_O, i_L ramps at a constant rate di_L/dt according to L_O's impressed voltage V_L. Since V_L is V_E when i_L rises and V_{DE} otherwise, the response time t_R for rising and falling load dumps is different:

$$t_R = \frac{\Delta i_{L(AVG)}}{di_L/dt} = \Delta i_{L(AVG)}\left(\frac{L_O}{V_L}\right) = \Delta i_O\left(\frac{L_O}{V_L}\right), \tag{8}$$

where $i_{L(AVG)}$ flows to the load as i_O. Unfortunately, modeling $f_{BW.I}$ with the longest t_R is overly pessimistic and with the shortest delay overly optimistic. Plus, a real response incorporates ringing that invokes both rising and falling slopes. Therefore, emulating the average of these delays with the previously defined 98% RC model balances the approximation and reduces V_L to $0.5(V_E + V_{DE})$, $f_{BW.I}$ to

$$f_{BW.I} = \left(\frac{4}{2\pi}\right)\left(\frac{1}{\Delta i_O}\right)\left(\frac{V_E + V_{DE}}{2L_O}\right), \tag{9}$$

and the oscillator's gain and response A_G to

$$A_G = \frac{A_{G0}}{1 + \frac{s}{2\pi f_{BW.I}}} = \frac{1}{R_S\left(1 + \frac{s}{2\pi f_{BW.I}}\right)}. \tag{10}$$

Since i_L requires more time to reach its target with higher load dumps Δi_O, $f_{BW.I}$ is inversely proportional to Δi_O. This means the worst-case delay across the oscillator corresponds to the highest load dump. In other words, hysteretic current-mode converters are least stable when subjected to wider load dumps, when $f_{BW.I}$ is lowest and closest to the systems unity-gain bandwidth f_{0dB}.

Incidentally, $f_{BW.I}$'s dependence on Δi_O is an indication that the hysteretic transconductor block is nonlinear.

IV. Voltage Loop

A. Operation

Amplifier A_V in Fig. 1 compares v_O to reference V_{REF} to generate an error voltage v_E in Fig. 4. When multiplied by A_V and the oscillator's A_G, v_E produces and feeds $i_{L(AVG)}$ to the load's C_O and R_O. So, with negative feedback, offsetting v_O from V_{REF} raises and amplifies v_E to oppose and reduce the offset between v_O and V_{REF} back to zero.

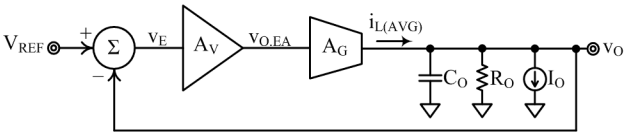

Fig. 4. Equivalent block diagram of the hysteretic buck dc–dc converter.

B. Stability

The loop is stable with 45° of phase margin when the loop gain A_{LG} reaches 0 dB and the unity-gain frequency f_{0dB} at 20 dB per decade, which can only happen after one pole. For this, the output pole p_O that R_O and C_O establish must be low enough to ensure A_{LG} reaches f_{0dB} before A_V's and A_G's respective bandwidths $p_{BW.A}$ and $f_{BW.I}$:

$$A_{LG} \equiv \frac{v_O}{v_E} = A_V A_G \left(R_O \parallel \frac{1}{sC_O} \right) = \frac{A_V A_G R_O}{1 + sC_O R_O} . \qquad (11)$$

Because A_{LG} falls linearly with frequency past p_O, the gain–bandwidth product that A_{LG0} and p_O establish is constant between p_O and f_{0dB} and equivalent to f_{0dB} at 0 dB:

$$f_{0dB} = A_{LG0} p_O = \left(\frac{A_V R_O}{R_S} \right) \left(\frac{1}{2\pi C_O R_O} \right) = \frac{A_V}{2\pi C_O R_S} . \qquad (12)$$

C_O must therefore be sufficiently high to ensure f_{0dB} is near or below the oscillator's $f_{BW.I}$. In feedback terms, A_{LG} must reach f_{0dB} with enough phase margin PM to maintain stable conditions. Since p_O is well below f_{0dB} and $f_{BW.I}$ near or above f_{0dB}, p_O lowers 90° of phase from the loop's 180° and $f_{BW.I}$ another fraction of 90° to reduce PM to

$$PM = 90 - \tan^{-1} \left(\frac{f_{0dB}}{f_{BW.I}} \right) . \qquad (13)$$

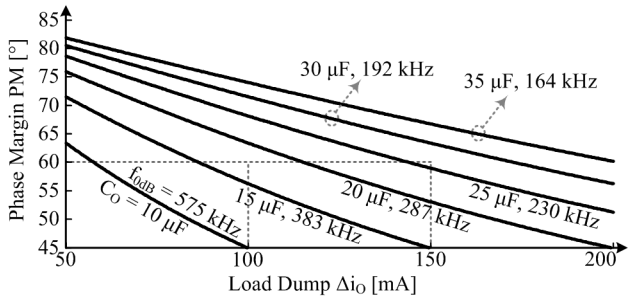

Fig. 5. Phase margin across load dumps and output capacitance.

Since the oscillator's bandwidth $f_{BW.I}$ changes with load dumps Δi_O, so does phase margin PM. With 10 µF of output capacitance C_O, for example, PM for the design of Fig. 1 is roughly 64° when subjected to 50-mA load dumps and 45° under 100-mA dumps, as Fig. 5 shows. With 20 µF, PM is 76° with 50 mA and 45° with 200 mA. In other words, the lowest allowable PM and the largest Δi_O ultimately dictate the lowest possible C_O.

V. Design Validation

The sample objective of the hysteretic buck converter of Fig. 1 is to generate a 0.4-mV ripple about 1 V that recovers from 100-mA load dumps within 1.5 µs with 45° of phase margin. With 45°, the output should settle to its new steady-state value after two oscillating rings [14]. This is why the targeted output ripple is so low: to ensure the output resolution is sufficiently fine to discern the oscillating rings that result from an under-damped system.

A. Design Process

To supply 98% of the load dump Δi_O within 1.5 µs, roughly four 424-kHz time constants must elapse, so f_{0dB} can be 500 kHz. With a 277-mΩ current-sense resistor R_S and a 20-dB amplifier A_V, C_O should not exceed 11.5 µF, so 10 µF complies with f_{0dB}. And for 45° of phase margin, the oscillator block's bandwidth $f_{BW.I}$ should be at f_{0dB} or 500 kHz and oscillating frequency f_{OSC} above that at, for example, 1 MHz.

With a 3.6-V input V_{IN} and a 1-V output V_O, energizing and de-energizing voltages V_E and V_{DE} are 2.6 and 1.0 V. With these, L_O should be less than 23 µH, so 20 µH satisfies $f_{BW.I}$ and f_{OSC} under 100-mA load dumps. Therefore, to produce 0.5-mV of output ripple Δv_O at 1 MHz, the oscillator should output a 40-mA current ripple Δi_L.

B. Validation

Fig. 6b shows the simulated response of the designed system. The resulting current and voltage ripples Δi_L and Δv_O are, as expected, roughly 36 mA and 0.4 mV. Although not obvious at first, inductor current i_L undergoes two oscillating rings before it settles after 100-mA rising and falling load dumps. The second ring is basically an oversized current ripple Δi_L of 45 mA. This means the system has, as expected, about 45° of phase margin.

With less output capacitance C_O, as Fig. 6a demonstrates for 5 µF, i_L settles after four to five rings, which corresponds to less than 45° of phase margin. In contrast, 17 µF produces no more than one ring, as Fig. 6c shows, so phase margin is higher at roughly 60° [14]. Note phase margin is worse for falling load dumps in Figs. 6a and 6c, when C_O is 5 and 17 µF, than for rising load dumps. This is because L_O's energizing voltage V_E at 2.6 V is higher than its de-energizing counterpart V_{DE} at 1.0 V, so i_L rises more quickly than it falls. In other words, the oscillator is faster when i_L climbs than when i_L drops.

With a higher load dump at 150 mA, the system recovers after three rings, as Fig. 6d illustrates. In other words, phase margin falls below 45° when Δi_O rises above its specified target. To maintain 45°, C_O must therefore rise to 15 µF, and for 60°, to 26 µF, as Figs. 6e–f further show. Irrespective of the conditions, however, phase margin for rising load dumps is, as before, equal or better than for their

falling counterparts. Also, since current ripple Δi_L and oscillating frequency f_{OSC} are the same across these graphs, raising C_O lowers output voltage Δv_O.

VI. Conclusions

This paper shows how to analyze and design stable hysteretic current-mode buck dc–dc converters for maximum speed. The underlying concept here is that the hysteretic inductor-current loop is a relaxation oscillator whose current ripples about an adjustable average that the voltage loop controls. The oscillator is therefore a transconductor block inside the voltage loop. Since inductor current rises and falls at different rates, the delay across the oscillating block changes with load dumps. However, mapping the delay to an RC-equivalent bandwidth that responds within the same time as the average of the delays simplifies and models the nonlinear system sufficiently well to predict phase margin. This way, engineers can design hysteretic converters for maximum speed with the lowest capacitance possible. This is important because hysteretic supplies respond within one switching cycle, several clock cycles faster than their pulse-width-modulated (PWM) counterparts. This means fast, stable, and tiny dc–dc converters can supply functionally diverse wireless microsystems whose components often engage on demand to produce vast load dumps.

Acknowledgement

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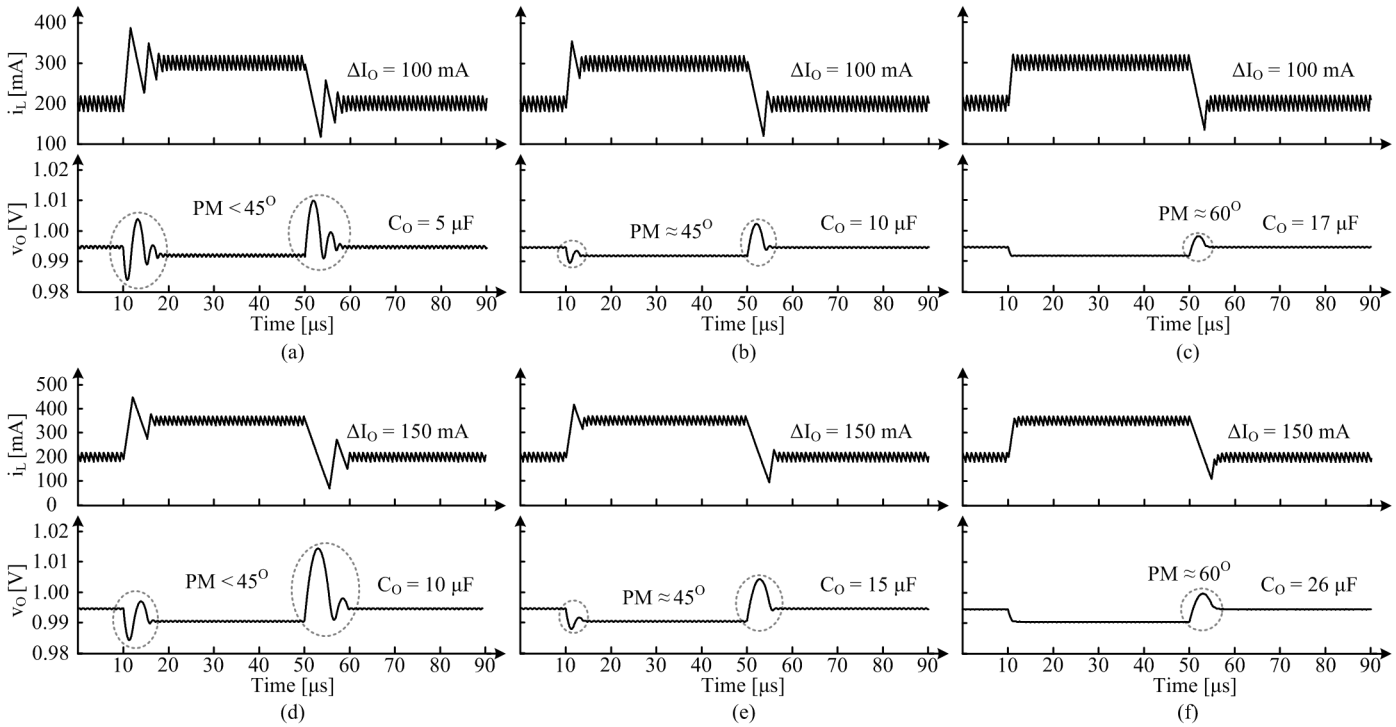

Fig. 6. Simulated load-dump responses of the hysteretic current-mode switched-inductor buck dc–dc converter designed.