Asynchronous Nonlinear Power-Tracking Supply for Power Efficient Linear RF PAs

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Abstract—**In the world of portable wireless electronics, battery life and therefore power efficiency are key parameters, and RF power amplifiers (PAs) are severe limiting agents in this regard because of their power-intensive demands. Spectral density is also critical to extend the effective bandwidth of a wireless transmitter, which is why linear PAs are popular, in spite of their inherently low power efficiency levels. An asynchronous power-tracking scheme is therefore proposed to more efficiently power-condition the supply of linear RF PAs and extend overall battery life performance. The RF supply is comprised of a high power but slow-responding voltage regulator with a lower power but fast-responding parallel nonlinear clamping circuit. Simulations with a SiGe HBT Class-A RF PA show that the proposed circuit consumes 10-15% less total power and achieves 1.5% better overall power efficiency than the state-of-the-art power-tracking scheme while meeting the same error-vector magnitude (EVM) performance.**

I. INTRODUCTION

Battery life and system integration are fueling the market for wireless battery-powered applications like cellular phones, ad-hoc sensor networks, and others to explosive levels. Increasing functional density, however, necessarily diminishes battery life, which is why power efficiency is so important. In fact, the radio frequency (RF) power amplifier (PA), which is a key component to any wireless transmitter, requires a large portion of the total power budget, since its task is to drive considerable energy into the antenna. As a result, improving the efficiency performance of the RF PA has a significant positive impact on extending battery life.

Switching (i.e., nonlinear) PAs are generally more efficient than linear PAs because the voltage across the driving transistors, when supplying current, is relatively small. Modern wireless signals, however, like code-division multiple-access (CDMA) and orthogonal frequency-division modulation (OFDM), which include wideband CDMA and 802.11a/b/g signals, modulate both amplitude and phase to increase spectral density and transmission rate, thereby demanding the linearity performance that conventional switching PAs are unfortunately incapable of delivering. Switching PAs are therefore linearized or altogether replaced with linear Class-A or -AB PAs, which inherently have low power efficiencies.

To achieve both high efficiency and good linearity performance, one of two approaches is typically adopted: (a) linearize inherently power efficient (switching) PAs or (b) boost the power efficiency of linear PAs. A switching PA is linearized by conditioning its output signal with either feed-forward reconstruction or feedback processing. Feed-forward architectures, however, must match and synchronize the gain and delay of all outbound paths, complicating the circuit and compromising performance. Alternatively, feedback schemes employ feedback loops that are necessarily five to ten times faster than the processed signal (envelop and/or phase) to properly condition the signal before driving it to the antenna, ultimately bounding the maximum bandwidth and consequently spectral density and effective transmission rate.

Boosting the efficiency of linear PAs is gaining popularity mainly because sacrificing linearity for efficiency tends to be more robust, less costly, and less complicated than sacrificing efficiency for linearity, the latter of which applies to switching PAs. In fact, boosting the efficiency of a linear PA basically amounts to dynamically adapting the PA supply according to the driving signals, reducing the voltage across the PA when not needed and increasing it only when required. In practice, the supply becomes a function of either the envelop or the average power of the driving signal.

In this paper, an asynchronous power-tracking supply circuit for linear PAs is proposed and presented. The main objective is to improve power efficiency and therefore extend battery life, while in the process maintaining acceptable linearity performance. The paper is consequently organized as follows: Section II reviews typical PA requirements, Section III state-of-the-art in dynamic power supplies, Section IV the proposed scheme, Section V the circuit, and Section VI the simulation results. Section VII draws relevant conclusions.

II. PA BACKGROUND

Given a constant supply voltage, the PA is typically designed to optimally sustain its worst-case (maximum) input power, resulting in less than ideal biasing conditions for the predominant state of the PA, which normally falls well below peak levels. The power efficiency (η) of a Class-A PA decreases with output power (P_{OUT}),

$$\eta = \left(\frac{P_{OUT}}{P_{OUT\_MAX}}\right)\eta_{MAX}, \qquad (1)$$

where P_{OUT_MAX} is the peak output power and η_{MAX} is the power efficiency of the PA at P_{OUT_MAX} [1]. As a result, the instantaneous efficiency of a PA is highest at P_{OUT_MAX}.

Instantaneous efficiency, however, is not as important as average efficiency when considering battery life. Average efficiency η_{AVG} is defined as the ratio of average output power to average input power, and given by

$$\eta_{AVG} = \frac{\int_0^{P_{OUT\_MAX}} P_{OUT} \cdot \text{Prob}(P_{OUT})\, dP_{OUT}}{\int_0^{P_{OUT\_MAX}} P_{IN}(P_{OUT}) \cdot \text{Prob}(P_{OUT})\, dP_{OUT}}, \qquad (2)$$

where $\text{Prob}(P_{OUT})$ is the probability function of P_{OUT} and $P_{IN}(P_{OUT})$ is the input power when delivering P_{OUT} [2]. Since the average output power is less than the peak output power and the probability of occurrence of peak output power levels is low when compared to that of average power levels for most modern non-constant envelope RF signals, as illustrated in Fig. 1 for 802.11g signals [4], the average efficiency of the PA is normally low, as can be noted from (1) and (2) [3-4].
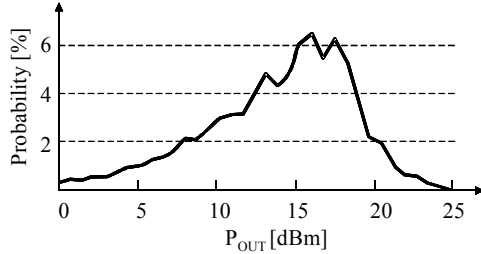

Figure 1.   Output power probability distribution for 802.11g signals.

The demands of a dynamically adaptive PA supply are most stringent for envelop-modulated signals whose probability for peak power is relatively higher yet average power is low. The problem is speed because a supply circuit must necessarily be bandwidth-limited to yield reasonable power efficiency performance. As a result, a PA supply cannot transiently follow the peak power conditions when initially biased at average power levels and must therefore back-off during normal operating conditions, sacrificing power efficiency in the process. The peak-to-average power ratio (PAPR) and probability of surpassing the average power by 3 dB of WCDMA, 802.11b, and 802.11a/g are 3.15, 1.78, and 8.24 dB and 0.08%, 0%, and 8%, respectively, as verified from simulations and reported in [3, 5-6] (also shown in Table 1), which is why PA average efficiencies for 802.11a/g signals tend to be worse.

Some signal degradation in the form of clipping may be tolerated to save power, however, but it must remain within acceptable limits. Error-vector magnitude (EVM) is a measure of this error, of signal to noise and distortion ratio (SNDR), which closely relates to bit-error rate (BER) at the receiver end [7]. As a result, any PA supply scheme must supply just enough headroom to yield acceptable EVM performance; more margin than needed constitutes unnecessary power losses.

TABLE I.   VARIOUS RF WIRELESS SIGNAL PARAMETERS.

	Typical $f_{Carrier}$ (GHz)	Application	PAPR (dB)	3 dB above Avg. Power Probability (%)	Envelope BW (MHz)
802.11a	5	Wireless LAN	8.2	8	20
802.11g	2.4	Wireless LAN	8.2	8	20
802.11b	2.4	Wireless LAN	1.8	0	20
CDMA IS-95	0.9/1.9	Mobile phone	5.1	2.2	1.23
WCDMA	1.95	Mobile phone	3.2	0.08	3.84
GSM	0.9/1.8/1.9	Mobile phone	0	0	0

III. BOOSTING EFFICIENCY WITH DYNAMIC PA SUPPLIES

Envelope Elimination and Restoration (EER): EER schemes essentially break the RF input signal into its phase with a limiter and envelop with an envelop detector and process them separately [8-9] (Fig. 2). The high frequency phase is processed with a switching PA, which is inherently power efficient, and its envelop is restored through a dynamic supply circuit, whose goal is to drive the envelop information back into the output. This approach suffers from two main drawbacks: (a) synchronizing the envelop and phase information (i.e., delay-matching) [10] and (b) having enough supply bandwidth to follow the envelop signal, which in the case of 802.11a/g signals amounts to bandwidths significantly higher than 20 MHz, where supply efficiency is prohibitively low [11].
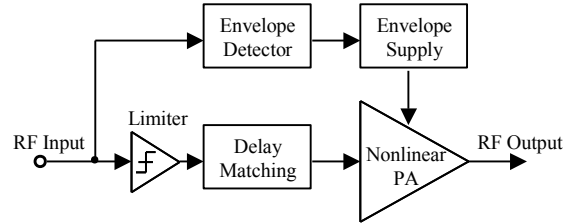

Figure 2.   Envelope elimination and restoration (EER).

Envelope-Following Supply: The envelop-following scheme is similar to the EER architecture in that the PA supply follows the envelop, but where it differs is in the PA itself, which is now linear and carries both envelop and phase information (Fig. 3) [12-13]. The supply in this case simply provides enough headroom for the PA to work; its purpose is not to set the envelop level of the PA output. As a result, the delay-matching requirements of the supply and the PA are mitigated. In the end, however, the supply bandwidth requirements are as stringent as those of the EER scheme and efficiency performance is lower than EER because a linear PA is now required.

Power-Tracking Supply: As mentioned earlier, the power efficiency of supply circuits decreases with bandwidth. In fact, the bandwidth of most practical supply circuits is well below 10 MHz, which is why EER and envelop-following architectures do not enjoy popularity in high envelope bandwidth wireless applications. As a result, designers have opted for a linear PA with an averaging power-tracking

supply (Fig. 4), whose output is a function of the average power but sufficiently backed off to yield acceptable EVM and BER performance (i.e., limit signal clipping instances). In this case, the supply bandwidth need not follow the envelop but the average power requirements, which have significantly lower bandwidths. The end result is lower PA efficiency (best PA efficiency is achieved when the supply follows the envelop) but even higher supply and therefore higher overall efficiency.
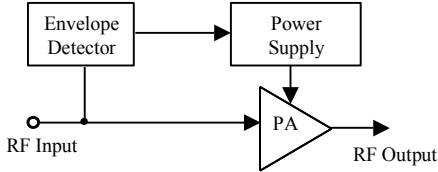

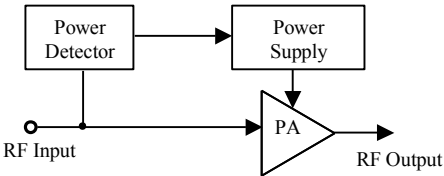Figure 3.   Envelope-following PA architecture.

Figure 4.   Linear PA with a power-tracking supply.

IV. PROPOSED NON-LINEAR POWER-TRACKING SUPPLY

The limitation of the aforementioned power-tracking scheme is efficiency because the supply is, on the average, higher than required (dotted trace in Fig. 5). To reduce this margin and therefore improve PA efficiency, the supply must be able to track peak-to-average power ratio (PAPR) events without, on the average, decreasing supply efficiency, which occurs with high bandwidth supply circuits. The proposed asynchronous power-tracking supply does just this (Fig. 5), reduce the average power supply level and dynamically adjust the supply voltage only during PAPR events, all with the same EVM performance but better overall efficiency.
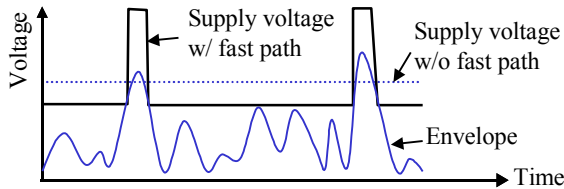

Figure 5.   Proposed asynchronous power-tracking supply voltage.

In the proposed embodiment, the average supply voltage is derived from a low bandwidth power-tracking supply circuit and the PAPR events supplied by a fast, parallel, nonlinear clamping circuit, as shown in Fig. 6. On the average, the nonlinear path is off and consumes next to no power. When the envelope signal exceeds the average level, the non-linear circuit activates and clamps the positive supply to its maximum level. The excess supply voltage during the PAPR event (Fig. 5) incurs minimal power losses because it occurs only for a small fraction of the total time.
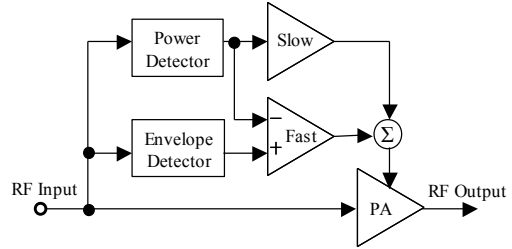

Figure 6.   Proposed asynchronous power-tracking supply scheme.

V. PROPOSED CIRCUIT

Operation: The proposed asynchronous power-tracking supply is shown in Fig. 7. The slow bandwidth, high power supply circuit is comprised of a sliding-mode, hysteretic DC-DC regulator with dead-time control circuit DTC to ensure the power switches are never conducting at the same time (i.e., to prevent short-circuit conditions) [14]. The hysteretic controller ensures PA supply V_{PA_Supply} is regulated against power-tracking reference V_{P_REF} by forcing it to remain within the hysteretic limits of the comparator (i.e., $V_{Hys\_Low} < V_{PA\_Supply} < V_{Hys\_High}$). The fast path, on the other hand, is simply a switch that is only engaged when its driving comparator senses that the envelop signal surpasses V_{TRIG}.
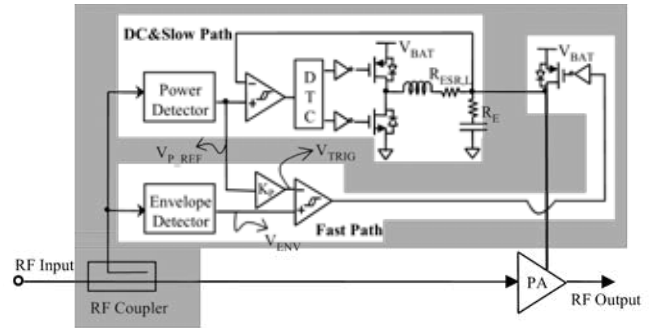

Figure 7.   Proposed asynchronous power-tracking supply circuit.

To meet the stringent linearity requirements of 802.11g signals, the PA is typically biased on the edge of Class-A operation, which implies large load-current transitions do not occur, and for the foregoing design, the average PA supply current (i.e., current drawn by the PA) is approximately 0.3 A. The goal here is to keep power-tracking voltage V_{P_REF} as low as possible (for high efficiency) while simultaneously maintaining acceptable EVM performance. According to the 802.11g standard, EVM must fall below 5.6% for a data rate of 54 Mbps.

The effective trigger point (V_{TRIG}) of the fast path is adjusted from V_{P_REF} to optimum levels by multiplier K_P. Reducing the value of K_P amounts to increasing the activation rate of the fast asynchronous path and therefore reducing signal clipping instances and improving EVM performance, but if K_P is too low, the supply switching noise degrades the linearity of the output and consequently degrades EVM, producing the upside-down bell-like response shown in Fig. 8. Additionally, increasing the activation rate (i.e., reducing K_P) increases switching losses and therefore reduces supply efficiency. In this case,

however, it also slightly increases the average supply voltage, increases slightly thereby increases the PA power gain of the PA and improving overall PA efficiency, given with the same input power. In the end, K_P must be optimally set to meet the EVM requirements (e.g., less than 5.6%) of the system at the highest possible PA efficiency – in the foregoing design, K_P was set to 1.3 at an input power of 8.5 dBm.
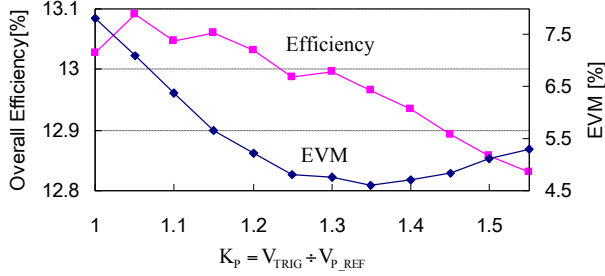

Figure 8. Overall efficiency and EVM performance for various K_P values.

The asynchronous nonlinear path must respond quickly to envelop voltage variations, but fortunately not to current changes. Since the PA is biased in Class-A mode, as mentioned earlier, only small supply current variations occur during peak-to-average power ratio (PAPR) events. This is an important characteristic because the instantaneous voltage across a capacitor is directly proportional to the displacement current flowing through it (fast path current) and its equivalent series resistance (ESR) R_E. Increasing R_E therefore mitigates the current-sourcing requirements of the fast switch, and since the voltage disappears as soon as the fast switch is disengaged, the power consumed as a result of this current is minimal. Increasing the value of R_E (5 Ω in this case), however, increases ripple power losses in the slow switching supply circuit, a description of which follows.

Supply Power Losses: Low power consumption, which manifests itself in the form of low conduction and switching losses, is key to the success of the proposed circuit. Resistive components like the power switches and equivalent series resistors (ESR) $R_{ESR,L}$ and R_E consume conductive power whereas switching power is lost in charging and discharging highly capacitive nodes like the gates of the power switches. In the proposed circuit, $R_{ESR,L}$ and the switches in the slow supply path carry DC current I_{Load} (300 mA in this design) and ac ripple current I_{RIP}, which for the purposes of averaged power simplifies to ripple root-mean square (RMS) current $I_{RIP,rms}$. Resistor R_E, on the other hand, only carries ripple current $I_{RIP,rms}$ (10 mA).

The average power consumed by a switch is therefore

$$P_{Switch} = (I_{Load}^2 + I_{RIP,rms}^2)R_{Switch}d, \qquad (3)$$

where R_{Switch} is the on-resistance of the switch (0.1 Ω) and d is its duty-cycle (i.e., percentage of time it is conducting current). Since one of the two switches must always conduct the total current, the net switching power, assuming both switches have approximately the same switch-on resistance, is

$$P_{Switches} = (I_{Load}^2 + I_{RIP,rms}^2)R_{Switch}, \qquad (4)$$

in other words, 9 mW. Similarly, $R_{ESR,L}$ and R_E (0.05 and 2.5 Ω) consume 4.5 and 0.25 mW,

$$P_{Inductor} = (I_{Load}^2 + I_{RIP,rms}^2)R_{ESR,L}. \qquad (5)$$

and

$$P_E = I_{RIP,rms}^2 R_E. \qquad (6)$$

Switching losses, on the other hand, depend on switching frequency f_{SW}, parasitic capacitance C_{PAR}, and the total voltage variation (battery voltage V_{BAT}) across the gates of the power switches,

$$P_{Switching} = C_{PAR}V_{BAT}^2 f_{SW}, \qquad (7)$$

where C_{PAR} is approximately 100 pF per switch, V_{BAT} is 2.7 V, and f_{SW} is 5 MHz, resulting in a net power loss of 3.6 mW per switch. The total power efficiency is therefore the output power (450 mW at 0.3 A and 1.5 V) to input power (output power plus all power losses, which sum to 471 mW) ratio, yielding 95.5% efficiency. The simulation results of Fig. 9 show close correlation with the foregoing analysis. Efficiency, of course, decreases when load currents are low because RMS and switching losses remain constant as output power is reduced.
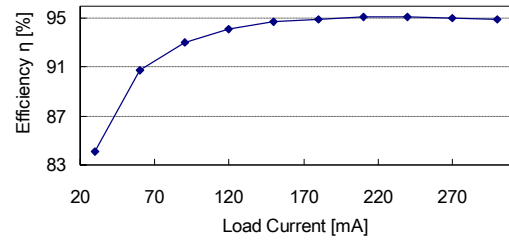

Figure 9. Efficiency dependence of the slow supply circuit to load.

VI. SIMULATION RESULTS

The proposed power-tracking supply was designed and simulated with a single stage, SiGe HBT Class-A RF PA for 802.11g signals. The maximum PA supply voltage and DC bias current were set to 2.5 V and 300 mA, respectively. The input voltage supplied to the DC-DC converter was 2.7 V, which corresponds to the lowest operating voltage of a lithium-ion battery. The two hysteretic comparators used in the supply circuit (Fig. 7) were implemented using SPICE macro-models while the power stage, drivers, and dead-time control circuits were all realized at the transistor level using AMI's CMOS 0.5 um SPICE models.

To prove the validity of the proposed architecture, the same supply circuit without the fast path was used to implement the conventional power-tracking scheme, but adjusting the power-tracking level to achieve the same EVM performance as the proposed architecture (less than 5.6%), as shown in Fig. 10. The performance of a fixed supplied PA was also tested as a reference metric, noting that EVM performance improves with lower output power levels, since linearity is best when there is more headroom across the PA. EVM performance of the conventional power-tracking

scheme improves slightly with lower power levels. This improvement over the proposed scheme is of little consequence when considering the EVM performance is still met.
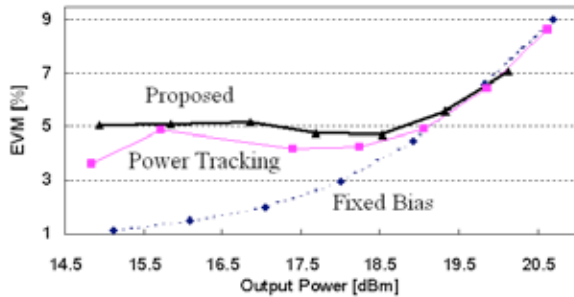

Figure 10. Output power dependence of EVM for various PA schemes.

Fig. 11 shows the transient response performance of the proposed circuit and the conventional power-tracking scheme. As expected, for the same EVM performance, the average power-tracking level of the proposed circuit is 400 mV lower than the conventional version. The overall PA power losses in the proposed circuit (including power supply losses) is consequently 10-15% lower than the state-of-the-art power-tracking scheme, resulting is an overall PA efficiency improvement of 1.5%.
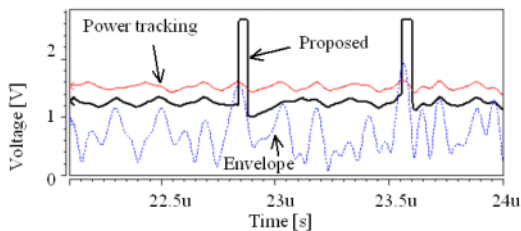

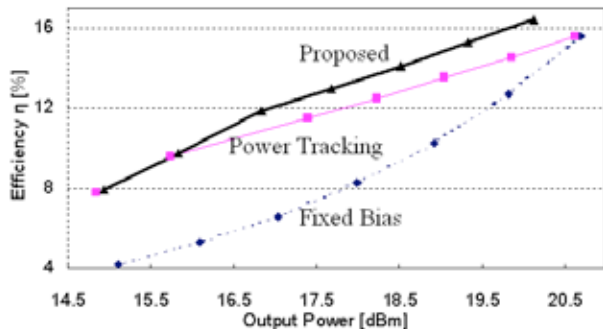Figure 11. Transient response waveforms of the proposed scheme.

Figure 12. Overall PA efficiency performance for various PA schemes.

VII. CONCLUSION

Linearity and power efficiency of wireless power amplifiers (PAs) are intrinsic yet necessarily conflicting. Given the high linearity requirements of modern, spectrally dense wireless signals, power-tracking PA supplies are attractive, and the proposed asynchronous power-tracking architecture has 10-15% lower power losses than state-of-the-art power-tracking schemes, when applied to 802.11g

applications, achieving an overall PA efficiency improvement of 1.5%, all the while meeting the 802.11g EVM standards. The circuit takes advantage of a fast nonlinear path to mitigate the power-tracking headroom requirements of conventional architectures. Although the circuit was applied to 802.11g signals, the proposed technique is expected to outperform conventional power-tracking schemes when processing high envelop bandwidth and high and relatively often peak-to-average power ratio (PAPR) events, as in CDMA IS-95 and WCDMA, because of its fast nonlinear envelop-tracking capabilities. High bandwidth and frequent PAPR events are in fact the side-effects of higher spectral density and therefore future trends.

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